RELIABILITY VERIFICATION REPORT

Apollo3 Blue BGA AMA3B1KK-KBR-B0

A-SOCA3B-RRGA01EN v1.0

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Revision History

Revision	Date	Description
1.0	July 2026	Initial Release.

Reference Documents

Document ID	Description

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Product Information

1.1 Product Information

Table 1-1: Product Information

Product Type:	Ultra-low Power MCU
Part Number:	AMA3B1KK-KBR-B0
Process Technology:	40nm
Foundry:	TSMC
Package Type:	5 x 5 mm 81-pin BGA
Assembly Site:	ASE
Date Code:	261201/261202/261203
Substrate Material:	HL832NS (MGC, E-glass/non-low CTE)

1.2 Qualification Results

Table 1-2: Qualification Reports

Test Item	Conditions	Lot #	Sample Size	Results
Pre SAT	C-Scan + T-Scan	3	24	Pass (No delamination phenomenon on die surface)
Pre-Conditioning (PC)	JESD22-A113; MSL-3	3	75	Pass

Table 1-2: Qualification Reports *(Continued)*

Test Item	Conditions	Lot #	Sample Size	Results
Post SAT	C-Scan + T-Scan	3	24	Pass (No delamination phenomenon on die surface)
High Temperature Storage Life (HTSL)	JESD22-A103; 150°C, 1000hrs	3	25	Pass 1000hr
Temperature Cycle (TC)	JESD22-A104, TC condition B (-55C – 125C) for 700 Cycles	3	35	Pass 700 Cycles
Unbiased Highly Accelerated Stress Test (UHAST)	EIA/JESD22-A118, +130°C / 85%R.H. Unbiased for 96hrs	3	25	Pass 96hr
Biased Highly Accelerated Stress Test (BHAST)	EIA/JESD22-A110, +130°C / 85%R.H. Biased for 96hrs	3	25	Pass 96hr

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Pre-Conditioning (PC)

Table 2-1: Pre-Conditioning (PC)

Test:	Pre-Conditioning (PC)
Purpose:	The Preconditioning test stresses mechanical integrity by exposing a device to moisture soak conditions. Weakness and thermal expansion in die interconnections, die attach, and wire bonds are often detected with this acceleration test.
Conditions:	JESD22-A113; MSL-3 ▪ Electrical Full Functional Test ▪ External Visual Examination ▪ Dry Bake at 125°C for 24 hrs ▪ Soak Devices to appropriate Moisture Level e.g., MSL 3 (30°C/ 60%RH, 192hrs) ▪ IR Reflow with JEDEC Standard Profile, 3 times ▪ External Visual Examination Lot No:
Lot No:	3 lot
Sample Size:	75 ea/ lot
Pass/Fail Criteria:	Zero failure in function test.
Results:	Pass; Refer to Attachment 1 (Reflow profile) and Attachment 2 (SAT Image).

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High Temperature Storage Life (HTSL)

Table 3-1: High Temperature Storage Life (HTSL)

Test:	High Temperature Storage Life (HTSL)
Purpose:	The test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to- failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). Thermally activated failure mechanisms are modeled using the Arrhenius Equation for acceleration. During the test, accelerated stress temperatures are used without electrical conditions applied.
Conditions:	JESD22-A103; +150°C for 1000 continuous hours
Duration:	1000 hrs
Lot No:	3 lot
Sample Size:	25 ea/ 3 lot
Pass/Fail Criteria:	Zero failure in function test.
Results:	Pass 1000hrs

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Temperature Cycle (TC)

Table 4-1: Temperature Cycle (TC)

Test:	Temperature Cycle Test (TC)
Purpose:	Temperature Cycle Testing (TC), or simply temperature cycling or temp cycling, determines the ability of parts to resist extremely low and extremely high temperatures, as well as their ability to withstand cyclical exposures to these temperature extremes. A mechanical failure resulting from cyclical thermomechanical loading is known as a fatigue failure, so temperature cycling primarily accelerates fatigue failures.
Conditions:	JESD22-A104, -55°C to 125°C Air to Air (Pre-Conditioned units)
Duration:	700 Cycles
Lot No:	3 lot
Sample Size:	25 ea/ 3 lot
Pass/Fail Criteria:	Zero failure in function test.
Results:	Pass 700 Cycles

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Unbiased Highly Accelerated Stress Test (UHAST)

Table 5-1: Unbiased Highly Accelerated Stress Test (UHAST)

Test:	Unbiased Highly Accelerated Stress Test (UHAST)
Purpose:	The test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test that employs temperature and humidity under noncondensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it.
Conditions:	EIA/JESD22-A118, +130°C / 85%R.H. Unbiased (Pre-Conditioned units)
Duration:	96 hrs
Lot No:	3 lot
Sample Size:	25 ea/3 lot
Pass/Fail Criteria:	Zero failure in function test
Results:	Pass 96hrs

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Biased High Accelerated Stress Test (BHAST)

Table 6-1: Biased Highly Accelerated Stress Test (BHAST)

Test:	Biased Highly Accelerated Stress Test (BHAST)
Purpose:	The test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.
Conditions:	EIA/JESD22-A110, +130°C / 85%R.H. Biased (Pre-Conditioned units)
Duration:	96 hrs
Lot No:	3 lot
Sample Size:	25 ea/ 3ot
Pass/Fail Criteria:	Zero failure in function test
Results:	Pass 96hrs

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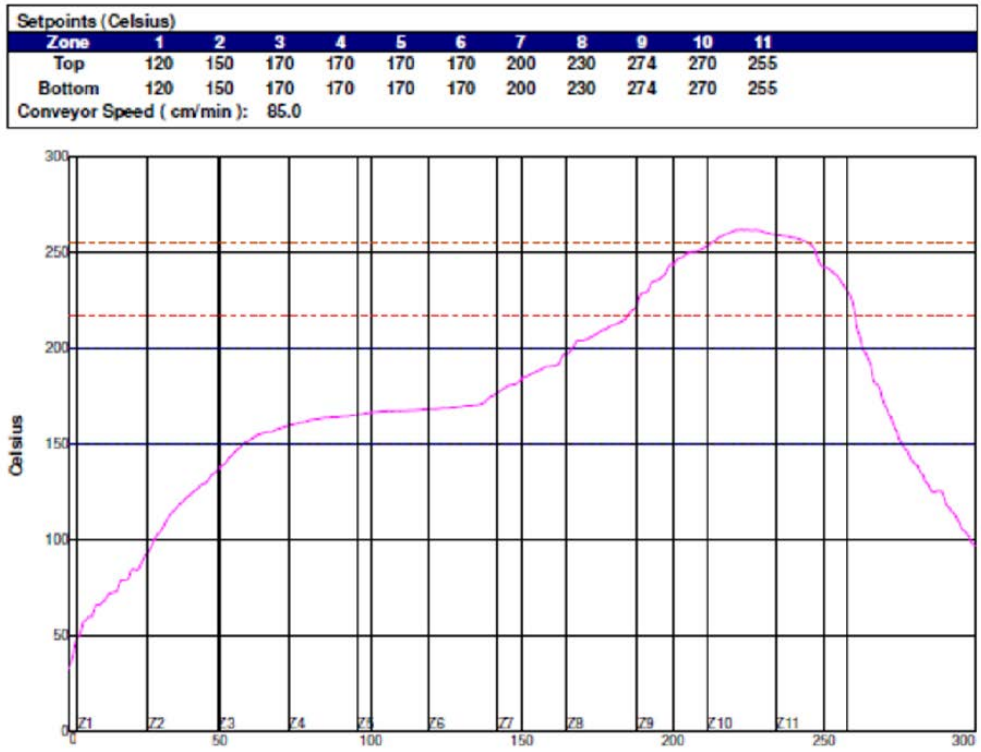
Reflow Profile

Figure 7-1: Reflow Profile



Real Reflow Result：

Peak Temperature	261.84 °C
Average ramp-up rate (217 to peak)	1.62 °C/second
Preheat temperature 150 to 200 °C	109.14 seconds
Temperature maintained above 217 °C	75.18 seconds
Time within 5 °C of actual peak temperature	32.00 seconds
Ramp-Down Rate	1.94 °C/second

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SAT Image

8.1 C-Scan

This section shows the C-Scan pre-color and post-color.

Figure 8-1: C-Scan Pre-Color

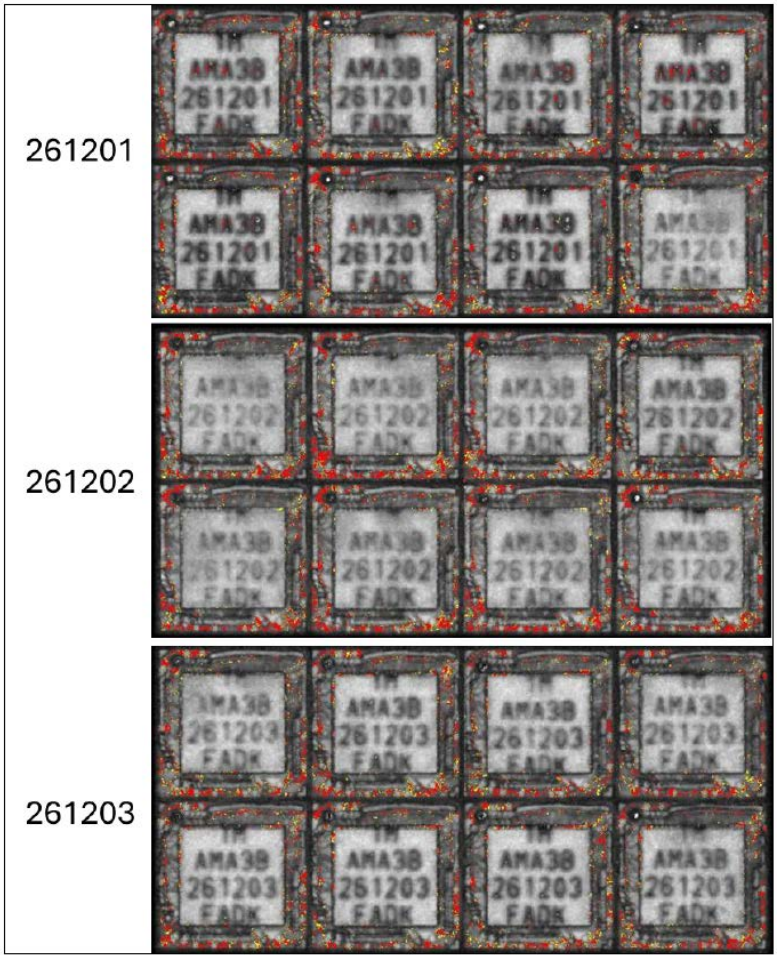
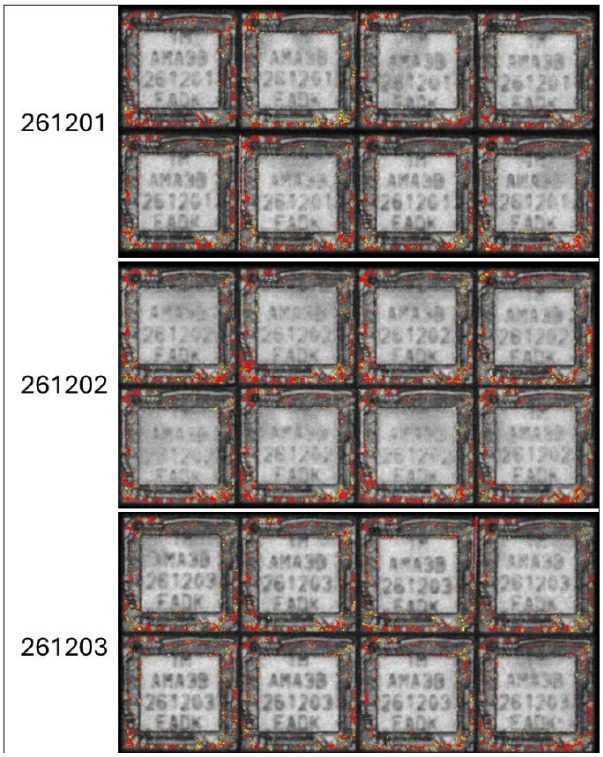


Figure 8-2: C-Scan Post-Color



8.2 T-Scan

This section shows the T-Scan pre and post images.

Figure 8-3: T-Scan Pro Image

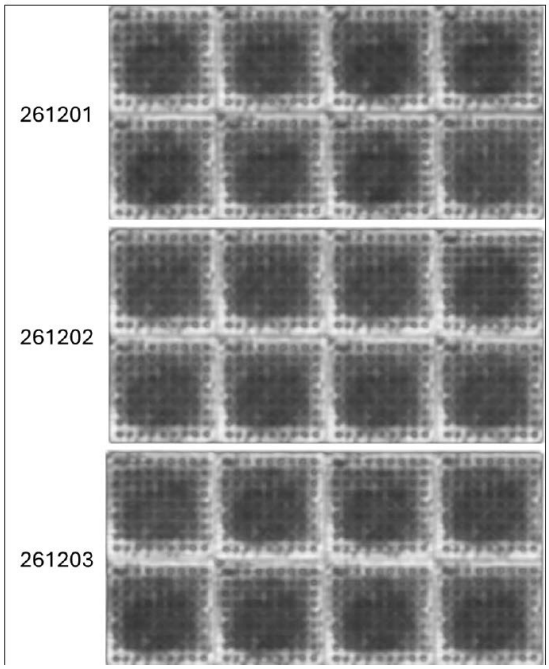
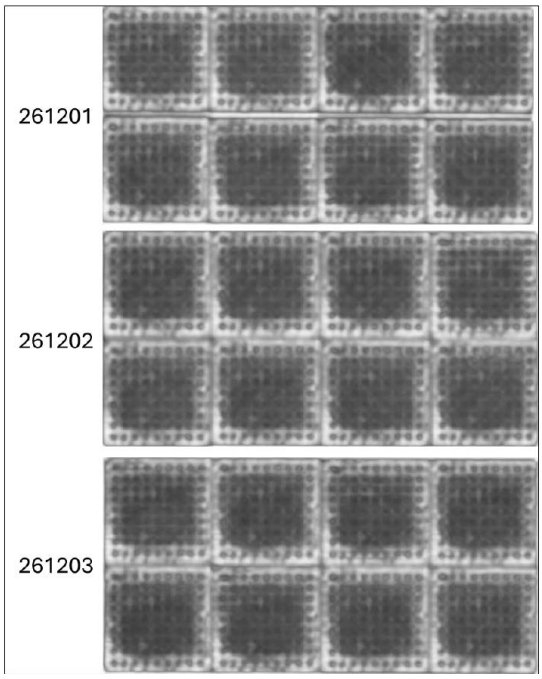


Figure 8-4: T-Scan Pro Image



NOTE: No delamination phenomenon on die surface and substrate.

8.3 Results

Table 8-1: SAT Image Results

Phenomenon	Results
Delamination on die surface	No
Defamination on wire bonding surface	No
Result	Pass

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