FEATURE SUPPORT RESTRICTIONS GUIDE

Applicable to Apollo4 Family SoCs:

Apollo4 / Apollo4 Blue,

Apollo4 Plus / Apollo4 Blue Plus,

Apollo4 Lite / Apollo4 Blue Lite

Ultra-low Power Apollo SoC Family

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Table of Content

Apollo4 Family Feature Support Restrictions

1. Introduction

This document is a detailed compilation of restrictions of feature support in the use of members of the Apollo4 family of Ambiq SoCs. It is intended to inform the user about features and functionality which currently have restrictions and therefore support of their use is limited. The use of any features or functionality beyond what is specified in this document as being supported is at the user's discretion and responsibility. Proper or expected operation of the SoC or its modules for features and functionality outside the scope of support as defined in this document is not guaranteed.

The scope of supported functionality and support restrictions as outlined in this document applies to all members of the Apollo4 family of SoCs except where noted.

2. Document Revision History

Table 1: Document Revision History

Rev No.	Date	Description
1.0	Sep 2021	Initial release for Apollo4 and Apollo4 Blue SoCs
2.0	May 2022	Document updated to apply to all existing general availability Apollo4 family SoCs. All entries for Apollo4 Plus and Apollo4 Blue Plus are new entries. ▪ Apollo4/ Apollo4 Blue: - Added ADC-01 restriction - Added AUDIO-02 restriction - Updated ETM-01 restriction description - Updated DISP-01 supported use cases to note supported frame rate for each SoC; updated configuration B for Apollo4/Apollo4 Blue (60 fps to 50 fps) - Updated IOM-01 restriction description - Updated IOS-01 restriction description - Updated MCUCTRL-01 with note - Updated PWRCTRL-02 restriction description - Updated USB-01 to include restrictions on use of HS mode.
3.0	August 2022	MRAM restrictions updated: ▪ Link to "Design Guidelines for Magnetic Immunity" updated. MSPI restrictions for Apollo4/Apollo4 Plus updated: ▪ Apollo4/Apollo4 Blue: - MSPI2 max clock for all data widths = 24 MHz for SDR (12 MHz for DDR where supported). - Clock on MSPIn_4 is not supported. ▪ Apollo4 Plus/Blue Plus: - Max MSPI2 clock for non-DQS DDR with Octal data width = 12 MHz. - Clock on MSPIn_4 is not supported.
4.0	July 2023	Document updated to include Apollo4 Lite and Apollo4 Blue Lite SoCs support restrictions. Updates of existing restrictions: ▪ PWRCTRL-01 retracted. New restrictions: ▪ MSPI-02 added. ▪ PWRCTRL-03 added.

3. Restrictions List

Table 2 is a list of feature support restrictions. For each feature support restriction, the affected module is listed along with the reference number and title for each restriction, a description of the restriction, and the applicable Apollo4 family SoCs.

IMPORTANT NOTE: There may be a support restriction on a module's use because of an existing chip erratum related to the module's functionality. Consult the latest version of the Errata List for the applicable SoC(s) for possible additional information about a listed support limitation or for additional usage restrictions due to an erratum.

Table 2: Summary of Restrictions

Affected SoC Module/ Feature	Restriction Number and Title	Restriction Description	Applicable SoCs
ADC	ADC-01: Actions required to prevent sample data loss	ERR091 discloses an issue with ADC sample data loss and/or corruption which requires certain action and restricted use: 1. Use ADC clock selection HFRC_24MHZ for all Apollo4 SoCs. 2. Use a TRKCYCx setting of 32 or higher. 3. Enable ADC auto calibration.	All existing
AUDIO	AUDIO-01: Audio modules (AUDADC[a], PDM and I2S) lack hardware circular buffer.	The lack of a circular buffer implemented in hardware means that such a buffer must be implemented in software which will result in a higher level of CPU intervention.	All existing
	AUDIO-02: AUDADC not supported.	Use of the Audio ADC module (AUDADC) is not supported.	▪ Apollo4 ▪ Apollo4 Blue
CLKGEN	CLKGEN-01: 32 MHz clock assertion/deassertion is handled in software	The 32 MHz clock control ISR must be executed in time to provide a stable clock to the BLE module. Please refer to Application Note A-SOCA4B-ANGA01EN, XTAL32MHz CLK Request.	All existing
	CLKGEN-02: Limitation on using XTALHS (XO32M) as a module clock source related with deepsleep mode	In deepsleep mode, since MCUL and MCUH power domains are shut down for power saving, XTALHS cannot be selected as the clock source for those modules for which XTALHS is offered (PDM, I2S or AUDADC) because the clock signal path passes through MCUL and MCUH domains.	All existing
CPU	CPU-01: DAXI buffer and aging counter limitations	The supported DAXI use is with only 1 buffer enabled and the aging counter value set to 2.	▪ Apollo4 ▪ Apollo4 Blue
		No restrictions.	▪ Apollo4 Plus ▪ Apollo4 Blue Plus ▪ Apollo4 Lite ▪ Apollo4 Blue Lite

Table 2: Summary of Restrictions

Affected SoC Module/ Feature	Restriction Number and Title	Restriction Description	Applicable SoCs
ETM	ETM-01: ETM/Trace not supported on Apollo4	ETM is functional, but has a non-standard interface which is complicated to configure, and technical support for configuring ETM is not available. If ETM trace is required, the recommendation is to use another Apollo4 family member such as Apollo4 Plus or Apollo4 Lite, which have a more standard ETM interface.	▪ Apollo4 ▪ Apollo4 Blue
DISPLAY[b]	DISP-01: Display & Graphics supported performance configurations (based on using NemaGUI)	Ambiq recommends the following configurations to achieve the listed frame rate at the specified display size. A. Screen size 390x390, single RGB24 frame buffer in SSRAM, assets in PSRAM, QSPI or DSI interface. Supported frame rate: ▪ 30 fps on Apollo4 / Apollo4 Blue ▪ 50 fps on Apollo4 Plus / Apollo4 Blue Plus B. Screen size 390x390, dual RGB565 frame buffers in SSRAM, assets in PSRAM, DSI interface. Supported frame rate: ▪ 50 fps on Apollo4 / Apollo4 Blue ▪ 60 fps on Apollo4 Plus / Apollo4 Blue Plus C. Screen size 454x454, dual TSC6 frame buffers in SSRAM, assets TSC-compressed in PSRAM, DSI interface. Supported frame rate: ▪ 30 fps on Apollo4 / Apollo4 Blue ▪ 60 fps on Apollo4 Plus / Apollo4 Blue Plus	▪ Apollo4 ▪ Apollo4 Blue ▪ Apollo4 Plus ▪ Apollo4 Blue Plus
		Apollo4 Lite and Apollo4 Blue Lite SoCs do not have a Display Controller. See MSPI-02 for supported frame rates over an MSPI channel.	▪ Apollo4 Lite ▪ Apollo4 Blue Lite
IOMSTR	IOM-01: I2C clock stretching limitation	I2C clock stretching operation is not guaranteed. If an I2C peripheral device that performs clock stretching is used, the recommendation is to perform compatibility testing with the Apollo4 I2C interface.	All existing
IOSLAVE	IOS-01: IOSLAVE has throughput limitations based on CPU utilization	The following host-to-slave communication speeds are supported: Direct Access (Host TX): 100 kHz to 24 MHz FIFO read range (Host RX): 100 kHz - 400 kHz and 16 MHz - 24 MHz.	All existing
MCUCTRL	MCUCTRL-01: Secondary bootloader limitations	The Apollo4 SDK uses dynamic trim adjustments for different operating modes. The software keeps track of the state using global variables to ensure trim adjustments are only applied once. However, if the user's design includes a secondary bootloader, the global software state is not enough to prevent multiple trim adjustments. NOTE: The SDK function am_hal_pwrctrl_settings_restore() was introduced in SDK 4.1.0, which must be called from the base application (e.g., secondary bootloader) before transitioning to another application.	All existing
MRAM	MRAM-01: MRAM is susceptible to external magnetic fields	MRAM magnetic immunity guidelines are provided to assist with end product design. See “Design Guidelines for Magnetic Immunity” in the Ambiq Content portal - https://contentportal.ambiq.com/login.	All existing

Table 2: Summary of Restrictions

Affected SoC Module/ Feature	Restriction Number and Title	Restriction Description	Applicable SoCs
MSPI	MSPI-01: MSPI implementation and clock limitations	The following restrictions apply to Apollo4 MSPI operation: ▪ Maximum SDR clock rate is 48 MHz. ▪ Maximum DDR clock rate is 24 MHz. ▪ MSPI2 has a maximum clock rate for all data widths of 24 MHz for SDR (12 MHz for DDR where supported). ▪ MSPI1 is limited to Quad SDR only - Quad DDR and Octal (SDR or DDR) not supported. ▪ Clock on MSPIn_4 is not supported. ▪ DQS operation is not supported. ▪ CQ/DMA usage is restricted. See erratum ERR063 regarding early shutdown during receive.	▪ Apollo4 ▪ Apollo4 Blue (MSPI1 not available on Blue SoCs)
		The following restrictions apply to Apollo4 Plus MSPI operation: ▪ Maximum supported SDR clock rate is 96 MHz. - Non-DQS SDR Octal not supported at 48 MHz or 96 MHz; recommend using DQS mode. ▪ Maximum supported DDR clock rate is 48 MHz. - Maximum supported MSPI2 clock rate for non-DQS DDR with Octal data width is 12 MHz. ▪ Clock on MSPIn_4 is not supported. ▪ CQ/DMA usage not restricted providing workaround of ERR080 is followed.	▪ Apollo4 Plus ▪ Apollo4 Blue Plus (MSPI1 not available on Blue Plus KBR package)
		The following restrictions apply to Apollo4 Lite MSPI operation. Only the specified configurations are supported. ▪ Maximum clock rate for DQS SDR or DDR in Octal width for all MSPI's is 48 MHz. ▪ Maximum clock rate for non-DQS SDR or DDR in Octal width for MSPI0 and MSPI1 is 48 MHz. ▪ Maximum clock rate for non-DQS SDR or DDR in Octal width for MSPI2 is 12 MHz. ▪ Maximum clock rate for non-DQS SDR in Quad, Dual or serial widths for all MSPIs is 96 MHz. ▪ Maximum clock rate for non-DQS or DQS DDR in HexSPI width for MSPI0 is 48 MHz. ▪ Clock on MSPIn_4 is not supported. ▪ CQ/DMA usage not restricted providing workaround of ERR080 is followed.	▪ Apollo4 Lite ▪ Apollo4 Blue Lite
	MSPI-02: Supported display frame rates based on using NemaGUI over MSPI interface	A. Screen size 390x390, 24-bit resolution, single RGB24 frame buffers in SSRAM, assets in PSRAM, 48 MHz MSPI QSPI interface (TE disabled). Supported frame rate: ▪ 30 fps on Apollo4 Lite / Apollo4 Blue Lite B. Screen size 456x456, single RGB565 frame buffers in SSRAM, assets in PSRAM, 48 MHz MSPI QSPI interface (TE disabled). Supported frame rate: ▪ 30 fps on Apollo4 Lite / Apollo4 Blue Lite	▪ Apollo4 Lite ▪ Apollo4 Blue Lite
POWER	POWER-01: Power supply voltage range limitation	The minimum recommended voltage for VDDA/VDDP/ VDDH is 1.75 V.	All existing

Table 2: Summary of Restrictions

Affected SoC Module/ Feature	Restriction Number and Title	Restriction Description	Applicable SoCs
PWRCTRL	PWRCTRL-01: High-performance/Low-power (HP/LP) debugger connection issue	Sustained debugger operation during HP/LP transitions is not guaranteed. Edit v4.0: Issue is resolved in SDK. Restriction is retracted.	None
	PWRCTRL-02: LDO Mode is restricted from use	The use of LDO Mode is restricted to only LP mode. The SIMO Buck should be used if using HP mode.	All existing
	PWRCTRL-03: Operating temperature	Supported operating temperature range is -20°C to 60°C.	All existing
RSTGEN	RSTGEN-01: Reset hardware workaround.	A 2.2 µF capacitor between VDDF and VDDP is recommended in order to ensure proper operation of POR circuitry at start-up.	All existing
SDIO	SDIO-01: SDIO interface limitations	The SDIO interface is limited to eMMC use only. In addition, only bare metal operation is supported at a maximum clock frequency of 48 MHz SDR or 24 MHz DDR.	▪ Apollo4 ▪ Apollo4 Blue
		The SDIO interface is limited to eMMC use only. In addition, only bare metal operation is supported at a maximum clock frequency of 96 MHz SDR.	▪ Apollo4 Plus ▪ Apollo4 Blue Plus ▪ Apollo4 Lite ▪ Apollo4 Blue Lite
	SDIO-02: DDR modes not supported	Because of ERR088, only SDR mode is supported for SDIO.	▪ Apollo4 Plus ▪ Apollo4 Blue Plus ▪ Apollo4 Lite ▪ Apollo4 Blue Lite
SECURITY/ CRYPTO	SECURITY-01: Secure LCS not supported		All existing
TIMER	TIMER-01: The set of usable timers and their functionality are limited	Timers 0, 2, 4 or 6 are supported for triggering application use. Timers 5, 7, 8 and 9 are supported for use in applications not requiring/using triggering. DOWNCOUNT mode is not supported. For functional limitations on (all) timers, please refer to ERR059 in the Apollo4 Errata List.	▪ Apollo4 ▪ Apollo4 Blue
		DOWNCOUNT mode is not supported.	▪ Apollo4 Plus ▪ Apollo4 Blue Plus ▪ Apollo4 Lite ▪ Apollo4 Blue Lite
UART	UART-01: UART baud rate limitation	The maximum supported UART baud rate is 1.5 Mbps.	All existing
USB[c]	USB-01: USB use case restrictions	The USB is only supported for firmware updates, debugger I/O, and serial logging output. High-speed mode is restricted to use cases where the CPU can be completely dedicated to the USB task.	▪ Apollo4 ▪ Apollo4 Blue ▪ Apollo4 Plus ▪ Apollo4 Blue Plus
	USB-02: Proper operation during simultaneous USB and BLE operation is not guaranteed.	Due to interference between USB power circuitry and the BLE Controller, BLE performance is not guaranteed during simultaneously USB operation.	▪ Apollo4 ▪ Apollo4 Blue ▪ Apollo4 Plus ▪ Apollo4 Blue Plus

a. AUDADC is not available on Apollo4 Lite / Apollo4 Blue Lite SoCs.
b. Display Controller and DSI module not available on Apollo4 Lite / Apollo4 Blue Lite SoCs.
c. USB is not available on Apollo4 Lite / Apollo4 Blue Lite SoCs.

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