DESIGN GUIDE

Apollo Bluetooth Low Energy SoC RF Hardware

Ultra-Low Power Apollo SoC Family

A-SOCAPG-DGGA01EN v1.0

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Revision History

Revision	Date	Description
1.0	April 1, 2024	Initial release

Reference Documents

These reference documents can be accessed on the Ambiq Website and/or Content Portal.

Document ID	Description
DS-A3-*	Apollo3 Blue SoC Datasheet
DS-A4B-*	Apollo4 Blue SoC Datasheet
	Apollo3 Blue AMA3B1KK-KBR EVB Schematic
	Apollo4 Blue Plus KBR EVB AMA4BPEVB Rev1.0 Schematic

*Indicates to use the latest version of the document.

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SECTION

1

Introduction

RF design is critical for radio systems to achieve optimum performance that does not only extend the operating range and improve communication quality but can also coexist with other in-band and out-of-band wireless technologies.

Each generation of Apollo series SoC also has a 'Blue' version integrated with Bluetooth Low Energy subsystem, such as Apollo3 Blue series (including Apollo3 Blue Plus), Apollo4 Blue series (including Apollo4 Blue Plus and Apollo4 Blue Lite), and more. The present document provides general RF design guidelines for these Apollo 'Blue' series which can help users reference and implement in their targeted end-product applications.

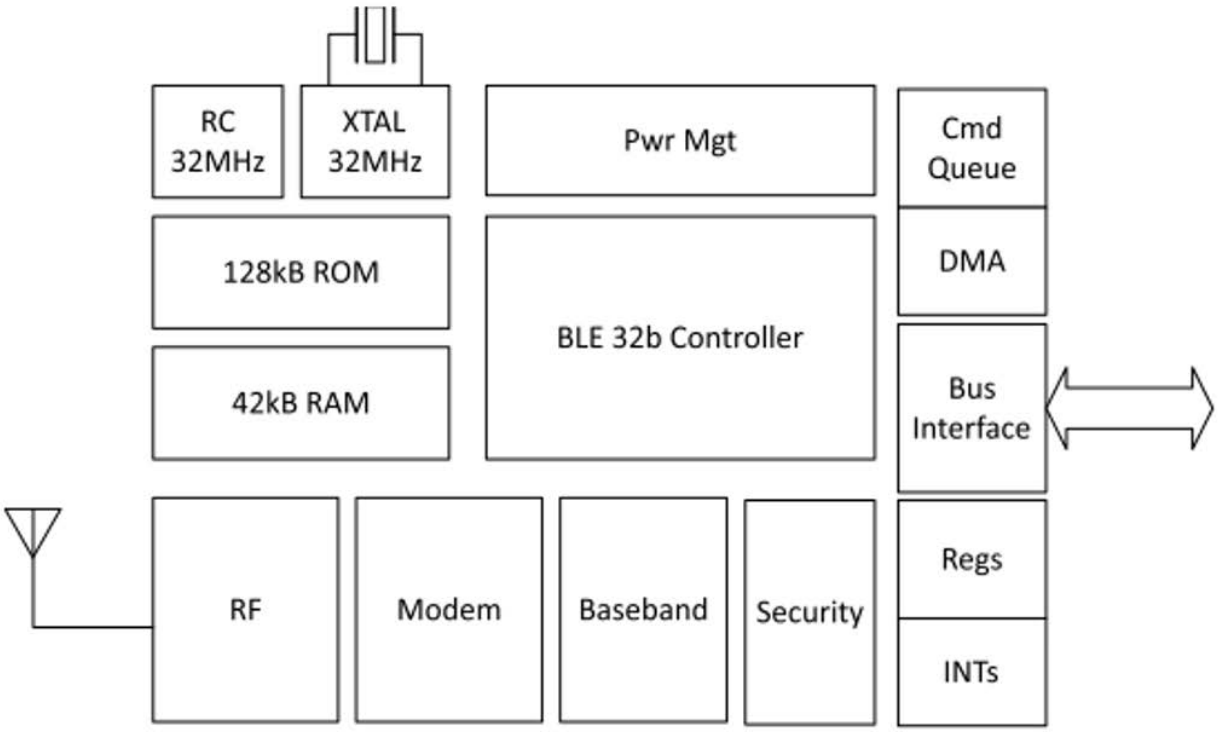
SECTION

2

Overview

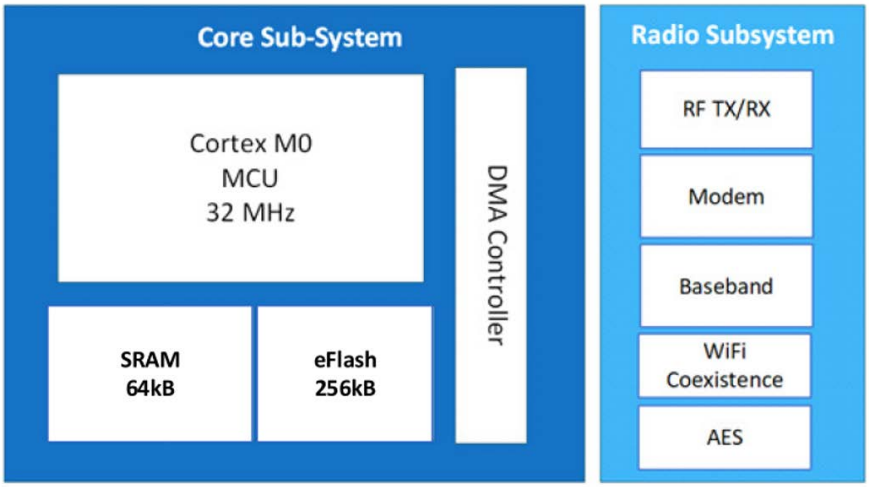
The Apollo Blue series SoCs are integrated with one Bluetooth Low Energy subsystem, where Apollo3 Blue is shown in below Figure 2-1 and Apollo4 Blue shown in Figure 2-2 on page 9 They both incorporate one Arm Cortex-M0 core, Bluetooth Low Energy baseband, modem and 2.4GHz RF transceiver. They also provide corresponding PMU, clocking, digital I/Os, dedicated RAM, ROM and embedded Flash[1,2].

Figure 2-1: Block diagram of Bluetooth Low Energy subsystem in Apollo3 Blue SoC



[1] See Apollo3 Blue SoC Datasheet.
[2] See Apollo4 Blue SoC Datasheet.

Figure 2-2: Block Diagram of Bluetooth Low Energy Subsystem in Apollo4 Blue SoC

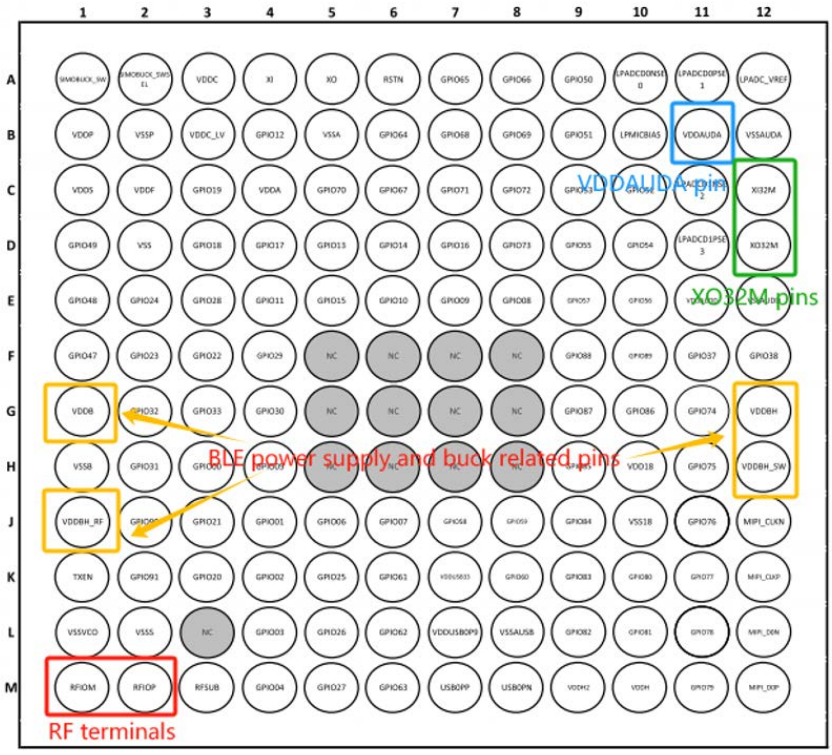


The Apollo3 Blue is provided with a 5×5 mm, 81-pin BGA package (also available in3.37×3.25 mm WLCSP package form), and its pinout is shown in Figure 2-3. The Apollo4 Blue series is provided with a 4.7×4.7 mm, 131-pin BGA package, and its pinout is shown in Figure 2-4 on page 10. For both options, the Bluetooth Low Energy module related pins (including RFIOs, power supply, XO32M) are highlighted with various boxes of different colors in below figures. The RF related terminals (RFIOP and RFIOM pins) are located at the left bottom corner to route RF signal out as short as possible[1,2].

Figure 2-3: Apollo3 Blue SoC BGA Package Pinout Diagram

[1] See Apollo3 Blue SoC Datasheet.
[2] See Apollo4 Blue SoC Datasheet.

Figure 2-4: Apollo4 Blue SoC BGA Package Pinout Diagram



SECTION

3

RF Basics

3.1 Radio Frequency Band

RF (radio frequency) is the oscillation rate of an alternating electric current or electromagnetic field in the frequency range from around 3 MHz to around 300 GHz. These are the frequencies at which energy from an oscillating current can radiate off an antenna into free space as EM waves. A radio band is a small frequency band where channels are usually used or set aside for the same purpose. Different frequency band specifies different upper and lower bounds for the frequency range shown as following Table 3-1 which are defined by ITU[1].

Table 3-1: Radio Spectrum Definition

Band Name	Frequency Range	Wavelength Range	Notes
VLF (Very low frequency)	3 ~ 30 kHz	100 ~ 10 km	
LF (Low frequency)	30 ~ 300 kHz	10 ~ 1 km	
MF (Medium frequency)	300 ~ 3000 kHz	1000 ~ 100 m	
HF (High frequency)	3 ~30 MHz	100 ~ 10 m	RF starts from here
VHF (Very high frequency)	30 ~ 300 MHz	10 ~ 1 m	
UHF (Ultra high frequency)	300 ~ 3000 MHz	100 ~ 10 cm	BLE operates here
SHF (Super high frequency)	3 ~ 30 GHz	10 ~ 1 cm	
EHF (Extremely high frequency)	30 ~ 300 GHz	10 ~ 1 mm	
THF (Terahertz)	300 ~ 3000 GHz	1 ~ 0.1 mm	

Thus, Bluetooth devices operate in the unlicensed 2400~2483.5 MHz ISM (industrial, scientific, medical) band and fall within the UHF spectrum (0.3~3 GHz). Unlicensed means users do not have to apply for a radio license from the local

[1] https://en.wikipedia.org/wiki/Radio_spectrum#IEEE_radar_bands

regulatory agencies while employing relevant wireless technologies located in these bands.

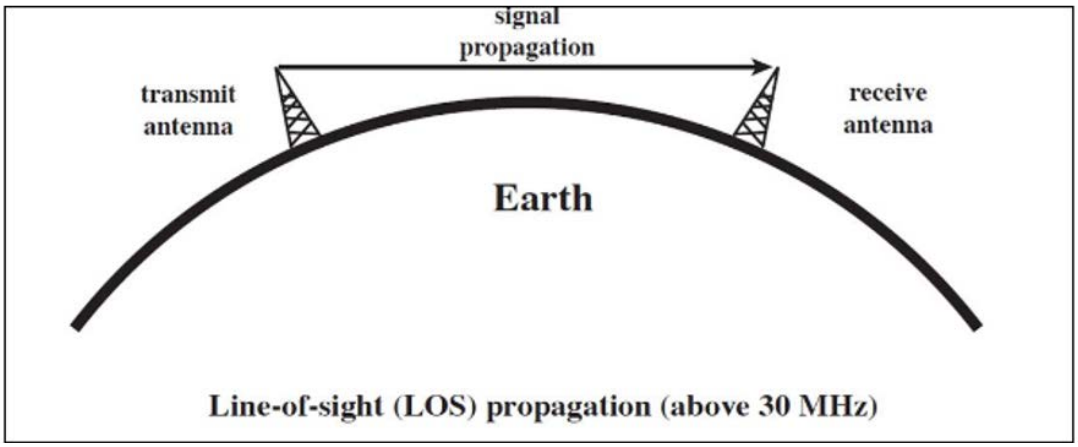
3.2 Radio Propagation Model

There are three typical radio propagation types for radio waves radiated in the free space:

- Ground wave propagation (VLF, LF, MF bands)
- Sky wave propagation (MF and HF bands)
- Line-of-sight (LOS) propagation (VHF band and above)

For Bluetooth devices, the propagation mode mainly refers to LOS. It's the most common propagation mode at VHF band and above which means far-field EM waves which travel in a straight line from the transmitting antenna to the receiving antenna. LOS transmission on the surface of the Earth is limited to the distance to the visual horizon, which depends on the height of transmitting and receiving antennas. The following Figure 3-1 depicts this propagation mode clearly.

Figure 3-1: Line-of-sight (LOS) Propagation



Radio wave propagation is affected by atmospheric conditions, ionospheric absorption, and the presence of obstructions, for example buildings or mountains. Disregarding those influential factors, the maximum LOS distance *d* (unit: km) is only depending on the Earth's radius *R*, the altitude height of transmit antenna (H_1) and receive antenna (H_2) respectively and given by the Pythagorean theorem:

$$d_{km} = \sqrt{(R + H_1)^2 - R^2} + \sqrt{(R + H_2)^2 - R^2} \qquad \text{Equation 3-1}$$

Since the height of antenna H_1, H_2 (unit: m) are much less than the radius of the Earth *R* (unit: km), so they can be ignored in final calculation and expressed by the following formula:

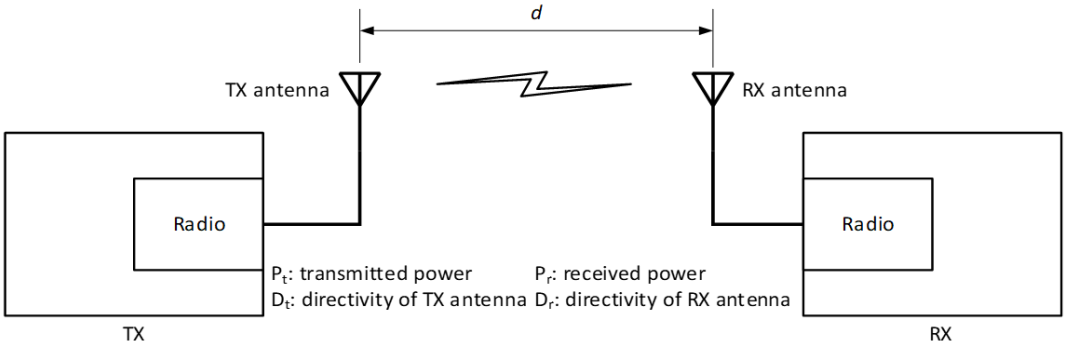
$$d_{km} \approx 3.57\left(\sqrt{H_1(meters)} + \sqrt{H_2(meters)}\right) \quad \text{Equation 3-2}$$

The simple formula gives a best-case approximation of the maximum LOS propagation distance but are not sufficient to estimate the real operating range in a radio system[1].

3.3 Free Space Path Loss

In radio systems as shown in Figure 3-2, the free-space path loss (FSPL) is the attenuation of radio energy through free space (usually air) between the feedpoints of two antennas. The FSPL is a factor that must be included in the power link budget of a radio communication system, to ensure that sufficient radio power reaches the receiver. However, in most cases radio communication takes place in and around buildings, around trees and mountains, and more, that will make the analysis more difficult. The discussion in this case is only on free space situation.

Figure 3-2: Typical Radio System



The FSPL formula derives from the Friis transmission equation. This states that in a radio system consisting of a transmit antenna transmitting radio waves to a receive antenna, the ratio of radio wave power received P_r to the power transmitted P_t is:

$$\frac{P_r}{P_t} = D_t D_r \left(\frac{\lambda}{4\pi d}\right)^2 \quad \text{Equation 3-3}$$

Where:

- P_t is the power delivered to the feed point of transmit antenna.
- P_r is the available power at the receive antenna terminals.
- D_t is the directivity of the transmitting antenna.
- D_r is the directivity of the receiving antenna.

The distance between the antennas d must be much larger than the signal wavelength λ that ensures the antennas are in the far field of each other. Assuming the

[1] https://en.wikipedia.org/wiki/Radio_propagation#Free_space_propagation

antennas are isotropic and have no directivity ($D_t = D_r = 1$), the FSPL can be expressed by the ratio of power transmitted to power received:

$$FSPL = \frac{P_t}{P_r} = \left(\frac{4\pi d}{\lambda}\right)^2 = \left(\frac{4\pi df}{c}\right)^2 \quad \text{Equation 3-4}$$

Beside the assumption that the antennas are lossless, this formula assumes that the polarization of the antennas is the same, that there are no multipath effects, and that the radio wave path is sufficiently far away from obstructions that it acts as if it is in free space. A convenient way to express FSPL is in terms of decibels (dB):

$$FSPL_{(dB)} = 20\log d_{(m)} + 20\log f_{(Hz)} - 147.55 \quad \text{Equation 3-5}$$

For Bluetooth applications operating at 2.4GHz ISM band, the FSPL is roughly calculated at around 80 dB at 100 meters distance and 40 dB at 1 meter distance, and along with the distance increasing doubled the attenuation will get more by 6dB[1].

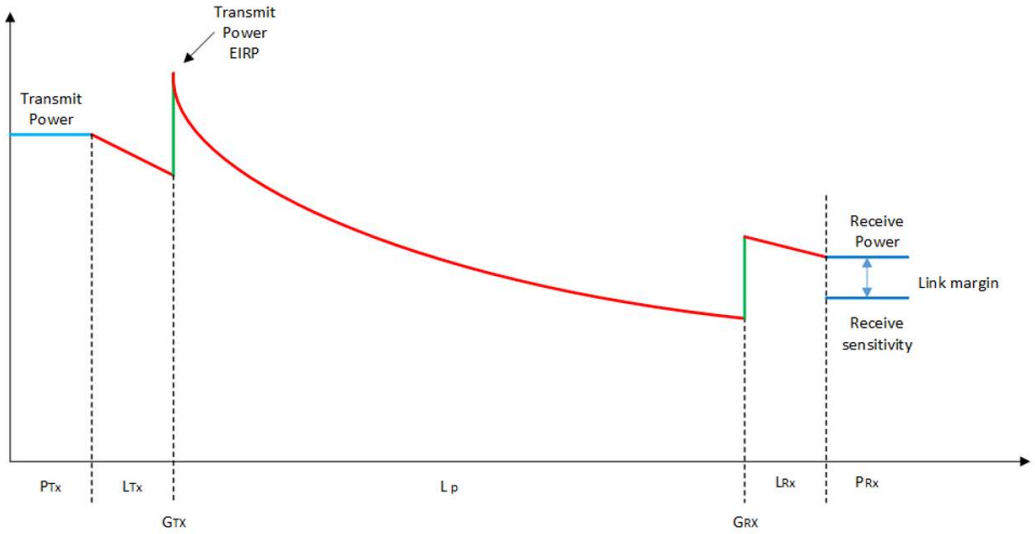
3.4 Link Budget

A communication link budget is an accounting of all the power gains and losses that an RF signal experiences in a radio system; from a transmitter, through a communication medium such as air to the receiver. It is an equation giving the received power from the transmitting power, after the attenuation of the transmitted signal due to propagation, as well as the antenna gains and feedline and other losses, and amplification of the signal in the receiver[2].

Therefore, by knowing all the gains and losses in RF systems we can predict how reliably the signal can be received. Link budget is very useful in point-to-point communication systems to determine the relation between received power and transmitted power, to ensure that the data is received robustly with an adequate signal-to-noise ratio and packet error rate. The following Figure 3-3 on page 15 shows a graphical representation of link budget.

[1] https://en.wikipedia.org/wiki/Free-space_path_loss
[2] https://en.wikipedia.org/wiki/Link_budget

Figure 3-3: Link Budget



A complete link budget equation that allows calculation of received power must consist of the following parameters:

- P_{TX}: transmitted power level
- L_{TX}: transmitter losses (coax cable, connectors, etc.)
- G_{TX}: transmitter antenna gain
- L_P: propagation loss, usually free space path loss
- G_{RX}: receiver antenna gain
- L_{RX}: receiver losses (coax cable, connectors, etc.)
- P_{RX}: received power level.

To calculate the received power level, combine the above parameters (note all of them are expressed logarithmically):

$$P_{RX} = P_{TX} - L_{TX} + G_{TX} - L_P + G_{RX} - L_{RX} \qquad \text{Equation 3-6}$$

Since the communication conditions fluctuate in real world, it is important to leave a margin between the minimum receiver sensitivity and the actual received power level to account for various other losses such as multi-path fading effects, antenna polarization mismatch, Doppler shift, and more. This can ensure communication reliability through link budget estimation[1].

[1] https://en.wikipedia.org/wiki/Link_budget

SECTION

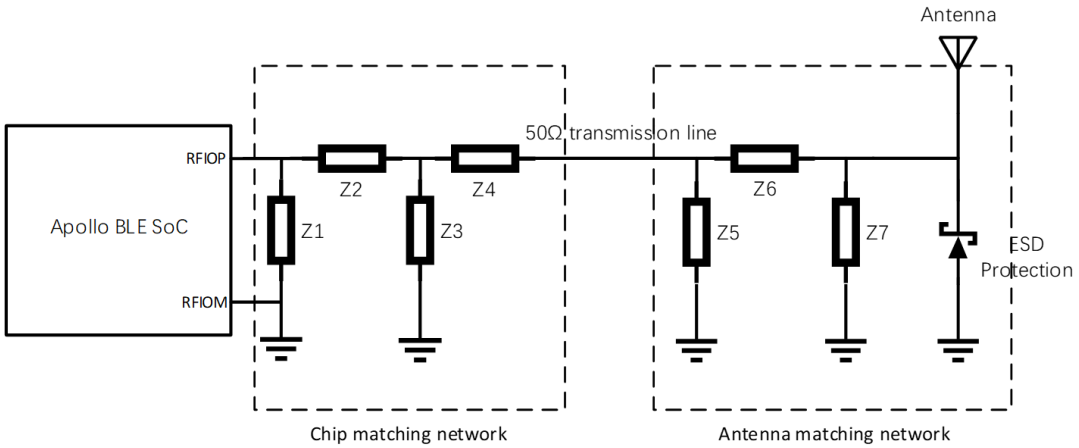
4

RF Schematic Design Guide

4.1 RF Front-end Matching Topology

For RF front-end design with Apollo series Bluetooth Low Energy SoC in user's R&D stage, it is strongly recommended to reserve two 4-element matching network where they are placed close to chip and antenna respectively. As is shown in Figure 4-1, the chip matching network is used for impedance matching for chip RF terminal (single-ended RFIOP) as well as the antenna matching network is used for antenna impedance matching purpose. The 4-element network has the most flexible advantage that can be combined as various impedance matching topology such as 2-element reverse L-type, 3-element Π-type or T-type, 4-element double reverse-L type, and more. Simultaneously, the PCB trace between chip and antenna should be routed as 50Ω transmission line. In addition, for end applications one ESD protection diode should be placed nearby antenna metal contact as close as possible to prevent degradation or damage from ESD events.

Figure 4-1: The proposed RF front-end design for Apollo BLE SoC



The discrete *Z1~Z8* elements marked in above figure can be mounted as resistor, capacitor, or inductor. The specific component type depends on the original RF port impedance, filtering topology (low-pass or high-pass, Chebyshev or Butterworth, and filtering orders) as well as the component values are determined by specific PCB parasitic parameters and tuned to optimal values. Note that although capacitors and inductors are mostly utilized for impedance matching, sometimes 0-ohm resistors are needed for helping matching process and mounted for final use.

Nowadays end products PCB get more and more complex and there are no extra room for placing more devices and components in their compact design. Nevertheless, for providing more competitive and differential products, the multi-element matching network topology is proposed to reserve in product prototype design phase. Once the RF performance meets expectations with less LC elements, the number of components can be minimized in final product design.

4.2 RF Front-end Reference Design

The following Figure 4-2 and Figure 4-3 show the example of RF front-end design schematic and LC component type and value on Apollo3 Blue EVB and Apollo4 Blue EVB respectively. One 3-element T-type matching network consist of 2×inductors and 1×capacitor was used for chip RFIO side matching, and one 3-element Π-type matching network consist of 2×capacitors and 1×inductor was used for PCB antenna side matching.

Figure 4-2: RF Front-end Design on Apollo3 Blue EVB Board

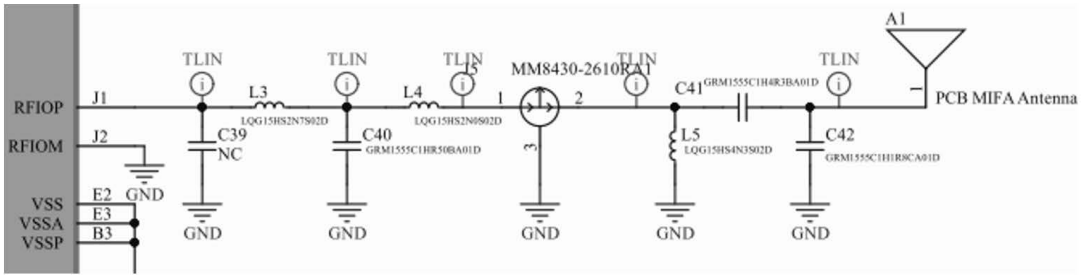
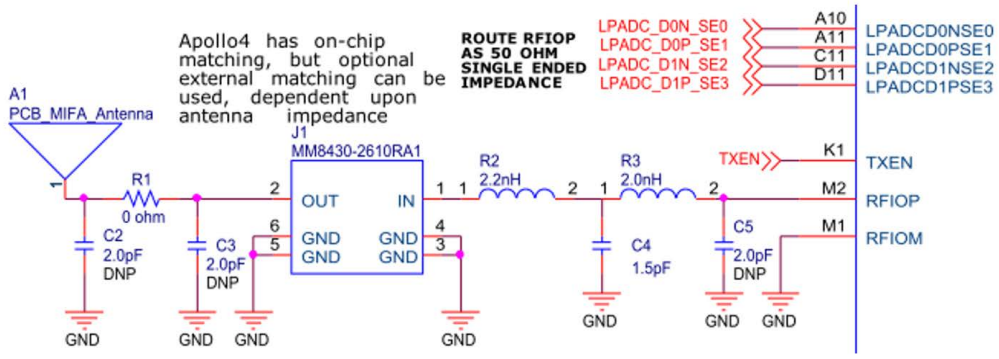
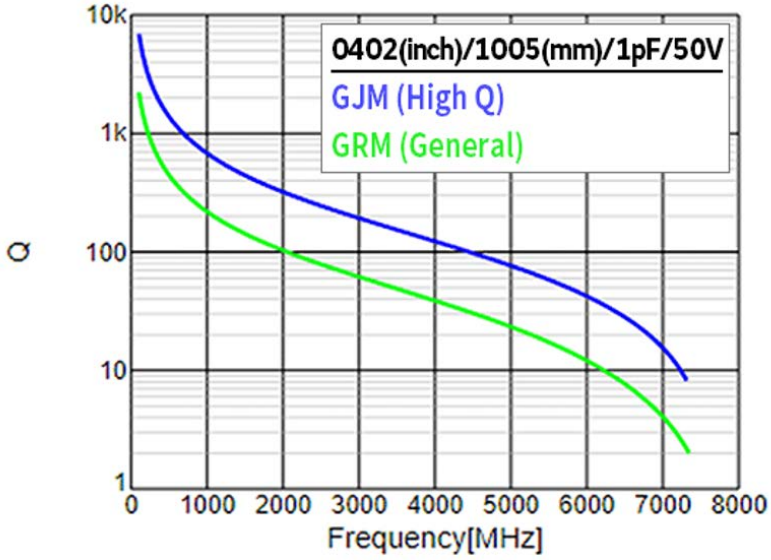


Figure 4-3: RF Front-end Design on Apollo4 Blue EVB Board



Regarding the LC components used for impedance matching, it is strongly recommended to selecting *Hi-Q* value (high SRF), low ESR (low DC resistor) inductors and capacitors for dedicated RF use. For example, according to Murata's official data the compared Q value of GRM and GJM capacitor series is given in below Figure 4-4. Obviously, the GJM series has higher Q performance than GRM series. So GJM series are more suitable for RF applications than GRM series, but they will be more expensive as well[1].

Figure 4-4: The Q Value vs Frequency Curves Between GRM and GJM Series



For Apollo Bluetooth Low Energy SoC, the suggested component value range for chip matching network is given in below Table 4-1. Employing appropriate LC component part number is very important for RF applications since this means an extremely low loss at high frequency[2].

Table 4-1: LC Component Recommendation for Matching

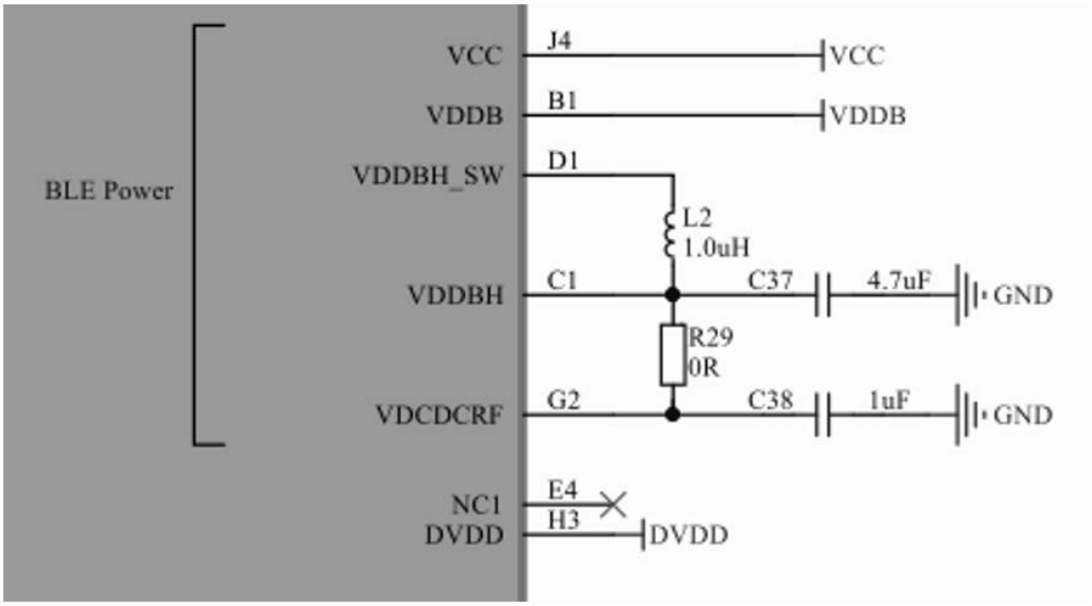
Component Type	Recommended Series	Component Value Range
Inductor L	LQG, LQP, LQW	1 ~ 3.9 nH
Capacitor C	GRM, GJM	0.5 ~ 3 pF

4.3 RF Power Supply Reference Design

In addition to RF front-end design suggestion, the user must also need to take care of the power supply portion for Bluetooth Low Energy subsystem since the RF power supply is as important as RF design itself. The following Figure 4-5 on page 19 shows the Bluetooth Low Energy power supply reference design for Apollo3 Blue.

[1] https://www.murata.com/en-us/products/capacitor/ceramiccapacitor/overview/lineup/smd/gjm
[2] https://www.murata.com/en-global/products/inductor/chip

Figure 4-5: BLE Power Supply Reference Design for Apollo3 Blue Series



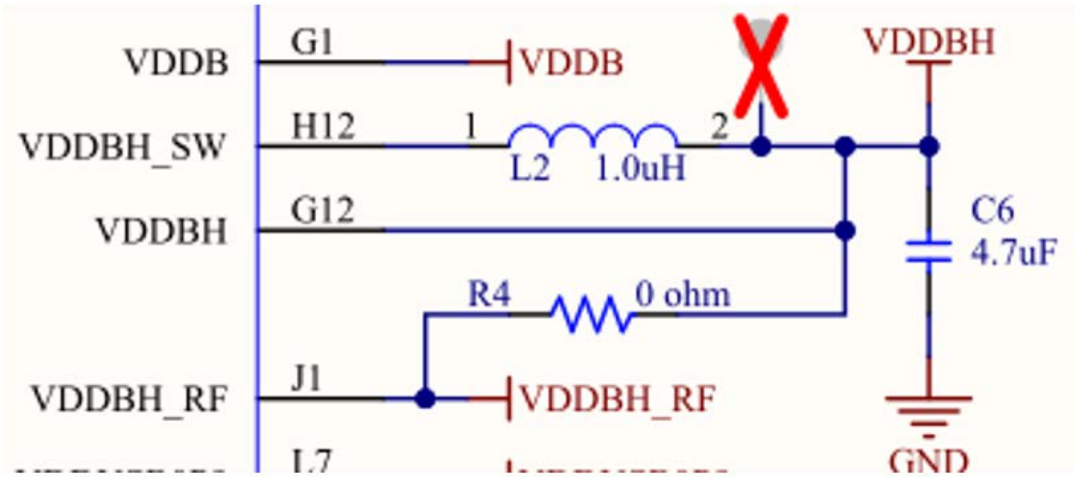
And the following Table 4-2 lists these Bluetooth Low Energy power supply related pins' function and their connection, precautions that would bring impact on practical use.

Table 4-2: BLE Power Supply Related Pins Description for Apollo3 Blue

Pin Name	Function	Description	Precautions
VDDB	BLE buck input	Connect to main power domain VDD_MCU	decoupling by one 2.2μF capacitor
VCC	BLE RF power supply (High supply voltage)		decoupling by one 1μF capacitor
VDDBH_SW	BLE buck inductor switch	Connect 1μH power inductor between them	
VDDBH	BLE buck output		decoupling by one 4.7μF capacitor
VDCDCRF	BLE RF power supply (Low supply voltage)	Connect to VDDBH through one 0Ω resistor or ferrite bead	decoupling by one 1μF capacitor
DVDD	BLE digital power domain output	BLE digital circuit part power output pin	decoupling by one 47nF capacitor

For Apollo4 Blue series, the Bluetooth Low Energy related power supply is basically similar with Apollo3 Blue but more simplified (reduced corresponding power supply pin numbers).

Figure 4-6: BLE Power Supply Reference Design for Apollo4 Blue Series



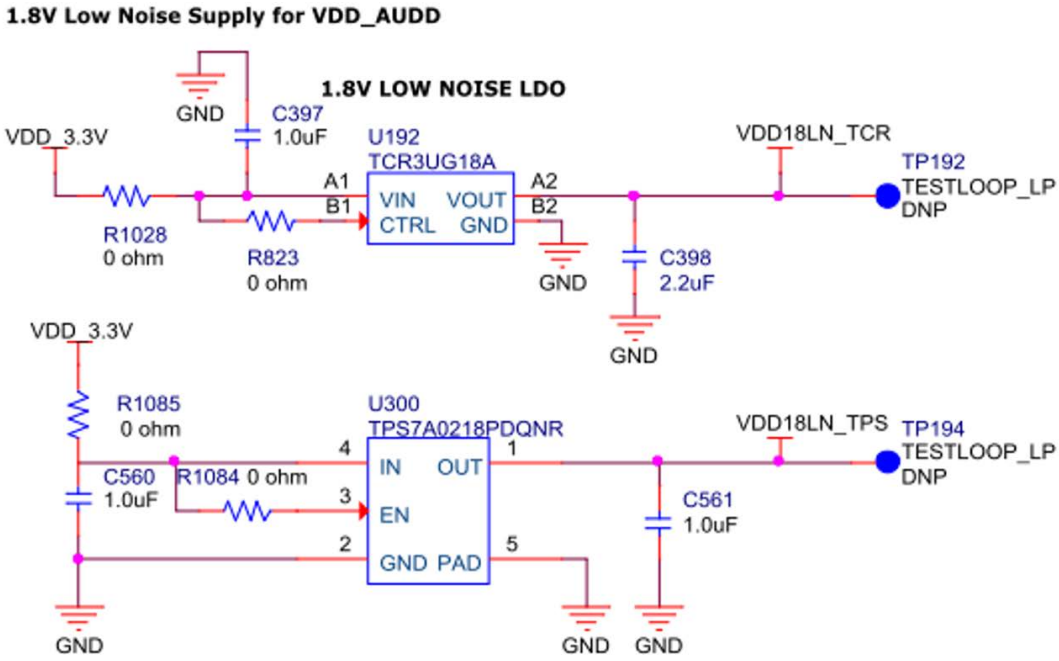
The following Table 4-3 also lists these pins' function, connection and their precautions when designing schematic in end applications.

Table 4-3: BLE Power Supply Related Pins Description for Apollo4 Blue

Pin Name	Function	Description	Precautions
VDDB	BLE power supply input	Connect to main power domain VDD_MCU	decoupling by one 2.2μF capacitor
VDDBH_SW	BLE buck inductor switch	Connect 1μH power inductor between them	
VDDBH	BLE buck output		decoupling by one 4.7μF capacitor
VDDBH_RF	BLE RF power supply input	Connect to VDDBH through one 0Ω resistor or ferrite bead	decoupling by one 1μF capacitor
VDDAUDA	Analog audio power supply input	BLE XO32M would be affected by it	must generated by one low noise LDO

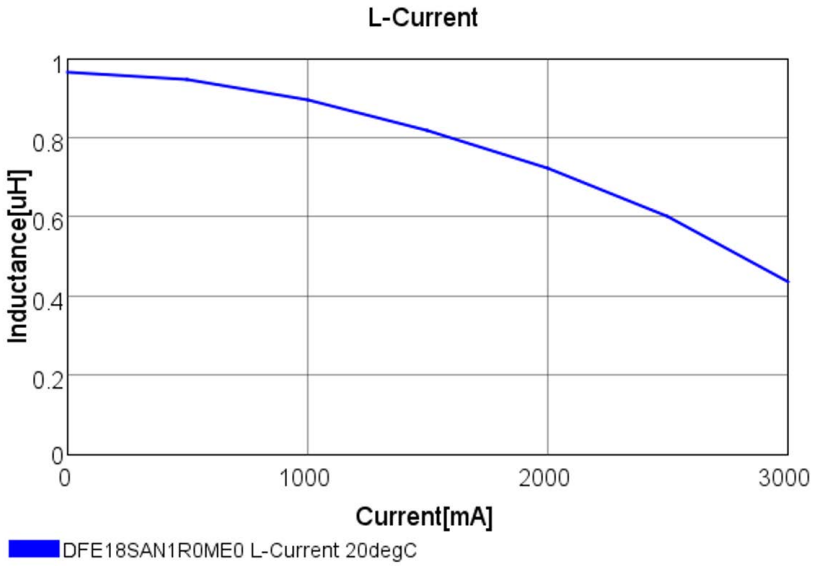
The difference from Apollo3 Blue is the extra power domain VDDAUDA that was used for analog/audio power supply. VDDAUDA needs to be supplied by one dedicated low noise LDO since BLE 32MHz clock will be greatly impacted by it. Hereunder is the reference LDO design.

Figure 4-7: Low Noise LDO Power Supply for VDDAUDA



Note both BLE buck circuits need one external 1µH power inductor between buck switch and output pins. For this 1µH inductor there are some cautions need to be treated seriously. It should meet the saturation current greater than 800mA when the inductance drops 20%, the DCR should be less than 0.55Ω and the SRF should be greater than 20MHz. Hereunder shows one typical power inductor employed on Apollo3/4 Blue EVB board and its saturation current exceeds 800mA a lot when the inductance decreased by 20%[1].

Figure 4-8: Typical Inductance vs Current Curve of BLE Buck Inductor



[1] https://www.murata.com/en-us/products/productdetail?partno=DFE18SAN1R0ME0%23

Another point that needs to be noted is that the series 0-ohm resistor R4 placed between VDDBH and VDDBH_RF pins in Apollo4 Blue EVB (R29 between VDDBH and VDCDCRF pins in Apollo3 Blue EVB). It could be replaced with one ferrite bead if there are other standards RF components coexistence on the board to suppress the noise may couple into Bluetooth Low Energy buck power supply. The typical ferrite bead P/N that applied to EVB board is BLM15HG601SN1D who has below characteristics, and users may reference these parameters during component selection[1].

Table 4-4: Reference Ferrite Bead Characteristics

Part Number	Impedance (Ω)		Rated Current (mA)	DC Resistance (Ω max)
	@100 MHz	@1 GHz		
BLM15HG601SN1D	600 ± 25%	1000 ± 40%	300	0.7

[1] https://www.murata.com/en-global/products/productdetail?partno=BLM15HG601SN1%23

SECTION

5

RF PCB Layout Guide

5.1 PCB layout considerations

There are many factors need to be considered before starting RF PCB layout in end applications, includes but not limited to:

- Form factors
- Stack layer structure
- Circuit function
- Voltage and current
- Operating frequency band
- Impedance control and matching
- Signal integrity and reliability
- Shielding and isolation
- EMC and ESD protection
- Heat dissipation
- …

This will involve a lot of content to list all kinds of considerations if expanded. Thus, the present chapter will only provide some general guidelines from the view of RF trace layout itself in Apollo Bluetooth Low Energy SoC based board layout. The basic layout rules are listed as follows:

1. The first rule of PCB layout is to make RF traces as short as possible. Long traces alter the matching network and then the suggested component values are no longer valid. Suggested LC values may vary due to PCB parasitic parameters. A PCB trace 100 mills (2.54mm) long will introduce about 1.1 nH inductance.
2. Make individual ground connections to the ground plane with a via for each ground connection. Do not share vias with ground connections. Each ground connection equals one or more vias. The ground plane must be solid and if possible, without interruptions. Avoid putting the ground plane on top next to

the matching elements. This normally adds additional stray capacitance which changes the matching state.

3. The RF path should be as straight as possible, avoiding loops and unnecessary turns. Separate ground and power supply traces from other circuits (digital signal chain, etc). Known sources of noise should be laid out as far as possible from the RF circuits. Avoid thick traces, the higher the frequency, the thinner the trace should be to minimize losses in the RF path.

   The RF traces are routed on the top layer; the immediate layers are ground and power planes.

The immediate ground plane ensures a minimum ground current return path. The non-RF traces are laid on the bottom layer to minimize interference between RF and non-RF components.

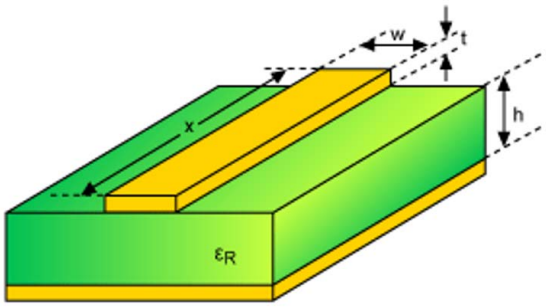
5.2 RF Transmission Lines

There are commonly three kinds of transmission lines oftenly employed in RF PCB design: microstrip, stripline and coplanar waveguide (CPW), and their respective characteristics are described as follows:

1. Microstrip

   Microstrip consists of fixed-width metal routing (the conductor), along with a solid unbroken ground plane located directly underneath (on the adjacent layer). For example, a microstrip on top layer 1 requires a solid ground plane on inner layer 2. The width of the routing, the thickness of the dielectric layer, and the type of dielectric determine the characteristic impedance (typically 50Ω).

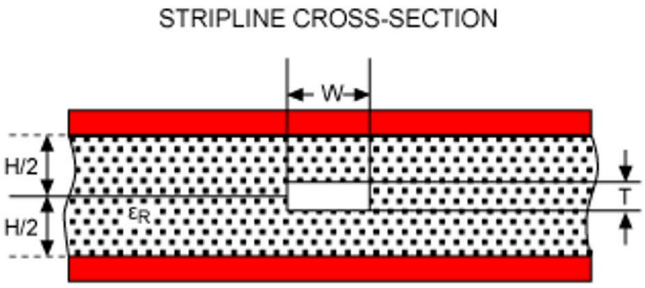
   Figure 5-1: Microstrip Structure



2. Stripline

   This line consists of a fixed-width routing on an inner layer, with solid ground planes above and below the center conductor. The conductor can be located midway between the ground planes, or it can be somewhat offset. Stripline is the appropriate method for RF routing on inner layers.

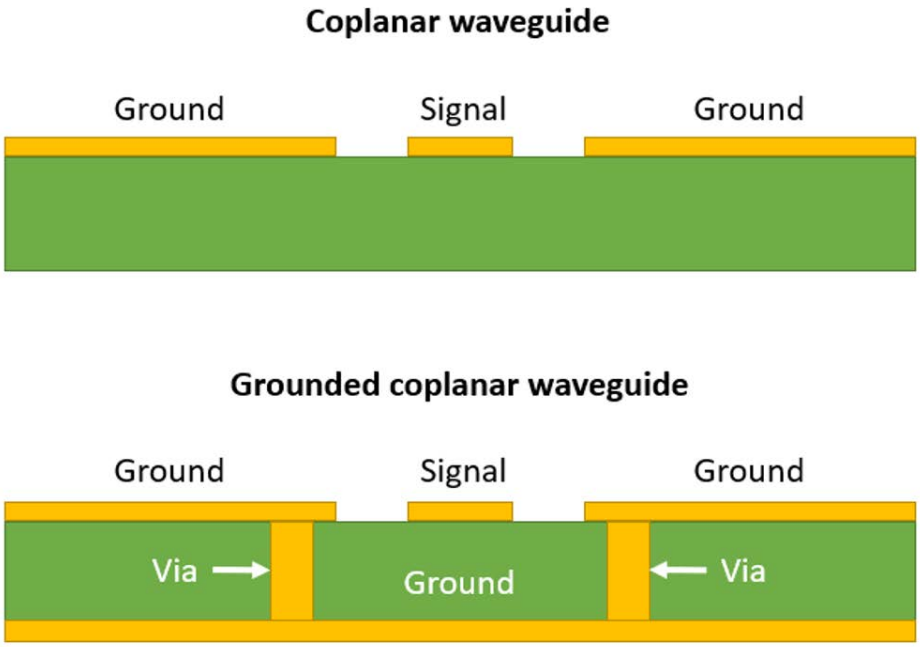
Figure 5-2: Stripline Structure



3. Coplanar Waveguide (CPWG)

A coplanar waveguide routing is a copper arrangement where RF signal trace is routed in parallel to two ground planes. The presence of the ground plane on each side of RF signal trace provides natural shielding for the signal against interference from other traces on a board. CPWG also comes in the grounded variety. The geometry is essentially the same, except there is another ground plane beneath the surface layer. CPWG provides for better isolation between nearby RF traces, as well as other signal traces. This medium consists of a center conductor with ground planes on either side and underlying layer. This is shown in the Figure 5-3 below.

Figure 5-3: Coplanar Waveguide Structure



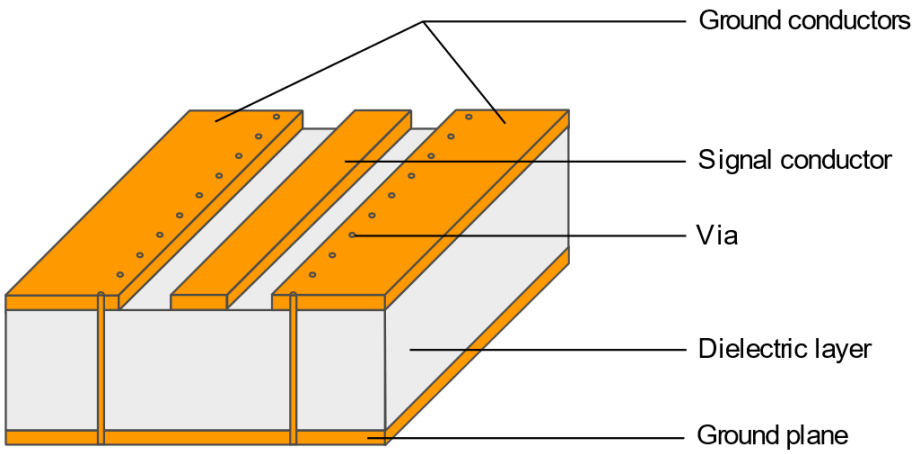
Compared to microstrip and stripline, CPWG structure places RF signal trace on the surface layer with the ground pour on each side of the trace causes a signal to see lower radiation losses. This also reduces resistive heating losses as the signal hugs the side of the trace, rather than hugging the bottom of the trace near the rough interface with the substrate. This means the signal will be stronger at the receiver

end of the trace, and the shape of the signals will not be distorted as they travel along the trace.

For 2.4GHz applications such as Bluetooth/Wi-Fi, it requires series and/or shunt components for impedance matching. Since CPWG has a nearby ground plane directly next to the RF trace, these shunt components can be mounted directly between the trace and the ground plane without placing them through vias. Therefore, the CPWG RF trace structure is most appropriate for Bluetooth Low Energy based products' PCB layout.

Fence vias are recommended placing on both sides of a coplanar waveguide, as shown in Figure 5-4. This stereoscopic view provides an example of a row of ground vias on each top metal ground plane on either side of the center RF signal trace. Return currents induced on the top layer are shorted to the underlying ground plane with shortest path.

Figure 5-4: A Grounded Coplanar Waveguide (GCPW) with Fence Vias



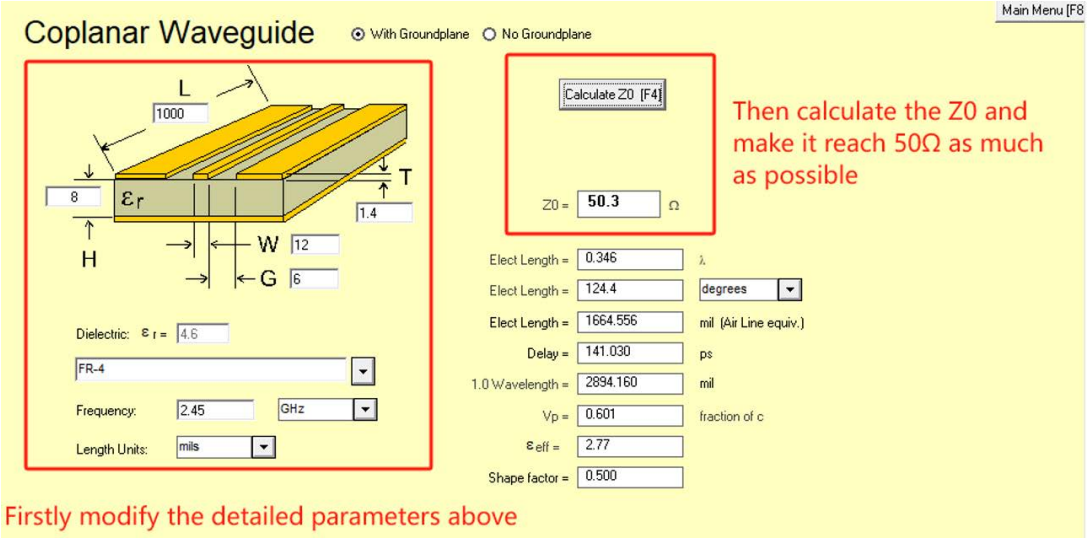
5.3 50-ohm Impedance Control

Since coplanar waveguide structure was most applicable for a user'swireless product hardware design, it is used as an example to illustrate how to figure out various PCB design parameters such as the RF trace width and thickness, the gap between RF trace and its surface nearby ground plane, and the thickness of specific dielectric layer, and more.

There are many easy-to-use RF circuit design tools and transmission line calculators available which can be utilized to calculate PCB layout parameters to achieve desired characteristic impedance Z_0 and hereunder Avago's AppCAD tool (now Broadcom) is employed as example for illustrating how to use it. The following Figure 5-5 on page 27 shows its graphical user interface after opening CPWG calculator function[1].

[1] https://www.broadcom.com/info/wireless/appcad

Figure 5-5: The CPWG Calculation by Using AppCAD Tool



As the window shown above, the user need to fill various PCB layout related parameters marked in left red box according to real PCB layout and layer stack requirement, which include the operating frequency, dielectric constant ε_R, dielectric thickness *H*, trace width *W*, trace thickness *T*, the gap between trace and nearby ground plane *G*, and more. All these design parameters will affect the final calculation of Z_0 marked in top right red box (note that the trace length *L* is basically irrelevant to Z_0 calculation so it can be ignored).

However, the user should be cautious when filling the dielectric constant ε_R of the inner layers. The outer laminated layers of typical PCB often contain less glass content than the core of the board, and consequently the dielectric constant will be lower than its intrinsic value. For example, FR4 core is generally given as ε_R=4.2 or 4.6, whereas the outer laminate (pre-preg) layers are typically ε_R=3.8. Examples are given in below Table 5-1 for reference only, trace thickness assumed for 1-oz copper (1.4 mils, 35µm).

Table 5-1: Example of Modified Z_0 Calculation

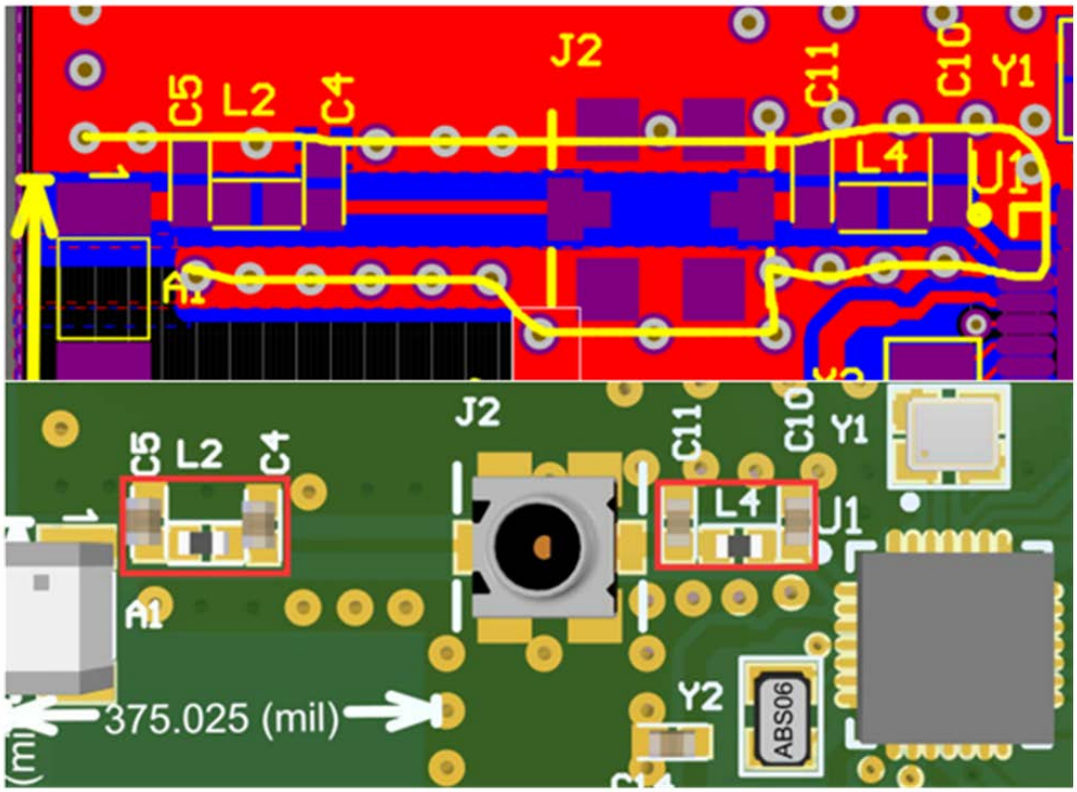
TX Line	Dielectric	Layer Thickness (mils)	Trace Width (mils)	Gap (mils)	Calculated Z_0 (Ω)
Microstrip	Prepreg (ε_R=3.8)	6	11.5	N/A	50.3
		10	20		50.0
Stripline	FR4 (ε_R=4.5)	12	3.7	N/A	50.0
CPW	Prepreg (ε_R=3.8)	6	14	20	49.7

As a result, the user can finally figure out the modified trace width, gap and dielectric thickness that can achieve approximate 50Ω pure resistance impedance by

adjusting their combinations. Then PCB manufacturer will follow this information and adjust the PCB stack layer structure to meet characteristic impedance Z_0 requirement. Sometimes PCB designers need to coordinate with PCB manufacturer to slightly modify some layout parameters due to the PCB materials limit.

The following Figure 5-6 shows an actual RF front-end PCB layout case, the RF trace routed from chip terminal and went straight to ceramic antenna feed point, ground via strips connected to bottom reference ground plane were evenly distributed on both sides of RF trace. Two Π-type matching networks were placed close to RF chip and antenna respectively.

Figure 5-6: RF Front-end PCB Layout Example



SECTION

6

Summary

This document describes how to implement reasonable RF hardware design based on Apollo Blue series SoC from radio concepts and theory, RF front-end and power supply schematic, and RF PCB layout considerations, and more. It also gives references and instructions for component selection used where their characteristics need to be treated carefully. It is strongly recommended that users refer to this guide to design RF related portion in their Apollo Blue SoC based products as much as possible.

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