DESIGN GUIDE

Apollo Bluetooth Low Energy SoC RF Impedance Matching

Ultra-Low Power Apollo SoC Family

A-SOCAPG-DGGA01EN v1.0

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Revision History

Revision	Date	Description
1.0	May 2, 2024	Initial release

Reference Documents

These reference documents can be accessed on the Ambiq Website and/or Content Portal.

Document ID	Description

*Indicates to use the latest version of the document.

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1

Introduction

Impedance matching can be defined as an impedance transformation that converts a practical complex impedance to another nominal impedance value, mostly defined as pure resistance of 50Ω in RF and Microwave applications. The impedance matching is very important for radio systems to achieve optimum RF performance that does not only minimize signal reflection and maximize power transfer but can also suppress harmonics and improve the SNR of whole systems. This design guide describes how to design matching circuits and perform impedance matching for Apollo Blue series BLE SoCs by using Smith Chart and vector network analyzer.

SECTION

2

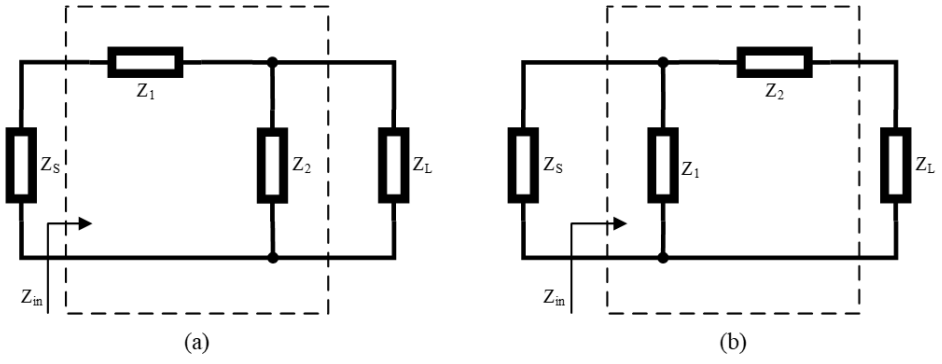
Matching Network

There are many ways in which impedance matching can be implemented in RF and microwave circuits, such as lumped LC matching networks, distributed microstrip line matching networks and hybrid LC and microstrip line type. The following sections will mainly introduce the discrete components impedance matching network topology and methods that is oftenly used in 2.4GHz Bluetooth-capable devices.

2.1 2-Element Matching Network

2-element matching network is the simplest matching topology and can be easily incorporated into RF circuits for impedance matching. As the element arrangement, the matching components are oriented in series and shunt connections such that they will form an 'L' shape, either inverted L-section networks or reverse L-section networks. These networks only use two reactive components (Z_1, Z_2) to transform the load impedance (Z_L) to the desired input impedance (Zin). Low insertion loss is the major advantage that keeps the L-type network superior to other types. The following Figure 2-1 shows their two topologies composed of one series component and another shunt component where they can be placed as capacitors or inductors.

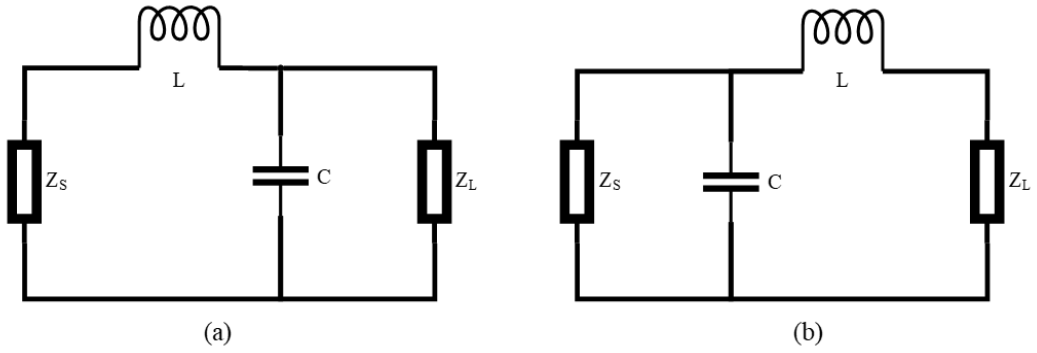
Figure 2-1: 2-Element LC Matching Networks Topology



Where, Z_S and Z_L in the above figure depict source and load impedance respectively. The input impedance Zin mentioned above needs to be equal to Z_S if the source impedance is expressed as pure resistance or the complex conjugate of Z_S if the source impedance is expressed as complex impedance.

There are eight possible configurations of L-sections based on different L and C combinations in the position of Z_1 and Z_2 above, and the frequency response of these networks can be classified as either low-pass, high-pass, or bandpass filters. The low-pass solutions are the most widely used L-sections in real designs since they can filter unwanted harmonics, noise, and other interferences except impedance matching itself. The following Figure 2-2 shows the two versions of low-pass circuits where inductor placed in series and capacitor placed in parallel connection.

Figure 2-2: Low-pass Matching Circuit Versions for L-Sections



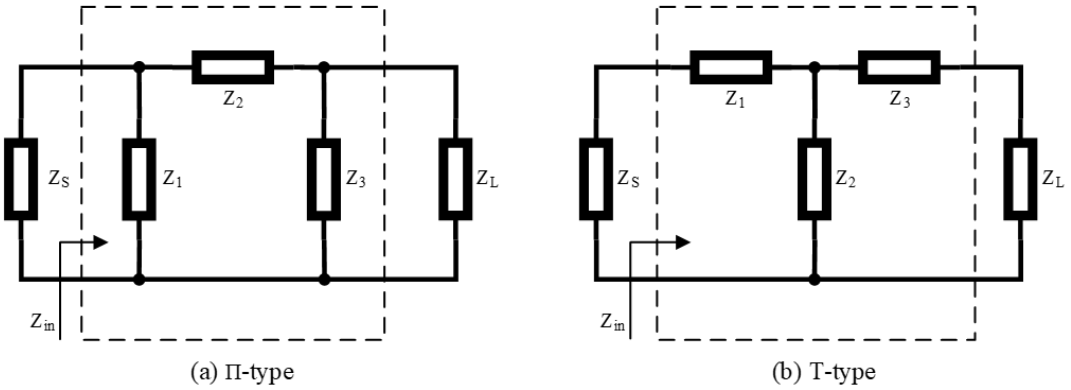
2.2 3-Element Matching Network

In RF designs, the *Q* (quality factor) defines the bandwidth of the matching network, i.e., the passband width of the filter constructed by matching circuits. Unfortunately, the *Q* of L-type matching network was fixed and only determined by the selected *L* or *C* that are being matched, which can not be chosen or changed flexibly. To gain the freedom of choosing the *Q* and thus affect the bandwidth of the circuit, a third element needs to be introduced in the matching network.

3-element LC matching networks provide more flexibility in choosing the network *Q*, which is much greater than that achieved with 2-element L-type matching networks. As shown in Figure 2-3 on page 9, there are two types of 3-element LC matching networks based on components arrangement.

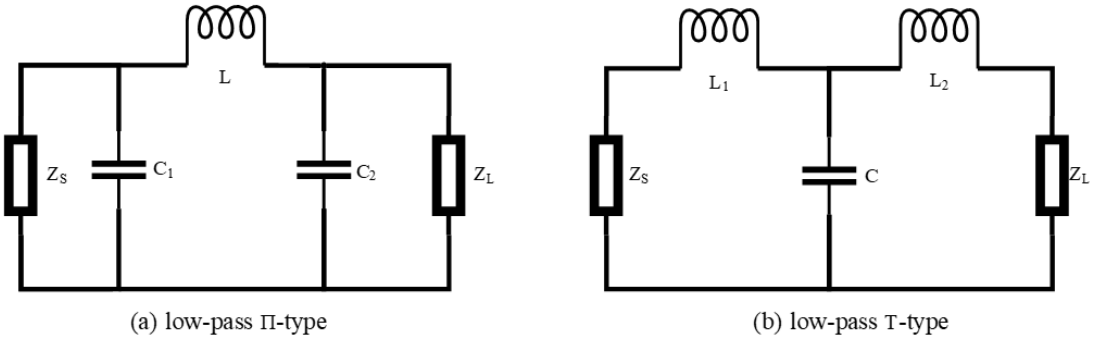
1. Π-type matching networks, consist of two shunt elements and one series element and they are arranged in the form of the Greek alphabet Π.
2. T-type matching networks, consist of two series elements and one shunt element and they are oriented in the form of the uppercase letter T.

Figure 2-3: 3-Element LC Matching Networks Topology



There are also eight configurations for Π-type and T-type matching network each respectively. Similarly, the low-pass circuits of the two types are the most widely used configurations in practical applications due to those additional benefits they will bring. Thus, the inductors will be placed in series connections and the capacitors will be placed in parallel connections as shown in the following Figure 2-4.

Figure 2-4: Low-pass Configurations for 3-Element Matching Network



2.3 4 or More Elements Matching Network

When RF applications demand high TX output power levels like above +10 dBm or more, as well as provide strong harmonic suppression capability, the four or more elements will be chosen to construct matching network. Generally, the multi-elements matching network can be regarded as the cascaded L-type network or the combination of L-sections and Π-type or T-type network. The more LC matching elements the higher filter's order, so they can give good out-of-band emissions and harmonic suppression. However, the side effect or trade-off of multi-elements matching network is to introduce higher insertion loss in passband as well as the impedance matching and tuning process becomes more complex. Thus, this will not be discussed in this case here since they are rarely used in Bluetooth-based applications.

SECTION

3

Smith Chart Basics

For designing an appropriate *LC* matching network, it will usually have two broad approaches: calculate and derive the matching components value mathematically; or use the Smith Chart as a graphical design tool. The mathematical approach is the traditional method which can yield precise results but needs very complicated math operations even for simple L-sections. Alternatively, the Smith Chart approach is more intuitive, easier to verify and faster to get results for matching circuits design since it does not need complicated computations.

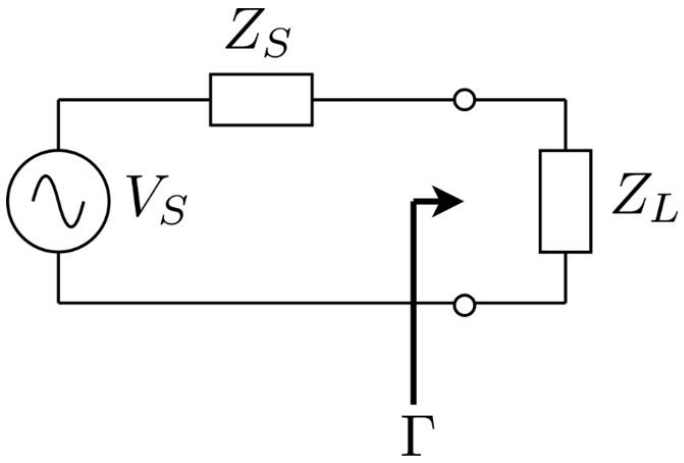
Thus, basically the Smith Chart for rapid and relatively precise designs of the matching circuits nowadays are used. The appeal of Smith Chart is that its complexity remains almost the same independent of the number of components in the matching network. Moreover, by observing the impedance transformation on the Smith Chart one can see how the individual circuit elements contribute to achieving a particular matching condition. Any errors in component selection and value assignment are observed immediately and the RF engineers can directly intervene. With the help of CAD tools, the parameter choice (*L* or *C*) and its value assignment can be instantaneously displayed in the Smith Chart tools[1].

3.1 Reflection Coefficient

In radio systems and transmission line theory, the reflection coefficient is used to calculate how much of the electromagnetic wave is reflected by an impedance discontinuity in the transmission line. It is equal to the ratio of the amplitude of the reflected wave to the incident wave. The following Figure 3-1 on page 11 shows a signal source with internal impedance Z_S followed by a transmission line of characteristic impedance Z_0 is driving the load with impedance Z_L[2].

[1] https://drive.google.com/file/d/1KytkPX0f7uzMQYm7cPSlLfMTxwpmwpw7/view?pli=1iew?usp=sharing&pli=1
[2] https://en.wikipedia.org/wiki/Reflection_coefficient

Figure 3-1: Simple Circuit Diagram of Reflected Coefficient



The reflection coefficient Γ is determined by the load impedance at the end of the line and the characteristic impedance of the line. As is shown in Figure 3-1, a load impedance of Z_L terminating a transmission line with a characteristic impedance of Z_0 will have a reflection coefficient of

$$\Gamma = \frac{V^-}{V^+} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

where:

- V^+ is the voltage of the incident wave.
- V^- is the voltage of the reflected wave.
- Z_L is the load impedance.
- Z_0 is the characteristic impedance, oftenly 50Ω in radio systems.

3.2 Standing Wave Ratio

The standing wave ratio (SWR) is defined as the ratio of the maximum voltage (or current) over the minimum voltage (or current) and will be determined solely by the magnitude of the reflection coefficient Γ[3].

$$\mathrm{SWR} = \frac{|V_{max}|}{|V_{min}|} = \frac{|I_{max}|}{|I_{min}|} = \frac{1 + |\Gamma|}{1 - |\Gamma|}$$

The above calculation assumes that Γ has been calculated using Z_0 as the characteristic impedance. Since it uses only the magnitude of Γ, the SWR intentionally ignores the specific value of the load impedance Z_L responsible for it, but only the magnitude of the resulting impedance mismatch. That SWR remains the same

[3] https://en.wikipedia.org/wiki/Reflection_coefficient

wherever measured along a transmission line (looking towards the load) since the addition of a transmission line length to a load Z_L only changes the phase, not magnitude of Γ. While having a one-to-one correspondence with Γ, SWR is the most commonly used figure of merit in describing the mismatch affecting a radio antenna or antenna system. It is most often measured at the transmitter side of a transmission line, but having, as explained, the same value as would be measured at the load itself.

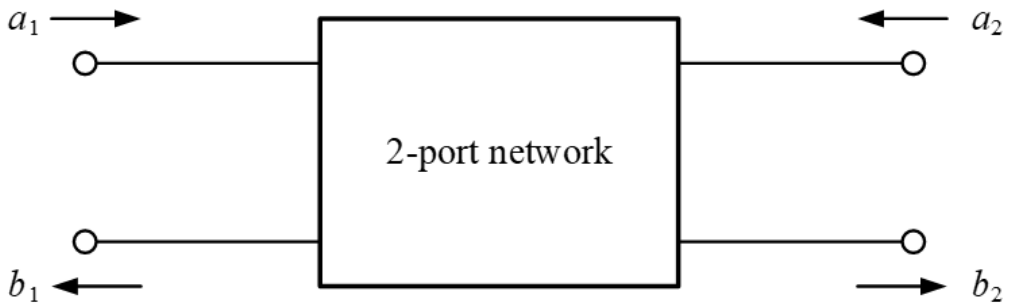
The SWR has a range of $1 \leq SWR < +\infty$. In most cases the term VSWR (voltage voltage standing wave ratio) is used, instead of SWR by defining it as the ratio of the maximum absolute voltage to its minimum. The ideal case of matched termination yields an VSWR of 1, whereas the worst case of either open or short-circuit termination results in VSWR $\dashrightarrow \infty$.

Strictly speaking, SWR can only be applied to loss-free transmission lines since it's impossible to define a SWR for lossy transmission lines. This is because the magnitude of the voltage or current waves decreases as a function of distance due to attenuation. But an approximate analysis can be made by using SWR for most low-loss RF systems especially for antennas.

3.3 S-Parameters

The S-parameter ('S' represents scattering) plays a very important role in radio systems. With the S-parameters, characterize all RF devices in the n-port network without requiring unachievable terminal conditions. The S-parameters are power wave descriptors that permit us to define the input-output relations of a two-port network in terms of incident and reflected power waves. As is shown in Figure 3-2, the incident normalized power waves are defined as a_n and reflected normalized power waves as b_n for a 2-port network, where the index n refers either to port number 1 or 2[4].

Figure 3-2: Definition of S-Parameters for a 2-Port Network



Based on the directional convention shown in above figure, define the S-parameters as follows by using one simple matrix multiplication:

[4] https://en.wikipedia.org/wiki/Scattering_parameters

$$\begin{Bmatrix} b_1 \\ b_2 \end{Bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{Bmatrix} a_1 \\ a_2 \end{Bmatrix}$$

where the terms are

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \equiv \frac{reflected\ power\ wave\ at\ port\ 1}{incident\ power\ wave\ at\ port\ 1}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \equiv \frac{transmitted\ power\ wave\ at\ port\ 2}{incident\ power\ wave\ at\ port\ 1}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \equiv \frac{reflected\ power\ wave\ at\ port\ 2}{incident\ power\ wave\ at\ port\ 2}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \equiv \frac{transmitted\ power\ wave\ at\ port\ 1}{incident\ power\ wave\ at\ port\ 2}$$

Note that the conditions $a_2 = 0$ and $a_1 = 0$ imply that no power waves are returned to the network at either port 2 or port 1. However, these conditions can only be ensured when the output or input port is matched into the characteristic impedances Z_0.

Thus, derive the physical meanings of S-parameters based on their expressions above. The S_{11} equals to the input reflection coefficient at port 1 under properly matched output conditions at port 2 and can be expressed as

$$S_{11} = \Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}$$

The VSWR at port 1 can also be rewritten as follows in terms of S_{11}:

$$VSWR = \frac{1 + |S_{11}|}{1 - |S_{11}|}$$

In engineering, use return loss to express the power mismatch of port and the return loss in dB at port 1 can be expressed by the logarithm of the magnitude of S_{11}

$$RL(dB) = 10\log|S_{11}|^2 = 20\log|S_{11}|$$

Similarly, the S_{22} depicts the output reflection coefficient and power mismatch at port 2 under properly matched input conditions at port 1.

The physical meaning of S_{21} is the forward transmission gain (from port 1 to port 2), while S_{12} is the reverse transmission gain or reverse isolation (from port 2 to port 1). For passive LC matching networks, the S_{21} refers to the insertion loss of matching network itself. Besides, S_{12} is usually used to indicate isolation of two ports and often appears in RF devices such as isolators, circulators, and duplexers, and more.

3.4 Smith Chart

As shown and marked in Figure 3-3, the Smith Chart can be used to simultaneously display multiple parameters including impedances *Z*, admittances *Y*, reflection coefficient Γ, VSWR, quality factors *Q*, and more. The most commonly used normalization impedance is 50 ohms.

There are two circles frequently used in impedance matching process:

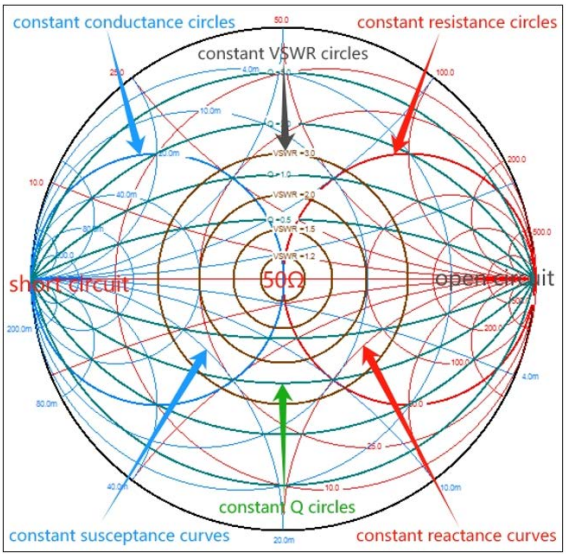
1. Constant resistance circle with $z = 1$, where $z = Z/Z_0$ means normalized impedance
2. Constant conductance circle with $y = 1$, where $y = 1/z$ means normalized admittance

Besides, three important points on the Smith Chart need to be taken care:

1. Open circuit with Γ=1, $z \dashrightarrow \infty$, located at the rightmost point on the real axis.
2. Short circuit with Γ= -1, $z = 0$, located at the leftmost point on the real axis.
3. The center origin with Γ=0, $z = 1$, located at the center of the Smith Chart.

The upper half of the Smith Chart is inductive since it corresponds to the positive imaginary part of the impedance. While the lower half is capacitive as it corresponds to the negative imaginary part of the impedance.

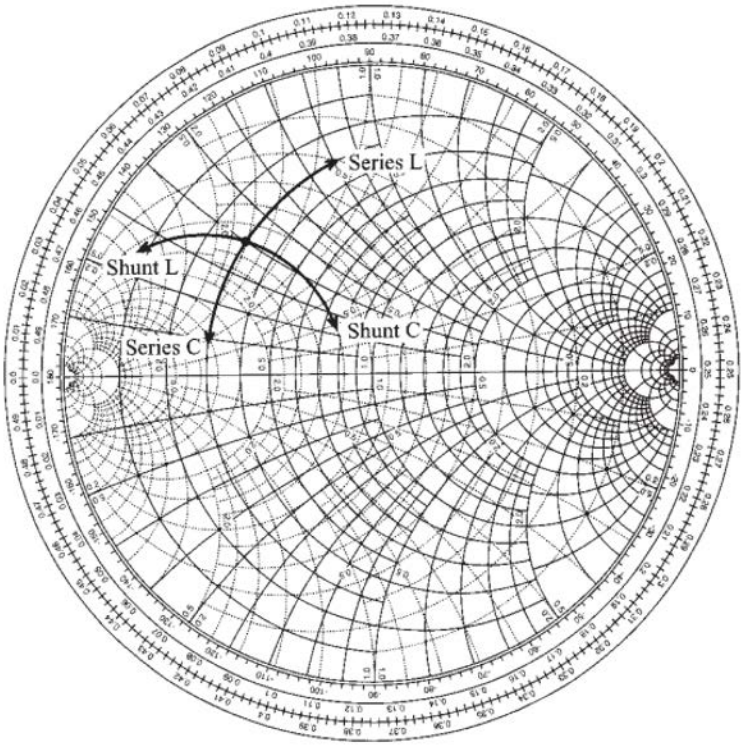
Figure 3-3: Combined Smith Chart with Impedance and Admittance



The movement path of series or shunt reactance components in the ZY Smith chart are provided as shown in Figure 3 4: the series connection of reactance elements will result in motion along a constant resistance circle and the shunt connection of reactance elements will produce motion along a constant conductance circle. More specifically, the general rules can be concluded as the following four sentences:

- The series inductor L moves clockwise along the constant resistance circle.
- The series capacitor C moves counterclockwise along the constant resistance circle.
- The shunt inductor L moves counterclockwise along the constant conductor circle.
- The shunt capacitor C moves clockwise along the constant conductance circle.

Figure 3-4: Impedance Variation of Series and Shunt L or C on Smith Chart



Having established the effect of connecting a single L or C component to the load, develop suitable multi-elements matching networks that perform the transformation from any load impedance to any specified input impedance. In general, designing an L-type or Π-type or T-type matching network in the ZY Smith Chart consists of moving along either constant resistance circles or constant conductance circles[5,6].

[5] https://en.wikipedia.org/wiki/Smith_chart
[6] https://drive.google.com/file/d/1KytkPX0f7uzMQYm7cPSlLfMTxwpmwpw7/view?pli=1iew?usp=sharing&pli=1

SECTION

4

Impedance Matching Procedures

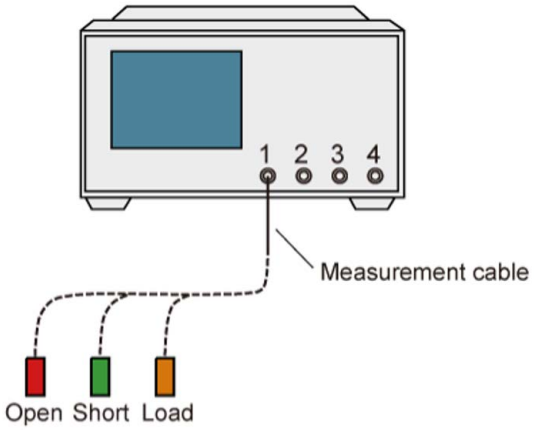
This section will introduce how to design an appropriate matching network and tune it to 50Ω for Apollo Blue series Bluetooth Low Energy SoC. Generally, the whole matching and tuning process consists of the following basic steps:

1. Perform calibration of network analyzer.
2. Measure the raw output impedance for on-board RFIC.
3. Plot the original impedance on the Smith Chart tools and creating the initial matching design with ideal, lossless LC components.
4. Place practical components on board and use VNA to verify simulation results and adjusting the LC component value repeatedly.
5. Conduct RF testing by using signal analyzer or Bluetooth tester.

4.1 Calibration of Network Analyzer

Calibration a.k.a system error correction is the process of eliminating systematic, reproducible errors from the measurement results. For example, as shown in Figure 4-1, the measurement cable between the analyzer ports and the DUT will introduce a magnitude attenuation and a phase shift of the EM waves. Both effects will affect the accuracy of the S-parameters measurement.

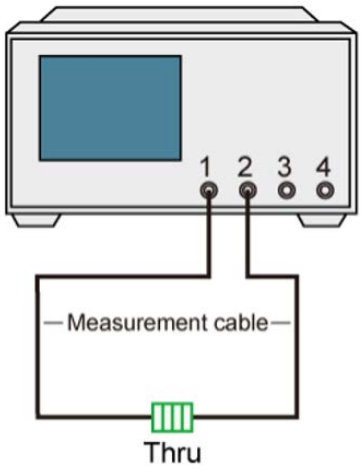
Figure 4-1: Port Calibration Test Setup of Network Analyzer



Thus, use the calibration kit to calibrate the measurement cable, in other words, move the 50ohm reference plane from the test port of analyzer to the end of measurement cable that will be used to connect DUT. For 1-port calibration shown in Figure 4-1, measure the calibration data for the Open/Short/Load standard at the test port 1 respectively and these operations are called reflection S-parameters calibration.

For 2-port calibration, in addition to their separate reflection Open/Short/Load calibration there will be one more transmission S-parameters calibration that requires connecting the Thru standard between the two cables as shown in Figure 4-2.

Figure 4-2: Connecting Thru Standard for 2-Port Calibration



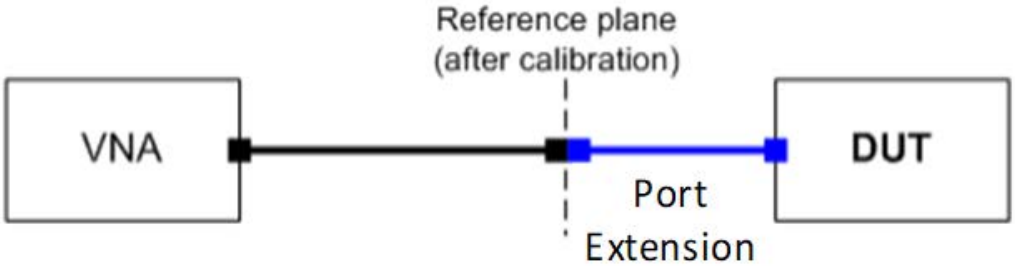
Besides, another important function called port extension will be oftenly used after calibration. Why port extension needed? That's because most of the network analyzer's calibration kits can only match some standard RF connectors like N-type or SMA type. However, in most cases the RF connectors and cables used in real design are possibly irregular and it's impossible to connect them with calibration kit directly. Figure 4-3 on page 18 shows the RF cable which is used on Apollo Blue

series EVB board, and it can not be connected to standard calibration kit, so in this case the port extension is required.

Figure 4-3: RF Cable Type Used by EVB

As shown in Figure 4-4, move the reference plane to the black cable end after calibration while there is another blue cable used to connect DUT, so port extension will be required to compensate the electrical delay and cable loss between the calibrated reference plane and the DUT.

Figure 4-4: Port Extension for Practical Applications



For the detailed calibration and port extension procedures, refer to specific user manual provided by corresponding network analyzer vendors. Further details will not be discussed here[7,8]

4.2 Determine Raw Output Impedance

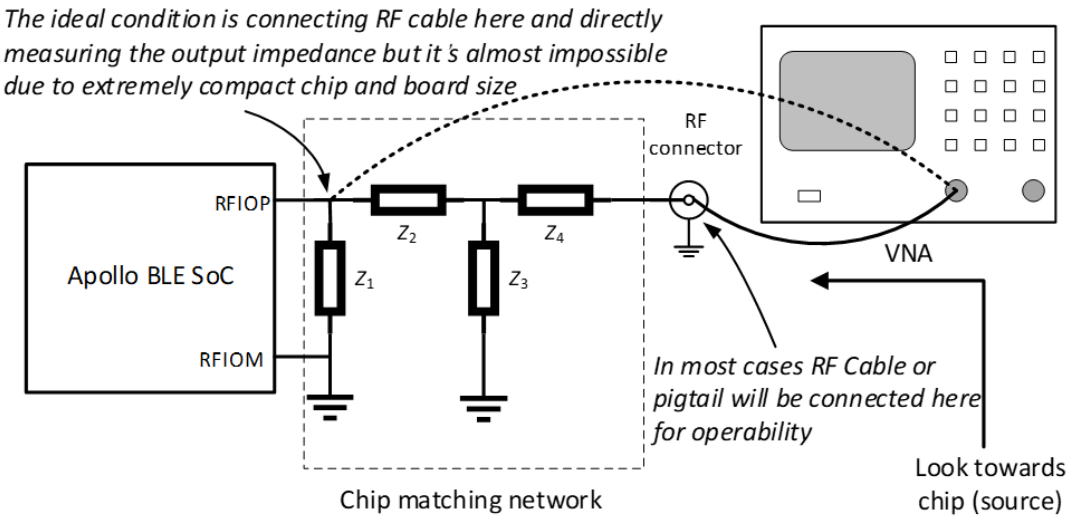
After calibration and port extension, measure the complex impedance and S-parameters of DUT by connecting its test port to network analyzer's port. Use Apollo4 Blue and its engineering board as example to illustrate how to measure, simulate and perform matching and tuning in this and subsequent sections.

As described in another technical doc *RF Hardware Design Guide for Apollo BLE SoC v1.0*, the recommended RF front-end circuit topology is shown as below Figure 4-5 on page 19, note the antenna matching circuit portion was removed here since

[7] https://www.keysight.com/us/en/lib/resources/help-files/help-file--user-manual-for-e5071c-ena-network-analyzer-operation-and-programming-1659862.html
[8] https://www.rohde-schwarz.com.cn/manual/r-s-znc-znd-manuals_78701-29339.html

designing chip matching circuits for RFIC itself hereinafter will only be discussed here.

Figure 4-5: Measuring Impedance Characteristic of DUT by Using VNA

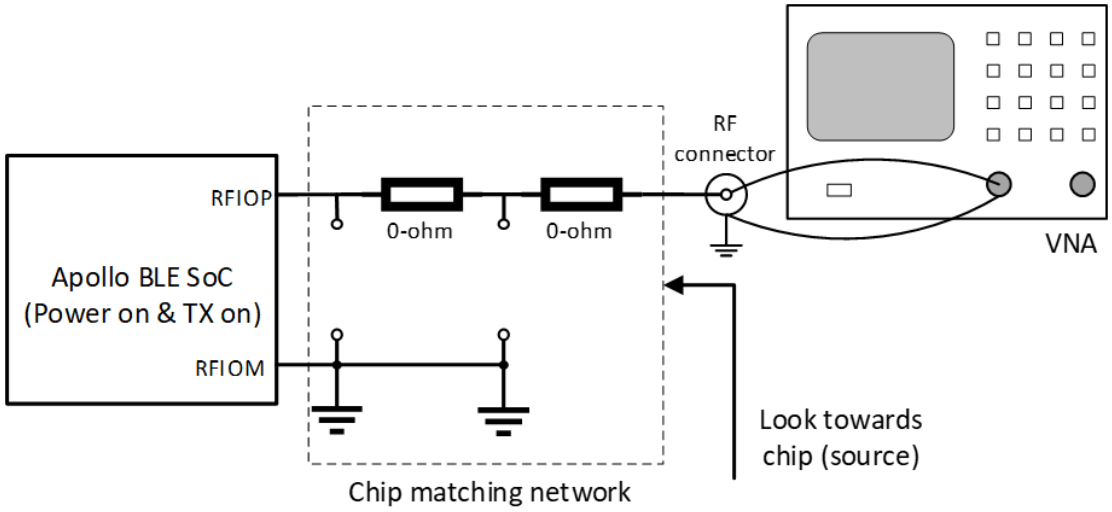


For measuring the raw output impedance of Apollo Blue series Bluetooth Low Energy SoC, power up DUT and set it to transmit mode at first. The transmit mode means all transmitter related modules inside DUT are powered on (e.g., the internal transmission path is turned on) and this can be easily configured by sending HCI commands under DTM mode.

As the RF front-end topology shown in Figure 4-5, two shunt components Z_1, Z_3 and two series components Z_2, Z_4 are used to design lumped LC matching network. The best place to measure the output impedance of RFIC is putting the measurement cable or soldering pigtail at the intersection of Z_1 and Z_2, since this will minimize the impact of board parasitic parameters and bring relatively precise measuring result. However, it's difficult to operate at the place closest to chip due to small component and board size. Thus, connect RF cable to the RF connector that locates between chip matching network and antenna matching network. Then keep the shunt elements Z_1 and Z_3 disconnected and replace series elements Z_2 and Z_4 with 0-ohm resistors. The matching circuit will become as shown in Figure 4-6 on page 20 after these operations.

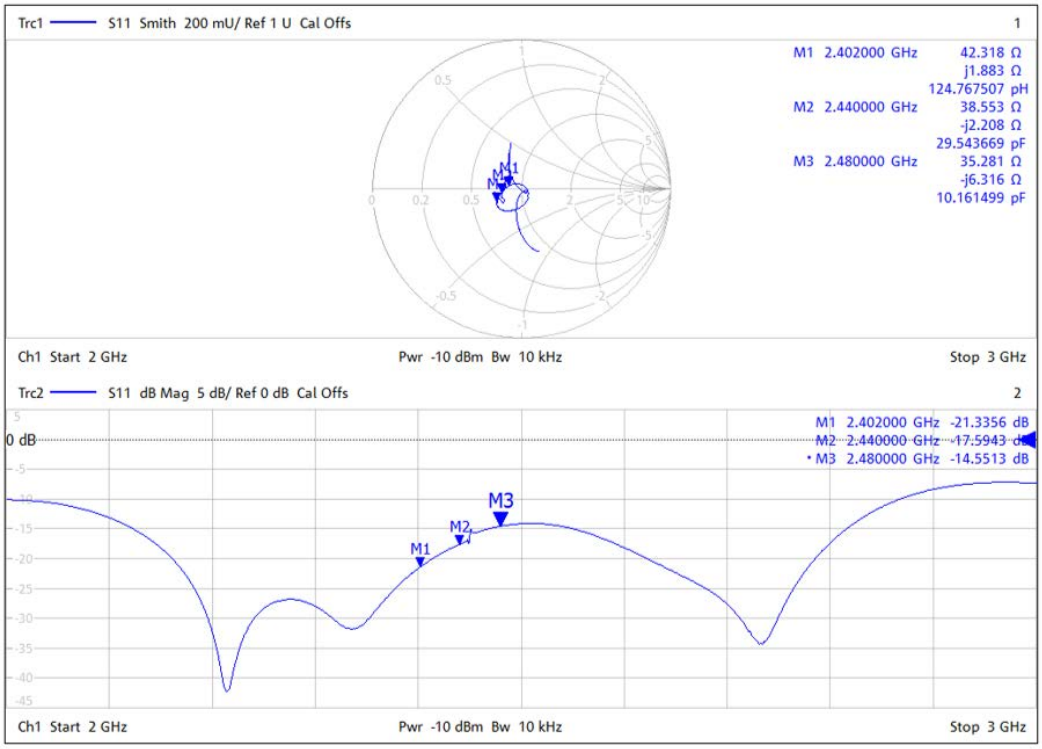
Next, perform 1-port reflection S-parameters calibration and port extension then connect the DUT to VNA by dedicated measurement cable.

Figure 4-6: Matching Circuit Config for Measuring the Output Impedance of DUT



It is recommended to set the sweep frequency range of network analyzer wider than operating frequency band 2402~2480 MHz, herein start from 2GHz and stop at 3GHz. Three markers shall be added representing the low 2.402GHz, mid 2.44GHz and high 2.48GHz respectively. As shown in Figure 4-7, two traces are selected to display impedance and S11-parameters in dB respectively. The measured complex output impedance and S11-parameters of them will be displayed on the VNA screen. Check and see that the raw output impedance of RFIC has already been relatively close to the center origin of Smith Chart, (e.g., 50Ω).

Figure 4-7: Impedance Measurement Results Displayed on Network Analyzer

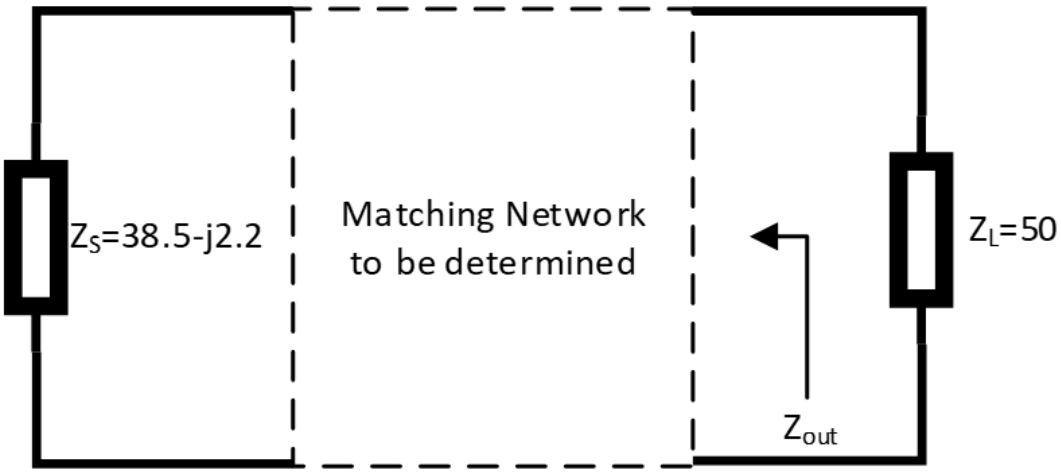


It should be noted that the PCB traces and the 0-ohm resistors themselves will bring parasitic effects both, so the output impedance of chip measured at the RF connector may slightly deviate from the actual situation (e.g., the impedance at RFIO terminal). These influencing factors will be taken into account during matching and tuning process afterwards.

4.3 Matching Design with Smith Chart

According to the actual measured values in above Figure 4-7 on page 20, simplify the RF front-end circuit and express it in the way of 2-port network as follows. The source impedance Z_S equals to the measured output impedance of Apollo4 Blue at center frequency 2.44GHz as well as the load impedance Z_L represents the 50Ω characteristic impedance (e.g., the input impedance of antenna matching network). Now, design one appropriate matching network so as to transform the source impedance Z_S to required load impedance Z_L. That means the output impedance Z_{out} towards RFIC after inserting matching network should be equal to 50Ω.

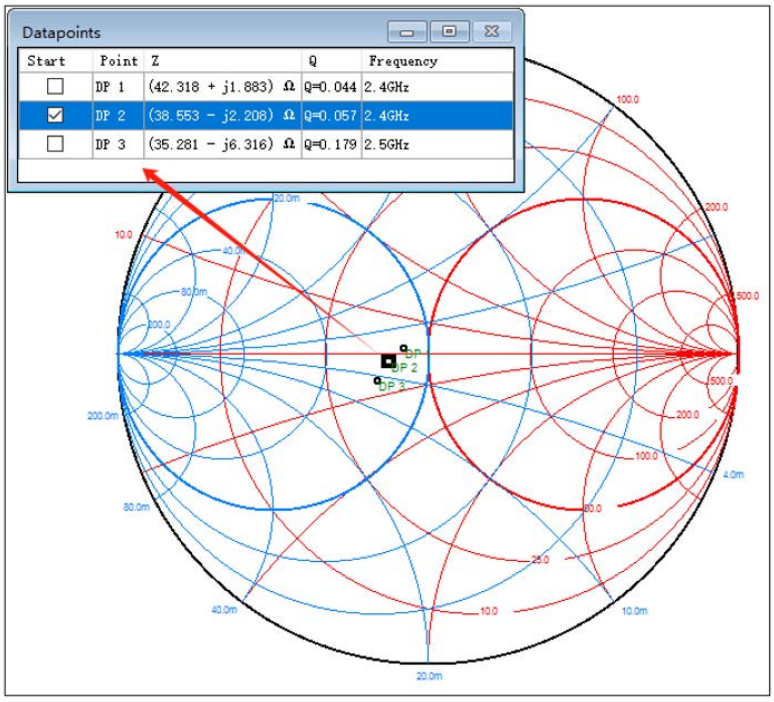
Figure 4-8: Simplified Circuit Expressed by 2-Port Network



Then mark the measured impedance values at low, mid, and high frequency as data points DP1, DP2 and DP3 on the Smith Chart as shown in Figure 4-9 on page 22. And the raw impedance at mid frequency 2.44GHz will be used to create matching network since the other two data points at low and high frequencies will move along with DP2 after matching elements added[9].

[9] http://www.fritz.dellsperger.net/smith.html

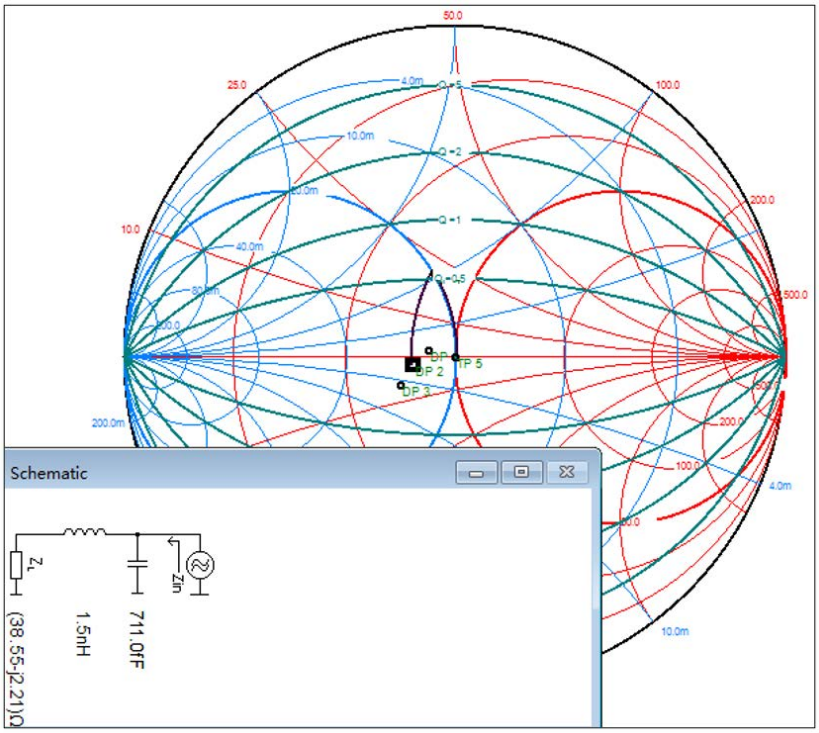
Figure 4-9: Measured Impedance Marked on Smith Chart



The matching circuit shows the source impedance Z_S=~38.5-*j*2.2 Ω at the input while it is terminated by 50 Ω antenna at the output. Reviewing the rotation direction of adding reactive components on Smith Chart, the two-element matching topology can be applied to create low-pass or high-pass matching solution for this case.

The low-pass matching solution composed of one series 1.5 nH inductor and one parallel 0.7 pF capacitor is shown in the following Figure 4-10 on page 23. The first series *L* will transform the data point move clockwise around the constant resistance circle and stop at the point TP4 that intersects with the constant conductance circle of y=1, then the second shunt C will transform the data point TP4 move clockwise along the *y=1* circle until it reaches the center origin TP5. The *L, C* component values are determined by these movements and displayed in the following schematic. Be aware that some calculated capacitance and inductance values are theoretical and may be not available in engineering (e.g., the 710 fF capacitor shown in below schematic), so the most approximative components will be applied to replace them in practice.

Figure 4-10: 2-Element Low-Pass Matching with Ideal LC Components



The Z_L marked in above schematic denotes the output impedance of RFIC as well as the Z_{in} denotes the matching impedance what is expected to achieve (e.g., 50-ohm). As mentioned in previous section, although the 2-element matching network is very simple to construct, the *Q* of network is constant and cannot be changed. As shown in Figure 4-10, the *Q* of this 2-element matching circuit can only achieve ~0.5 (constant *Q* contours also displayed in the Smith Chart), which means the low-pass matching circuit will have quite wide bandwidth and poor harmonic suppression.

Therefore, it is strongly recommended to use 3-element matching topology to improve the *Q* of matching network. The low-pass T-type and Π-type matching designs that applied to this example are illustrated on Smith Chart tool as shown in Figure 4-11 and Figure 4-12 on page 24 respectively. Two series inductors and one shunt capacitor are inserted in T-type matching network, while two shunt capacitors and one series inductor are inserted in Π-type matching network. As shown in the following two figures, the TP4 in T-type network and TP5 in Π-type network intersect with constant *Q* contour of *Q*=1, which denotes the designed network *Q* will be equal to 1.

Figure 4-11: T-Type Low-Pass Matching with Ideal LC Components

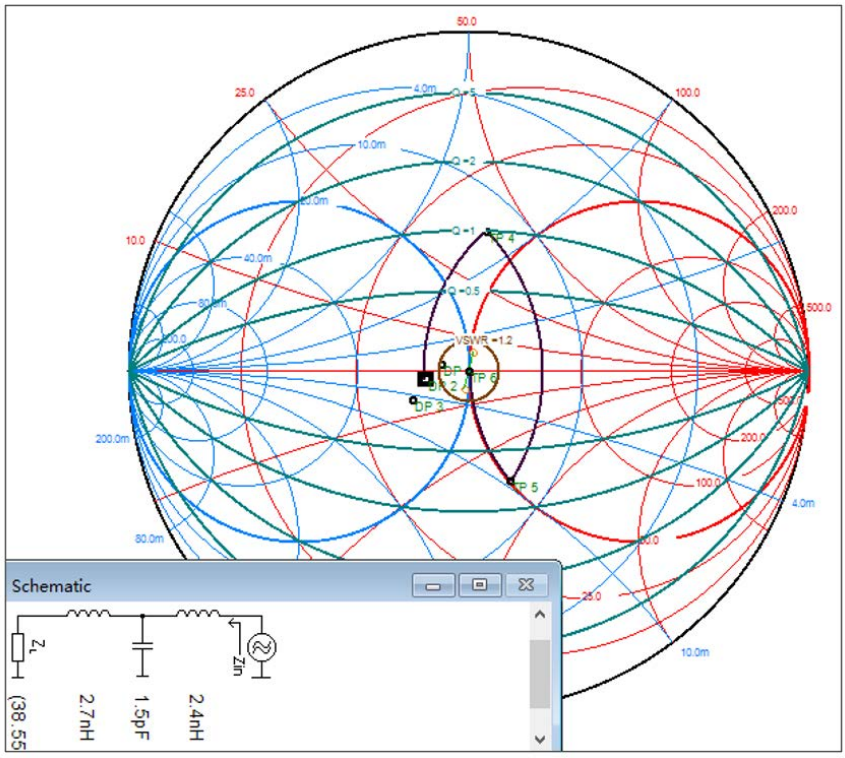
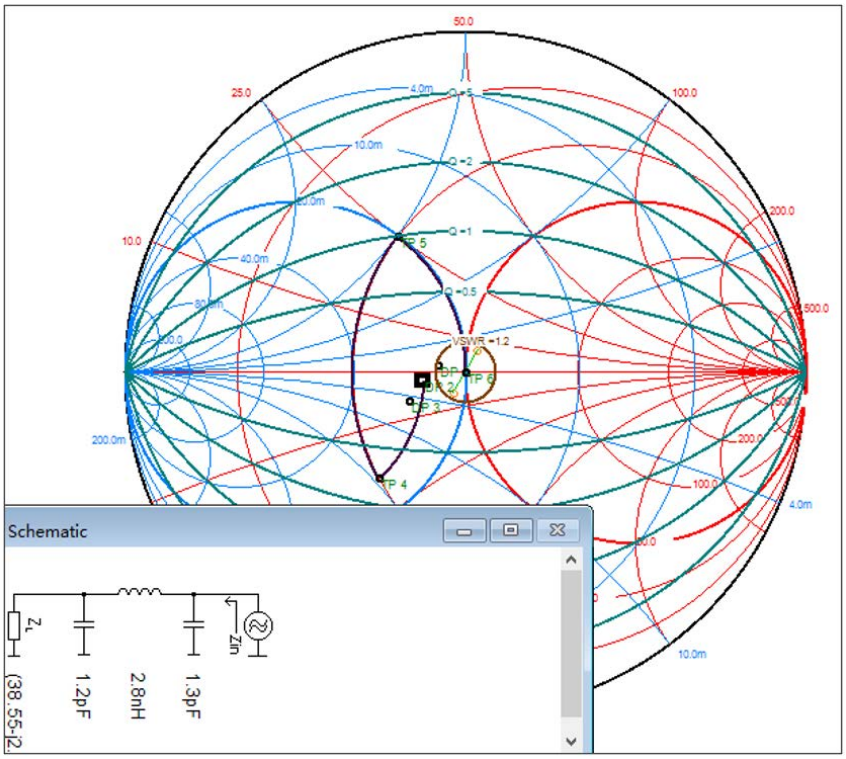


Figure 4-12: П-Type Low-Pass Matching with Ideal LC Components



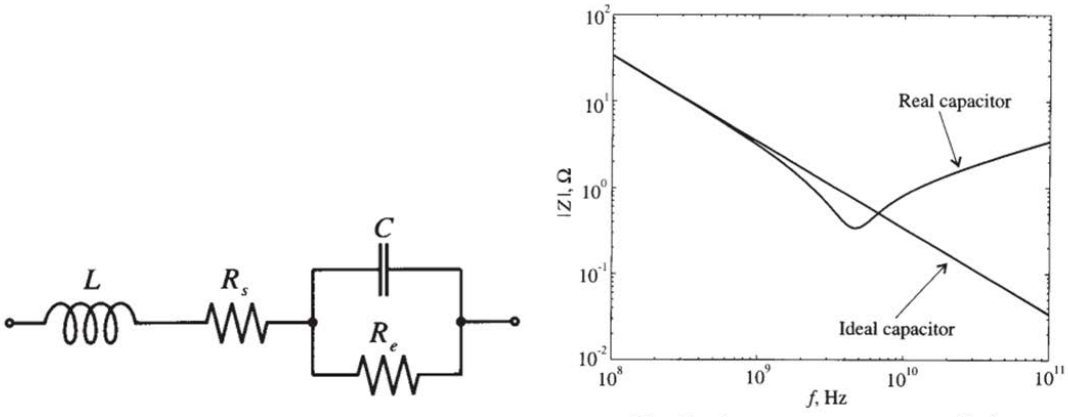
For Bluetooth capable devices, impedance matching is not performed for one single frequency but required for the entire operating frequency band from 2.4 GHz to 2.5GHz range. Thus, use the frequency sweep over data points function to check whether all three matched impedance points related to low, mid, and high frequency are converged and close enough to the center origin. In this example, open the display of constant VSWR circles on Smith Chart tool and find all the three matched impedance points fall within the VSWR=1.2 circle after frequency sweep, which indicates the designed matching network can also be applicable to broadband matching.

4.4 Verifying and Tuning by VNA

The theoretical matching network constructed by ideal passive components has been designed on the Smith Chart, now verify their real performance by using network analyzer. Why verification and tuning procedures necessary? One reason is that lots of simulated component values are not available in engineering, and they need to be replaced with approximate components; the other reason is the real situation may differ from the simulation result a lot due to parasitic parameters produced by non-ideal passive components themselves and PCB layout factors, even if passive components with the same values were used as what obtained from simulation.

As shown in Figure 4-13, in addition to its own capacitance C high-frequency capacitor's equivalent model consists of one parasitic lead inductance *L*, one series resistance R_S characterizing losses in the lead conductors, and one shunt resistance R_e characterizing dielectric loss. The impedance v.s. frequency response curve shows the impedance behaves approaching ideal capacitor only when the operating frequency is lower than one certain fixed value and it will exhibit the opposite characteristics when the operating frequency exceeds this point. The turning point is called Self-Resonant Frequency (SRF). The capacitor has a minimum magnitude of the impedance at its SRF.

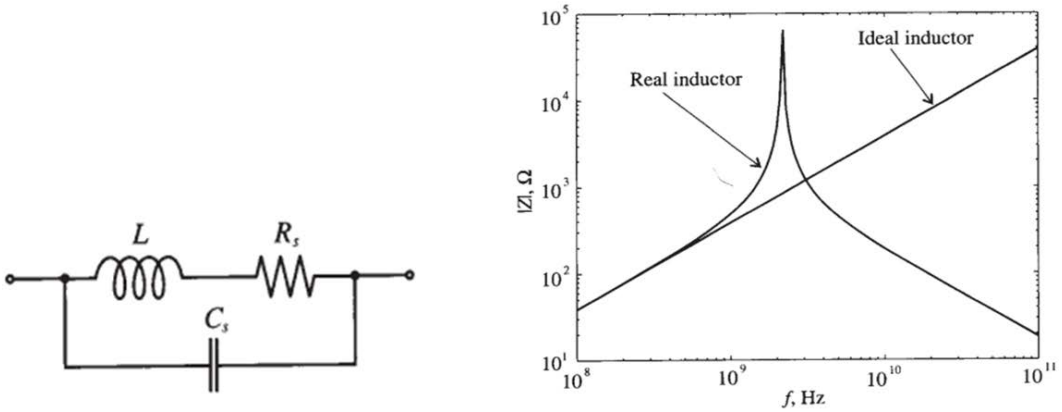
Figure 4-13: Equivalent Model and Frequency Response of Capacitor



(a) The equivalent circuit (b) The frequency response of |Z|

As shown in Figure 4-14, high-frequency inductor's equivalent model includes its own inductance *L*, the parasitic shunt capacitance C_s and series resistance R_s that represents composite effects of distributed capacitance C_d and resistance R_d, respectively. As can be seen from its impedance v.s. frequency response curve, the behavior of high-frequency inductor also deviates from the expected behavior of an ideal inductance at high frequencies. Firstly, the impedance of inductor increases or decreases more rapidly as the frequency approaches resonance on both sides. Secondly, as the frequency continues to increase, the influence of the parasitic capacitance C_s becomes dominant and the impedance of inductor decreases more slowly. The quality factor *Q* is commonly used to characterize the impact of the series resistance (e.g., the resistive loss of inductor or capacitor). For matching and tuning purpose, it's desirable that *Q* is required as high as possible, in other words the resistive loss would be as low as possible.

Figure 4-14: Equivalent Model and Frequency Response of Inductor



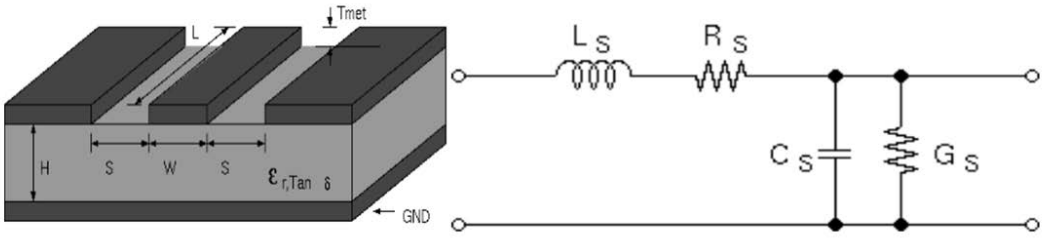
(a) The equivalent circuit (b) The frequency response of |Z|

Therefore, the characteristics of capacitance and inductance will gradually deteriorate as the operating frequency increases. They behave as inherent capacitance or inductance only when operating frequencies are far lower than their SRF, otherwise their impedance will exhibit opposite characteristics when the operating frequency goes beyond SRF. In other words, capacitor will show inductive as well as inductor will show capacitive while the operating frequency reaches up to greater than their SRF. Thus, take into account the impact of SRF and quality factor *Q* when selecting the specific passive components used for RF applications. For the selection guide of chip capacitors and inductors applicable to impedance matching, some tips are given in another application note *RF Hardware Design Guide for Apollo Bluetooth Low Energy SoC v1.0*.

In addition to the intrinsic parasitics of passive LC components, the PCB layout parasitics also have significant effects on impedance matching, including the series stray inductance of RF trace, and the parallel stray capacitance between RF trace and adjacent reference ground plane. These PCB layout parasitics usually result in the further decrease in values of the discrete low-pass LC matching elements (series inductance and parallel capacitance). It's difficult to obtain the accurate PCB parasitics and professional EM-based simulation tools may be required to use for

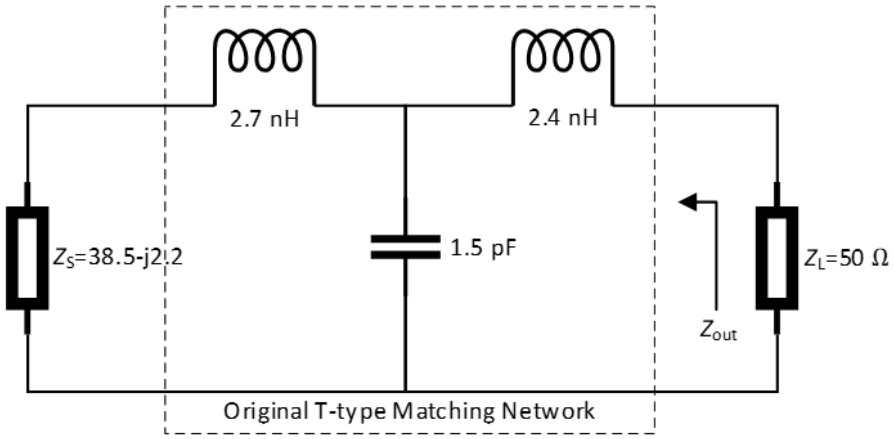
modeling. Thus, the estimation of PCB parasitics can be performed by using a coplanar waveguide calculator, which calculates the unit parallel capacitance and series inductance parasitics based on practical PCB design parameters. Figure 4-15 shows an example of this type of calculator. According to the detailed PCB layout parameters, the various parasitics such as stray inductance, stray capacitance, and more, can roughly be calculated[10].

Figure 4-15: Coplanar Waveguide Calculator Used for Calculating PCB Parasitics



As per the theoretical lumped elements derived from the movements around the Smith Chart in previous section, populate corresponding LC passive components onto PCB board and replot the simplified schematic of front-end matching circuit as shown in Figure 4-16. Hereunder use the T-type matching topology as an example, and connect it to network analyzer to verify if its behavior meets expectations.

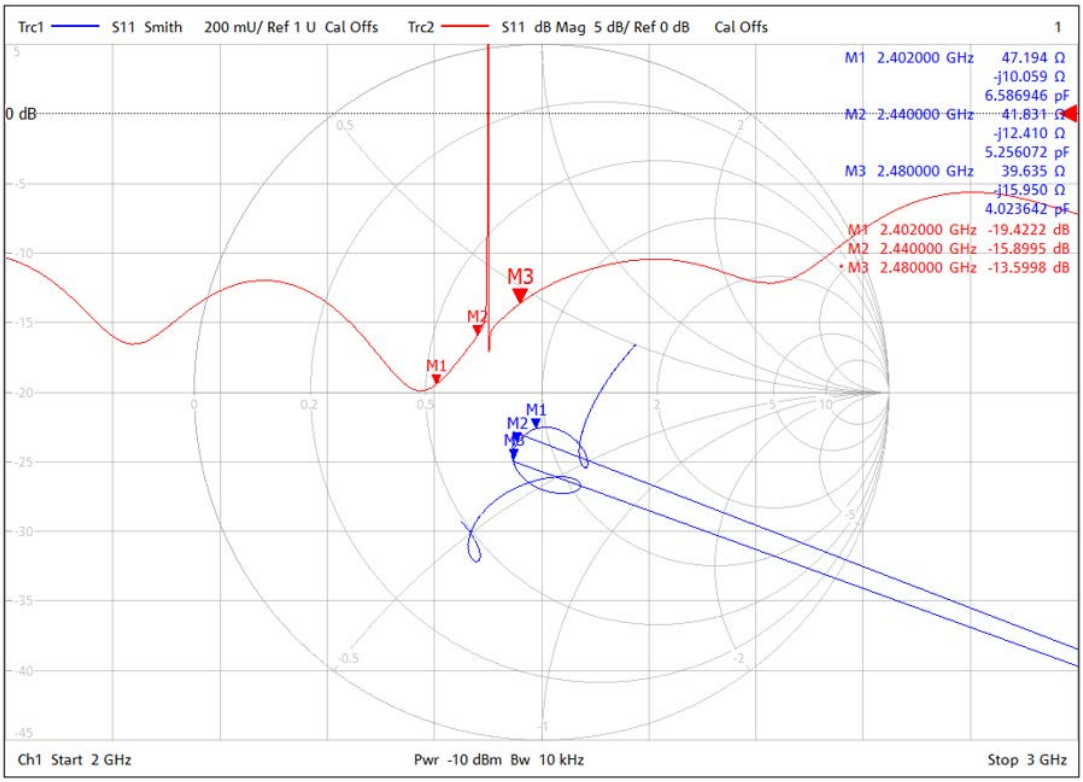
Figure 4-16: Simplified Schematic of T-Type Matching Circuit



The network analyzer here acts as one 50-ohm port and looks towards chip side to measures the output impedance Z_{out} of this T-type matching circuit. The measured impedance and S_{11} are shown in Figure 4-14 on page 26. It deviates from the ideal situation what simulation expected since the PCB layout and discrete LC matching elements parasitics detune the matching network. Thus, fine tuning procedures are required to impose on for eliminating the parasitic effects.

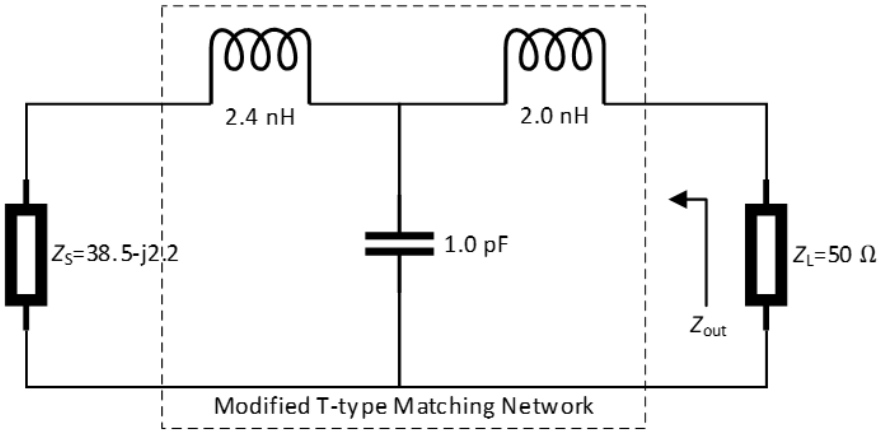
[10] https://wcalc.sourceforge.net/cgi-bin/coplanar.cgi

Figure 4-17: Initial Measured Impedance and S_{11} After Matching



After multiple attempts the two series inductors decreasing to 2.4 nH and 2.0 nH respectively and the shunt capacitor decreasing to 1.0 pF compensate for the PCB layout and discrete parasitic effects, which means the total stray inductance may have a range of less than 1 nH as well as the stray capacitance bring an impact with an amount of ~0.5 pF in our example. Thus, parasitics do not always have negative consequences, sometimes can be taken advantaged of instead.

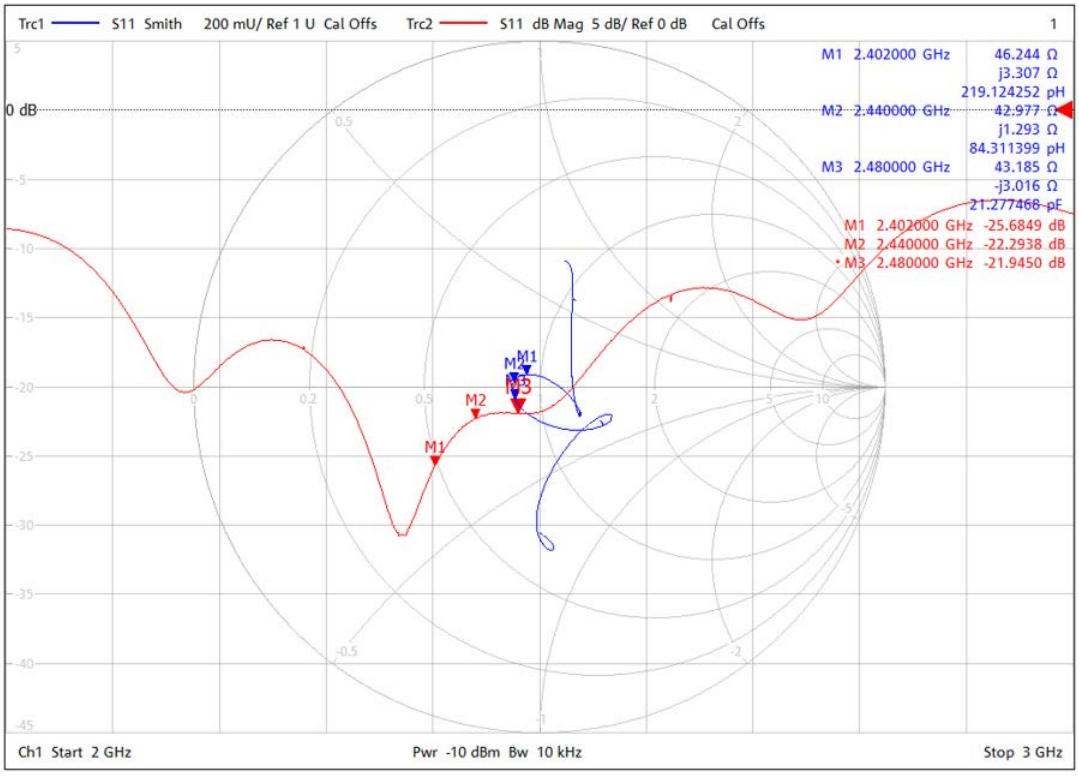
Figure 4-18: Modified Configuration of T-Type Matching Circuit



Finally, the measured impedance and S_{11} characteristics after tuning are shown in Figure 4-19. It seems that it's not a perfect match since the in-band impedances did

not completely converge into the center origin. Why it still occurs after tuning? As mentioned previously, for the available inductance or capacitance sold in the market their component values are not consecutive, so that in most cases approximate solutions can be found, and it's impossible to achieve a totally perfect match in practice. As a matter of fact, to make the in-band S_{11} as low as possible (e.g., lower than -20 dB) or less can ensure enough good broadband matching performance.

Figure 4-19: Final Measured Impedance and S_{11} after Tuning



SECTION

5

Conclusion

Although one perfect or ideal 50-ohm matching may be hard to achieve in engineering practice, it's necessary to design one appropriate matching network that can also benefit many other aspects except impedance matching itself. Measuring the precise output impedance of RFIC is the first critical step towards success since all subsequent matching and tuning operations are depending on it. Each RF engineering individual needs to master the basic knowledge of RF theory, especially transmission line theory and know how to utilize the Smith Chart to simplify impedance matching design procedures.

This design guide described how to intuitively design an optimal lumped-elements matching circuit for Apollo Blue series SoC. The document also provides introduction to some RF concepts along with matching network design points to promote a successful RF front-end board-level design for Apollo Blue series SoC. In addition, it provides the example design applied to Apollo4 Blue based engineering board. However, it should be noted that the example only exhibits how to match and tune step by step and cannot be simply copied to other use cases since RF design is strongly PCB layout dependent.

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