USER'S GUIDE

Hardware Design Guidelines

For Apollo4 and Apollo3 SoC Families

A-SOCAPG-UGGA02EN v1.1

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Revision History

Revision	Date	Description
1.0	November 4, 2022	Initial release
1.1	November 29, 2023	Updated Section 14.2 guidelines for ETM, IOM SPI, and MSPI.

Reference Documents

These reference documents can be accessed on the Ambiq Website and/or Content Portal.

Document ID	Description
DS-A4BP-*	Apollo4 Blue Plus SoC Datasheet
DS-A4P-*	Apollo4 Plus SoC Datasheet
DS-A4B-*	Apollo4 Blue SoC Datasheet
DS-A4-*	Apollo4 SoC Datasheet
PG-A4-*	Apollo4 Family Programmer's Guide
SE-A4P-*	Apollo4 Plus Silicon Errata List
SE-A4-*	Apollo4 and Apollo4 Blue Silicon Errata List
A-SOCAP4-ANGA01EN	Design Guidelines on Magnetic Immunity Application Note
SE-A3P-*	Apollo3 Blue Plus Silicon Errata List
SE-A3-*	Apollo3 Blue Silicon Errata List
n/a	Apollo4 Family SoC Pin Mapping Spreadsheets
n/a	Apollo3 Blue and Apollo3 Blue Plus SoC Pin Mapping Spreadsheets

* Indicates to use the latest version of document

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SECTION

1

Introduction

This document is a compilation of detailed design guidelines for the Apollo3 and Apollo4 SoC families. This document is to be used in conjunction with the selected SoC documentation, including datasheet, programmer's guide (if applicable), and Errata List. See Reference Documents for a comprehensive list.

SECTION

2

Recommended Capacitors for Voltage Supplies

2.1 Overview

This design guideline describes the recommended values and types of output and bypass capacitors for the system on chip (SoC) voltage supplies.

2.1.1 Scope

This document is applicable to all Apollo3 and Apollo4 SoC families

2.1.2 Guidelines

The recommended values and types of capacitors for the Apollo3 and Apollo4 SoC families are listed below.

2.1.2.1 Apollo4 Guidelines

Table 2-1: Apollo4 Recommended Internal Supply and Capacitor Values

Internal Supply	Capacitor
VDDC, VDDC_LV, VDDS	2.2 µF to ground
VDDF	2.2 µF to ground 2.2 µF to VDDP
LPADC_VREF	100 nF to ground
VDDBH	4.7 µF to ground
VDDBH_RF	1 µF to ground

NOTES:
1. 0201, 2.2 µF, 10 V, X5R caps are recommended for these internal rails.
2. Murata GRM033R61A225KE47D used on Ambiq Evaluation Boards.
3. See Apollo4 Errata ERR087 for details on VDDF to VDDP capacitor.

Table 2-2: Apollo4 Recommended External Supply and Capacitor Values

External Supply	Capacitor
VDDP, VDDH, VDDH2, VDDA	1 µF to ground
VDDAUDD	2.2 µF to ground
VDDAUDA	2.2 µF to ground (typical); see notes 4, 5 and 6 below
VDDUSB33	2.2 µF to ground
VDDUSB0P9	2.2 µF to ground
VDD18	2.2 µF to ground
VDDB	2.2 µF to ground

NOTES:
1. Recommend use of 5 V or greater caps for 1.9 V rails.
2. Recommend use of 10 V caps for 3.3 V rails.
3. Do not float any supply inputs. If a supply is not powered, it should be grounded.
4. VDDAUDA supplies power to both the AUDADC and the high-speed crystal oscillator circuit, and care must be taken for selecting an appropriate power supply. Refer to the *Apollo4 SoC Datasheet*, and refer to the *Electrical Characteristics* section for details.
5. Follow recommendations of LDO supplier.
6. Suitable standalone small form factor LDOs:
   a. Microchip MCP1811A in 1.0 x 1.0 x 0.50 mm UDFN package
   b. TI TPS7A02 in 1.0 x 1.0 x 0.40 mm X2SON package

2.1.2.2 Apollo3 Guidelines

Table 2-3: Apollo3 Recommended Internal Supply and Capacitor Values

Internal Supply	Capacitor
VDDC, VDDS	2.2 µF to ground
VDDF	2.2 µF to ground 1.5 - 2.2 µF to VDDP
ADC_VREF	470 nF to ground
VDDBH	4.7 µF to ground
VDCDCRF	1 µF to ground
DVDD	47 nF to ground

NOTES:
1. 0201, 2.2 µF, 10 V, X5R caps are recommended for these internal rails.
2. Murata GRM033R61A225KE47D used on Ambiq Evaluation Boards.
3. See Apollo3 Errata ERR029 for details on VDDF to VDDP capacitor.

Table 2-4: Apollo3 Recommended External Supply and Capacitor Values

External Supply	Capacitor
VDDP, VDDH, VDDA, VCC	1 µF to ground
VDDB	2.2 µF to ground

NOTES:
1. Recommend use of 5 V or greater caps for 1.8 V rails.
2. Recommend use of 10 V caps for rails above 1.8 V.

SECTION

3

SIMO Buck Inductor Selection

3.1 Overview

This guideline describes recommended inductor used for the SIMO Buck.

3.2 Scope

This applies for all Apollo3 and Apollo4 SoC families.

3.3 Guidelines

Recommended SIMO Buck inductor for the Apollo4 and Apollo3 families is described below.

- Apollo3 and Apollo4: 2.2 µH
- Saturation current > 400 mA (> 500 mA preferred)
- Maximum DC resistance < 0.55 Ω
- Operating frequency range > 20 MHz

It is recommended to use the highest saturation current inductor that can meet the board space constraints and cost targets for a particular application, as higher saturation current improves overall system efficiency.

> **NOTE:** For Apollo3 Family, the above saturation current requirements can be relaxed to 120 mA (minimum) to 400 mA when operating within a limited voltage range of 1.755 V – 1.90 V, and limited temperature range of -20°C to 60°C.

Recommended inductors: Murata DFE201610E-2R2M=P2 (0806) or Taiyo Yuden MBKK1608T2R2M (0603)

SECTION

4

BLE Buck Induction Selection

4.1 Overview

This design guideline describes recommended inductor used for the BLE Buck.

4.2 Scope

This applies for all Apollo3 and Apollo4 SoC families.

4.3 Guidelines

Recommended BLE Buck inductor for the Apollo3 and Apollo4 families is described below.

- 1 µH
- Saturation current > 800 mA
- Maximum DC resistance < 0.55 Ω
- Operating frequency range > 20 MHz

Recommended inductor: Murata DFE18SAN1R0ME0 (0603)

SECTION

5

32 kHz XTAL Selection

5.1 Overview

This design guideline describes the recommended components for the 32 kHz XTAL circuit.

5.2 Scope

This applies for all Apollo3 and Apollo4 SoC families.

5.3 Guidelines

The recommended 32 kHz XTAL circuit components used for both the Apollo3 and Apollo4 SoC families are described below.

- 7 pF maximum load capacitance per pin
- 90 kΩ or less ESR
- Start-up time < 300 ms

With the 7 pF maximum pin per load capacitance, it is recommended to choose an XTAL with a capacitive loading specification of 7 pF or less. Use of a lower load capacitance leads to better power efficiency, and as a result it is recommended to pick a crystal rated for 4 pF. The Apollo3 and Apollo4 evaluation boards can be consulted for example selections at the lower (3 pF for Apollo3 Blue Plus) and higher (7 pF for Apollo4 Plus) load ranges.

Note the XI and XO pins form an oscillator circuit that has low bias current to get extremely low power consumption. Therefore, the user's design should ensure that the leakage current on the XI and XO pins are 1 nA or less. Given the low capacitance of loading capacitors, this is not likely to be an issue with component selection, but users should give special consideration to this area of design to ensure parasitic leakages are minimized.

- Apollo4 Evaluation Boards use 9HT12-32.768KDZY
- Apollo3 Evaluation Boards use ABS06W-32.768KHZ-D-2-T

SECTION

6

32 MHz XTAL Selection

6.1 Overview

This design guideline describes the recommended characteristics of the 32 MHz crystal used for each SoC family.

6.2 Scope

This applies for all Apollo3 and Apollo4 SoC families.

6.3 Guidelines

The 32 MHz crystal characteristics for each family are as described below.

6.3.1 Apollo4 SoC Family 32 MHz Crystal Characteristics

The Apollo4 32 MHz XTAL circuitry is designed to work with crystals specified for 6 pF of load capacitance, a maximum ESR of 100 Ω, and a maximum of ± 40 PPM including initial tolerance/aging/temperature drift. It is recommended to choose a crystal with tighter tolerance to account for board-to-board load capacitance variation.

Load capacitors are integrated within the Apollo4, but it is recommended to keep pads available on the PCB design in case additional tuning is required. These capacitor pads do not have to be populated.

For both the Apollo3 and Apollo4 Families, using lower than specified load capacitance could result in lower XTAL frequency. Higher capacitance than the specified value may lead to insufficient frequency trim range.

Apollo4 Evaluation Boards use ABM12W-32.0000MHZ-6-D1X-T3.

6.3.2 Apollo3 SoC Family 32 MHz Crystal Characteristics

The Apollo3 32MHz XTAL circuitry is designed to work with crystals specified for 8 pF load capacitance, a maximum ESR of 100 Ω, and a maximum of ± 40 PPM including initial tolerance/aging/temperature drift. It is recommended to choose a crystal with tighter tolerance to account for board-to-board load capacitance variation.

Load capacitors are integrated within the Apollo3, but it is recommended to keep pads available on the PCB design in case additional tuning is required. These capacitor pads do not have to be populated.

Apollo3 Evaluation Boards use 520-ECS-320-8-47JTNT.

SECTION

7

Apollo3 External 32 kHz Guidelines

7.1 Overview

This design guideline describes the recommended external circuit components and SoC pins required to supply an external 32.768 kHz clock to the Apollo3 family.

7.2 Scope

This applies for all Apollo3 SoC families only.

7.3 Guidelines

Due to design requirements, some customers prefer to use an external oscillator (XO) device, or a temperature-controlled external oscillator (TCXO) as a replacement for the 32.768 kHz crystal. The Apollo SoC's crystal oscillator can be adapted to work with an external clock fed into the Apollo's XO pin. There are two requirements to enable external clocking of the SoC - an acceptable clock signal/circuit and correct register configuration.

The sections below provide guidelines for connecting the oscillator source and sizing the signal properly.

7.3.1 Applicable Silicon Revisions and Packages

This design guideline applies to all versions and packages of Apollo3 Blue SoCs (as well as Apollo2 and Apollo2 Blue).

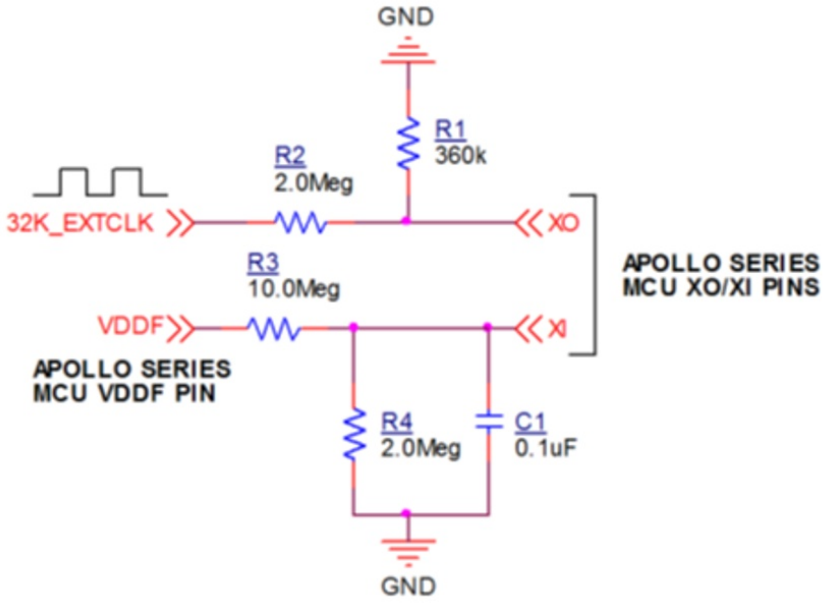
7.3.2 Application Impact

Following these recommendations ensures that the Apollo SoC is clocked reliably and safely with an external clock source.

7.3.3 Clock Signal and Circuit

The crystal-controlled oscillator circuit requires a clock input which meets a specific range of frequency, amplitude and duty cycle. Figure 7-1 shows the recommended circuit diagram, components, and SoC pin connections using a 32.768 kHz external clock (32K_EXTCLK) with peak-to-peak voltage variation allowance from 1.5 V to 3.6 V.

Figure 7-1: 32.768 kHz Crystal Clock Circuit Diagram



The recommended circuit must meet the following requirements:

- 32K_EXTCLK:
  - Frequency range: 32.768 kHz external clock source +/- 10% (29.491 - 36.044 kHz). Operation at any frequency above or below this range is not guaranteed.
  - Duty cycle: 45% - 55%
  - Amplitude (Vmin to Vmax peak-to-peak): Vmin = 0 V to 0.2 V and Vmax = 1.5 V to 3.6 V
- C1 capacitor
  - Tolerance: 30%
- R1, R2, R3, R4 resistors

  - Tolerance: 10%
  - R3, R4 values cannot be changed if this resistor divider is powered from VDDF
  - R2 value must be between 100 kΩ – 2.0 MΩ.
  - R1, R2 values can be adjusted as long as the XO pin voltage requirements below are met.
- XO pin voltage requirements:
  - Voltage input low range: 0 – 35 mV
  - Voltage input peak-to-peak: 340 mV (nominal)
  - Voltage input high range: 260 mV – 440 mV (recommended); 230 mV – 600 mV (acceptable)
- XI pin voltage requirements:
  - Nominal: 130 mV
  - Maximum: 155 mV
  - Minimum: 105 mV
  - Maximum ripple: 10 mV

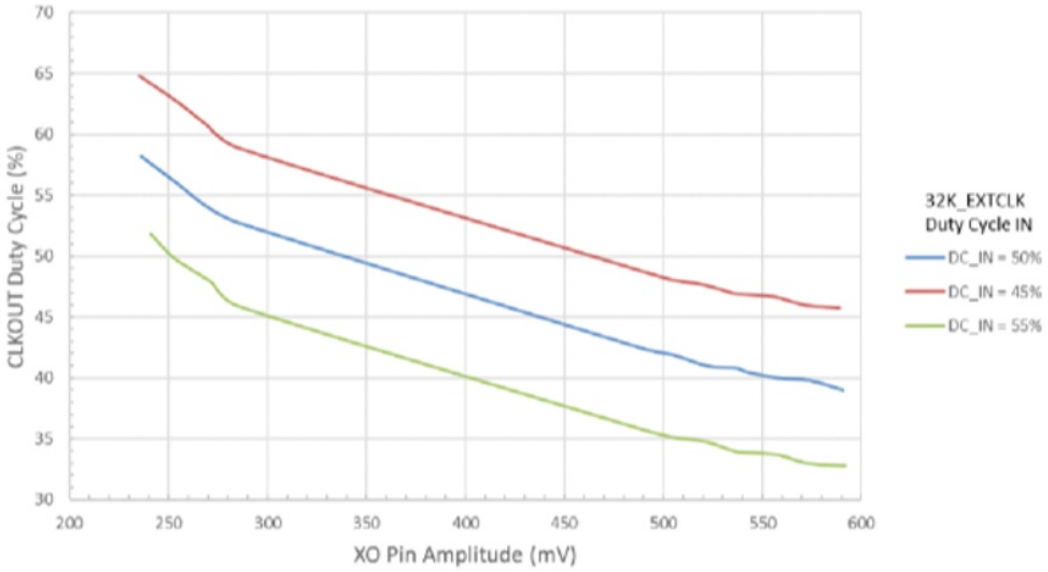
The 32 kHz clock source, 32K_EXTCLK, should be located as close to the XO pin as possible and be routed away from high-switching signals. Trace length should be minimized such that total capacitive load (board + chip pad capacitance) on the XO net should not exceed 5 pF.

NOTE: The user/designer needs to be very careful when probing the net containing the XO pin (output of the resistor divider) and must use a FET probe or similar with ultra-high input impedance (10 MΩ or greater) and very low capacitance (1 pF or less).

7.3.4 Clock Duty Cycle

The chart below shows the CLKOUT duty cycle variation versus XO pin peak-to-peak voltage for 32K_EXTCLK input duty cycles of 45%, 50%, and 55% with an XI pin bias voltage of 135 mV. Under typical conditions, an XO pin peak-to-peak voltage of 340 mV will produce a nominal 50% CLKOUT duty cycle with a 50% 32K_EXTCLK input duty cycle.

Figure 7-2: CLKOUT Duty Cycle: XI Pin Voltage = 135 mV



7.3.5 Register Setting

The XTALBIASTRIM and the XTALKSBIASTRIM fields in the MCUCTRL_XTALGENCTRL register, located at address 0x40020124, must set the crystal bias current and the crystal bias kick start current, respectively, to the minimum setting. The XTALGENCTRL register fields are as shown in the register table below.

XTALGENCTRL Register
XTAL Oscillator General Control
ADDRESS: 0x40020124

Table 7-1: XTALGENCTRL Register Bits

Bit	Name	Reset	RW	Description
31:14	RSVD	0x0	RO	RESERVED.
13:8	XTALKSBIASTRIM	0x1	RW	XTAL IBIAS Kick start trim. This trim value is used during the startup process to enable a faster lock.
7:2	XTALBIASTRIM	0x0	RW	XTAL BIAS trim
1:0	ACWARMUP	0x0	RW	Auto-calibration delay control SEC1 = 0x0 - Warmup period of 1-2 seconds SEC2 = 0x1 - Warmup period of 2-4 seconds SEC4 = 0x2 - Warmup period of 4-8 seconds SEC8 = 0x3 - Warmup period of 8-16 seconds

The XTALBIASTRIM and XTALKSBIASTRIM fields must be set to a value of 0 for the Apollo3 SoC, and 32 (decimal) for the Apollo2 and Apollo2 Blue SoCs.

SECTION

8

Apollo4 USB Guidelines

8.1 Overview

This design guideline describes the USB hardware design considerations for the Apollo4 SoC family. For full details on proper power sequencing and other system use considerations, consult the applicable Apollo4 family SoC datasheet.

8.2 Scope

This applies for all Apollo4 SoC families only.

8.3 Guidelines

Below are several design guidelines which should be followed for proper USB operation.

8.3.1 USB Unused

If the USB peripheral is not used, please leave the USB data pads (USB0PP and USB0PN) floating, and connect the USB PHY power rails (VDDUSB33 and VDDUSB0P9) to ground.

8.3.2 Power Tree

For designs utilizing the USB peripheral, the following power tree is recommended:

1. VDDUSB33 and VDDUSB0P9 should be powered by an LDO with output discharge and ON/OFF control over I^2C or GPIO. It is recommended to source

VDDUSB33 and VDDUSB0P9 power from USB VBUS to minimize system power consumption from the battery. The following devices are examples of suitable standalone, small form-factor LDOs:

a. ST Micro LDBL20 in 0.47 x 0.47 x 0.22 mm STSTAMP™ package

b. ST Micro LD39130S in 0.69 x 0.69 x 0.5 mm CSP package

c. TI LP5910 0.74 x 0.74 x 0.4 mm DSBGA package

2. VDDUSB0P9 noise/ripple should be < 3% (peak-to-peak).
3. On system power-up, VDDUSB33 and VDDUSB0P9 should be in the OFF state.
4. For power-sequencing considerations, see the *Apollo4 SoC Datasheet*.

8.3.3 ESD Protection and Common-mode Filtering

ESD protection on the USB data lines, USB0PP and USB0PN, is required. An integrated CMF and TVS solution, such as the Nexperia PCMF1USB3B/C or Panasonic EXC-14CS900H, is recommended.

If the design achieves EMC compliance without CMF on the USB data lines, then a TVS-only solution, such as the TI ESD122DMXR, may be used.

8.3.4 USB VBUS Detection

The Apollo4 family has no 5 V tolerant pins. Therefore, it relies on the external circuit for getting VBUS power OK (VBUS connected) status. The recommended solution is to connect the PMIC/charger VBUS_OK output to an Apollo4 GPIO configured as an interrupt.

8.3.5 Other Considerations

In the case that VDDUSB33 may be powered while VDDUSB0P9 is powered-down, up to 34 mA may be consumed by the USB PHY. This scenario should be avoided. However, if for some system design this situation is unavoidable, weak pull-down resistors (~10 MΩ) may be added to both D+ and D-.

SECTION

9

MIPI DSI PHY Guidelines

9.1 Overview

This design guideline describes guidelines for the MIPI Display Serial Interface (DSI) PHY.

9.2 Scope

This applies for all Apollo4 SoC families only.

9.3 Guidelines

9.3.1 Unused

If the MIPI DSI interface is not used, the DSI data and clock pads, MIPI_D0P, MIPI_D0N, MIPI_CLKP and MIPI_CLKN, must be left floating. The MIPI supply pads, VDD18 and VSS18, should be tied to ground.

9.3.2 Power Tree

The recommended power tree for the DSI PHY is as follows:

1. VDD18 is powered by an LDO with output discharge and ON/OFF control over I^2C or GPIO. Noise/ripple should be kept to ±2% (72 mVpk-pk), frequency range 10 MHz – 3 GHz.
2. On system power-up, VDD18 should be disabled.

NOTE: On Apollo4 and Apollo4 Blue, powering VDD18 without powering the DSI TX/D-PHY internal power rails results in uncontrolled current leakage to VDD18 and may lead to long-term reliability issues. This has been resolved for Apollo4 Plus devices. Consult the *Apollo4 SoC Datasheet* for proper power-up sequence to avoid this issue.

SECTION

10

MRAM Considerations

10.1 Overview

This design guideline describes guidelines to prevent MRAM corruption/damage.

10.2 Scope

This applies for all Apollo4 SoC families only.

10.3 Guidelines

The Apollo4 family SoCs contain non-volatile Magneto-resistive Random Access Memory (MRAM). MRAM is susceptible to strong external magnetic fields and requires proper handling in the commercial and industrial environments. For design guidelines and system considerations, reference the *Apollo4 MRAM Design Guidelines Application Note A-SOCAP4-ANNA01EN*.

SECTION

11

AUDADC Considerations

11.1 Overview

This design guideline gives recommendations for using and powering the Audio Analog-to-Digital Converter (AUDADC).

11.2 Scope

This applies for all Apollo4 SoC families only.

11.3 Guidelines

The Apollo4 SoC family supports a low power analog audio interface, referred to as the AUDADC, for interfacing to analog micro-electro-mechanical systems (MEMS) microphones or line inputs. The AUDADC circuit can accept up to two fully-differential or pseudo-differential inputs, or four single-ended inputs.

AC-coupling capacitors are used to block the common-mode voltage (VCM) from the Apollo4 AUDADC PGA input network from the VCM of the chosen ADC input source. These AC-coupling capacitors can be sized between 100 nF to 1 µF, and, together with the input impedance, form a high-pass filter for the input signals.

For best signal-to-noise ratio performance, it is recommended to use an analog microphone (AMIC) with a fully differential signal output. If the AMIC does not provide a fully differential signal, then pseudo-differential signaling must be used. In pseudo-differential mode, the LPADC_DxP pin should be connected to the AMIC output through the selected AC-coupling capacitor, while the LPADC_DxN pin should be connected to ground through a capacitor of the same value. These AC-coupling capacitors can be either X5R or X7R, however X7R is recommended for better performance across temperature.

11.3.1 Mic Bias

No pull-ups or pull-downs are needed on mic bias lines. MICBIAS can source up to 200 µA at 1.5 V, and should have a 2.2 µF decoupling capacitor.

MICBIAS provides a user-programmable 0.9 V to 1.5 V supply for analog Mems microphones. Microphones that need 1.62 V or greater (up to 1.98 V) can be supplied directly using VDDAUDA. MICBIAS bypass mode is active when the MCUCTRL_AUDIO1_MICBIASVOLTAGETRIM[5:0] field is set to 0x3F. This sets MICBIAS as a bypass that outputs VDDAUDA voltage, which allows the MICBIAS circuit to act as a load-switch for analog microphones requiring voltage greater than 1.5 V.

11.3.2 Anti-Aliasing

This section discusses how to tune the corner frequency of the Apollo4 family AUDADC's anti-aliasing filter using external passive components.

An alias occurs when a signal above half the sample rate is allowed into, or created within, a digital system. An anti-aliasing filter is responsible for limiting the frequency range of the analog input signals before getting converted, so the maximum frequency coming into the system is less than half the sampling rate (Nyquist limit).

The higher the Nyquist frequency, the less risk of distortion. The higher the sampling frequency/oversampling, the less likely it is to capture distortion since you are moving the lower image further away from the wanted audio. The level represents the amplitude of the signal.

Figure 11-1: Frequency of the Apollo4 Family AUDADC's Anti-Aliasing Filter

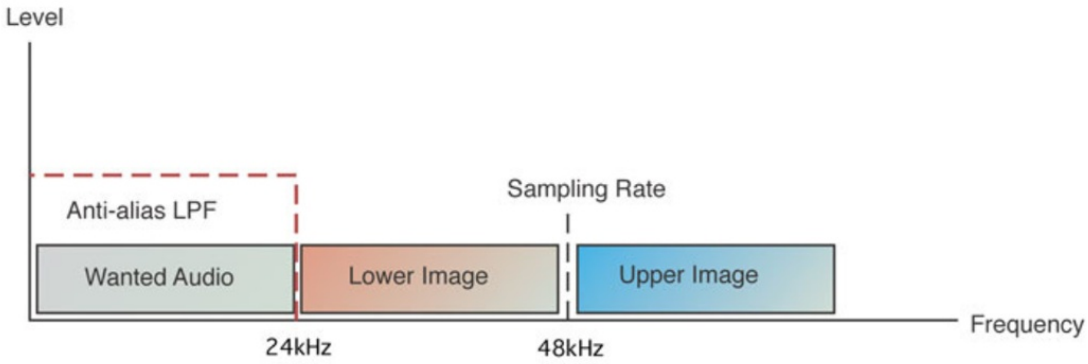
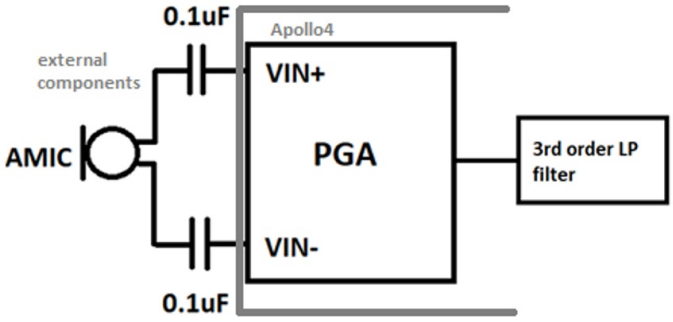


Figure 11-2 on page 28 is a representation of the AUDADC input circuitry which include an analog microphone (AMIC), AC coupling capacitors, a programmable gain amplifier (PGA) and the internal anti-aliasing filter.

Figure 11-2: Apollo4 AUDADC Input Circuitry Without External Anti-Aliasing Filter Components



In a fully differential topology, the PGA input impedance can be assumed to have the following values.

- If gain ≥ 12 dB, then impedance = 2 MΩ.
- If gain is between 0 dB and 12 dB, the impedance is between 0.49 MΩ and 1.13 MΩ.

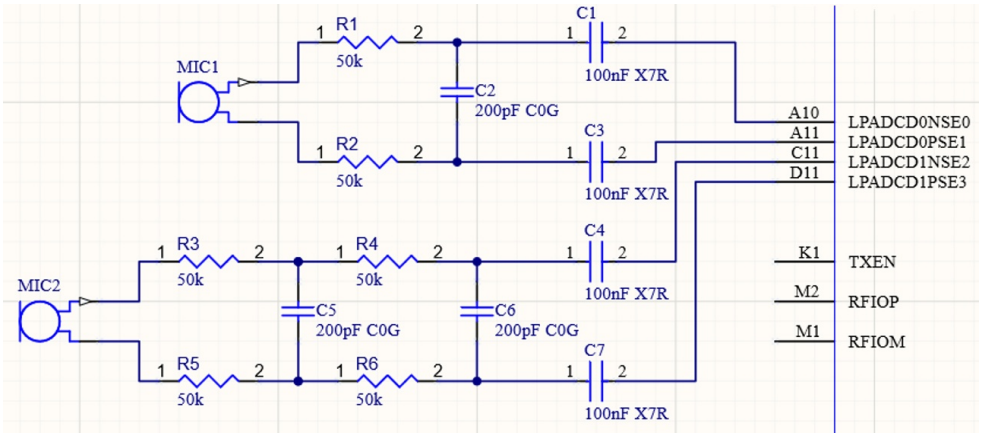
The cut off frequency for the third Order RC low pass filter after the PGA is set to 80 kHz.

This is important because, in an audio application, the minimum impedance usually determines how large the AC coupling capacitors between the AMIC and the PGA need to be to get the right high-pass filter corner. The larger the input resistance, the smaller the capacitors need to be for a given corner frequency.

The worst case of the input impedance can be used as a starting point to select the proper resistor values that are at least 5x smaller from the input impedance of the PGA. The smaller value compared to the PGA is to limit the effect of the cut off frequency of the filter.

Figure 11-3 shows a schematic of MIC1 with a first order low pass filter, and MIC2 with a second order low pass filter.

Figure 11-3: AUDADC with External Anti-Aliasing Filters



11.3.3 1st and 2nd Order RC Filter Option

Table 11-1: Frequency Cut off (Fc) Equation

Order	Frequency Cut-off Equation
1st order roll-off (20 dB per decade after Fc)	$F_c = 1/(2\pi RC)$
2nd order roll-off (40 dB per decade after Fc)	$F_c = 1/(2\pi \times \text{sqrt}(R1 \times R2 \times C1 \times C2))$ If R1 = R2 and C1 = C2 then: $F_c = 1/(2\pi RC)$

Table 11-2: First and Second Order (with same R and C) Values for a Determined Fc

C	R	Fc
80 pF	104.5 kΩ	19.04 kHz
100 pF	104.5 kΩ	15.23 kHz
200 pF	104.5 kΩ	7.62 kHz

11.4 Simulation Values with LTspice

Circuit simulated: In this drawing, the 4.5 kΩ represent the MIC impedance, the 1 MΩ represent the input impedance of the PGA.

Figure 11-4: Circuit Simulated

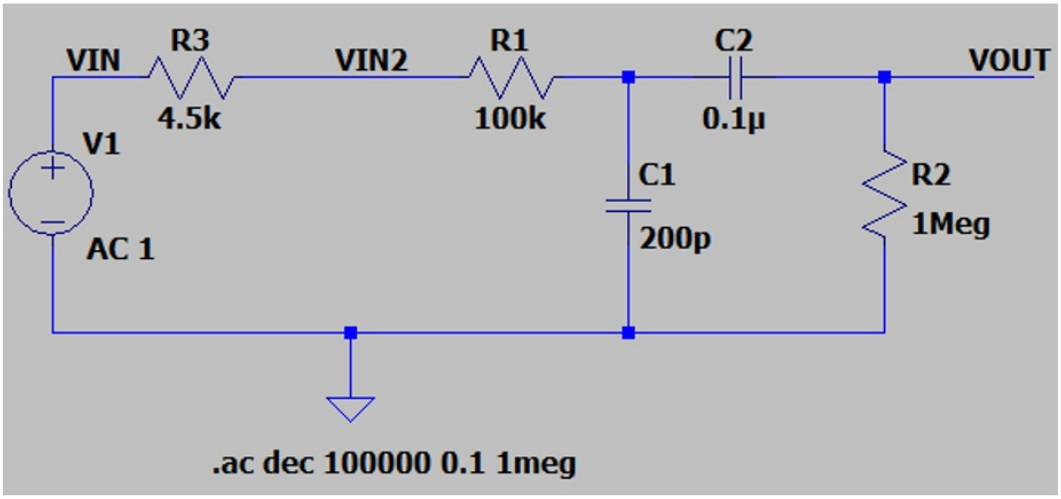
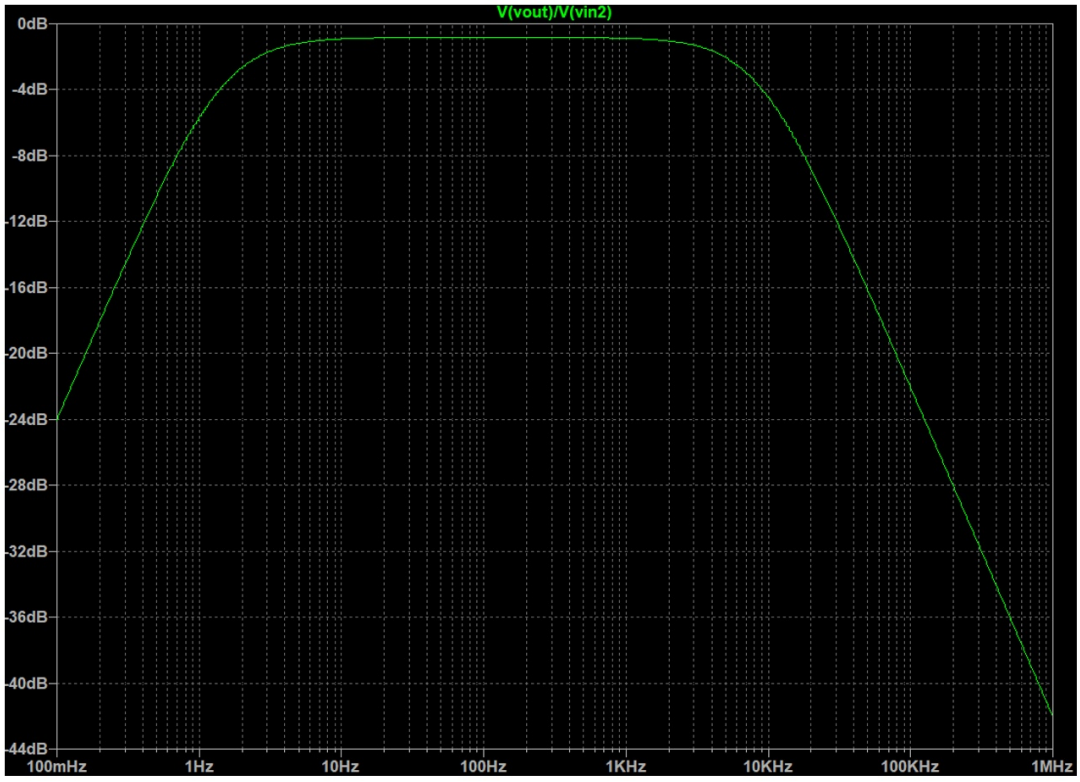


Figure 11-5: Circuit Simulated Results



11.4.1 Component Selection

For audio applications, it is recommended to use C0G capacitor because they are not significantly affected by temperature, applied voltage, aging, electrical losses and have high stability and accuracy.

SECTION

12

Apollo3 Family No-Bluetooth Low Energy Configuration

12.1 Overview

This design guideline describes circuit modifications and simplifications when not using Bluetooth Low Energy.

12.2 Scope

This applies for all Apollo3 SoC Family only.

12.3 Guidelines

The following guidelines should be followed to configure the Apollo3 SoC when not using Bluetooth Low Energy. Refer to the Apollo3 Blue or Apollo3 Blue Plus EVB schematic for the full schematic and for components, supplies and circuits referenced below. Note that the BLE inductor remains populated to support operation of turboSPOT® mode in this configuration. If turboSPOT mode is not a requirement, see *Section 13 Apollo3 Family Inductor-less Operation on page 32* for details on additional hardware configuration changes.

- The DVDD rail is not supplied and the DVDD pin is not connected. Its bypass capacitance is not needed.
- No need for a special VCC supply. Tie the VCC pin to the other supplies (VDDP, VDDH, VDDA, and VDDB)
- The 32 MHz crystal circuit is not needed. X032MP and XO32MM may be left floating
- The antenna circuit is not needed. RFIOP may be left floating, RFIOM should be connected to PCB ground
- All VSS pins, including VSSB, are tied to PCB GND.

SECTION

13

Apollo3 Family Inductor-less Operation

13.1 Overview

This design guideline describes when and how the SIMO Buck and BLE Buck inductors may be omitted.

13.2 Scope

This applies for all Apollo3 SoC Family only.

13.3 Guidelines

For space-constrained applications, the user may decide to not include the SIMO Buck and BLE Buck inductors in the design. Note that the BLE Buck circuit, which includes the BLE inductor, also provides power for high-speed turboSPOT mode. If turboSPOT is not required, the BLE Buck inductor may be removed. BLE production trims are calibrated with the BLE Buck turned on. For Bluetooth Low Energy enabled designs without the BLE Buck inductor, it is required to keep the system operating voltage at 1.8V. Also, removing the SIMO Buck inductor disables SIMO Buck mode, in which case only LDO mode is available.

The following guidelines should be taken into consideration when designing the system hardware.

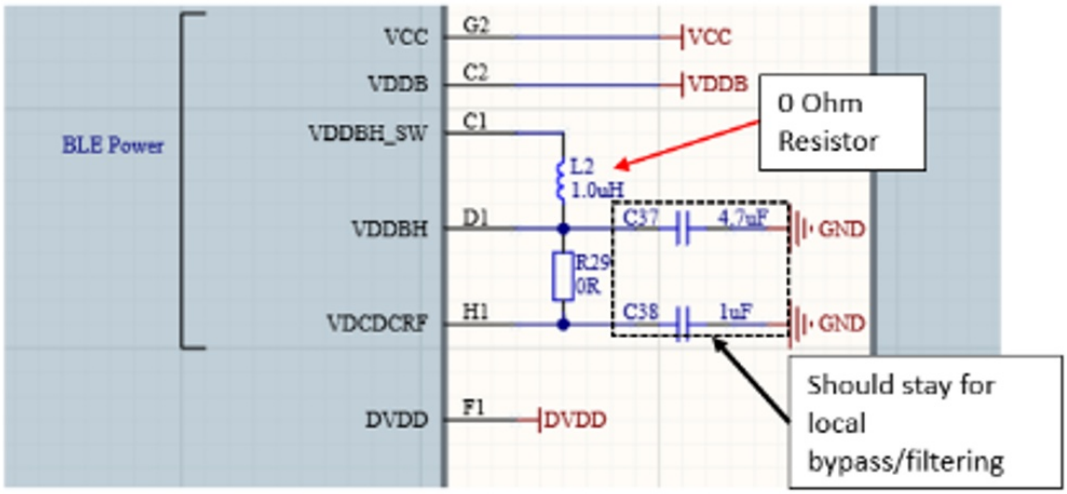
13.3.1 SIMO Buck

SIMOBUCK_SW and SIMOBUCK_SWSEL may be left floating. In this configuration, the OTP_CUSTOMER_TRIM setting must have the SIMO_BUCK disabled by setting the PWRCTRL_MISC_SIMOBUCKEN bit to ‘0’. In this configuration, the SIMO Buck circuit remains powered down. Consult the *Apollo3 SoC Datasheet*.

13.3.2 BLE Buck

The BLE inductor is replaced with a 0 Ω resistor, creating a short between VDDBH_SW and VDDBH. The 4.7 µF bypass capacitor on VDDBH should remain for local bypass capacitance. If Bluetooth Low Energy operation is intended, then the 1 µF VDCDCRF capacitor should remain as well. Otherwise, for non-Bluetooth Low Energy operation, VDCDCRF's bypass capacitor may be removed.

Figure 13-1: BLE Inductor



SECTION

14

Appendix - Review Checklists

This section includes the following two review checklists forms:

- Schematic Review Checklist
- Layout Review Checklist

14.1 Schematic Review Checklist

14.1.1 Overview

This design guideline provides a checklist when conducting a schematic review of an Apollo SoC design.

14.1.2 Scope

This applies for all Apollo3 and Apollo4 SoC families.

14.1.3 Guidelines

Table 14-1: Schematic Review Checklist

Item	Schematic Review Checklist	
1	Confirm the Ambiq SoC symbol against the package appropriate pin numbers provided in the datasheet to ensure correct mapping of power, signal, and ground pads.	☐
2	Verify all intended GPIO and peripheral connections against the Apollo SoC family pin map in the datasheet. Alternatively, the Ambiq-provided pin mapping spreadsheets, linked below, can assist with this: ▪ Apollo3 family pin mapping See the *NCE Encoding Table* in the Apollo3 Blue or Apollo3 Blue Plus Datasheet for chip select mapping considerations ▪ Apollo4 family pin mapping	☐
3	Check the reset pin. External 1nF capacitor recommended to filter external noise/glitches. Consider including pads for an external pull-up resistor. If an external IC is connected to control nRST, it must be open-drain.	☐
4	Check SWDCK and SWDIO, which should be connected to a debug header. ▪ SWDCK needs a 10 kΩ pull-down resistor ▪ SWDIO needs a 10 kΩ pull-up resistor	☐
5	Check SWO, which is recommended to be routed to a header or test point	☐
6	Check all decoupling and bypass capacitor values to ensure they're meeting recommended values. Confirm the SIMO Buck and BLE Buck (if applicable) inductors meet the recommended specifications.	☐
7	Confirm 32 kHz XTAL and 32 MHz XTAL (if applicable) specifications meet datasheet recommendations. If an external oscillator high-speed oscillator is used, confirm it meets the requirements	☐
8	Ensure the design follows the SoC errata guidelines. All errata should be reviewed, with particular attention paid to: ▪ Apollo3: ERR029 ▪ Apollo3 Plus: ERR022, ERR023, ERR025, ERR029 ▪ Apollo4: ERR008, ERR014, ERR039, ERR046, ERR056, ERR066, ERR070, ERR087, ERR096, ERR108. ▪ Apollo4 Plus: ERR008, ERR039, ERR046, ERR056, ERR066, ERR087, ERR096, ERR097.	☐

14.2 Layout Review Checklist

14.2.1 Overview

This design guideline lists layout considerations in the form of a checklist for an Apollo SoC layout design.

14.2.2 Scope

This applies for all Apollo3 and Apollo4 SoC families.

14.2.3 Guidelines

This section provides guidance for the collection of modules supported by Apollo SoCs.

Table 14-2: Layout Review Checklist

Layout Review Checklist		
Item	**Power**	
A1	Decoupling capacitors, such as those for VDDP, VDDA and VDDH, should be as close as possible to their respective pins.	☐
A2	For power rails that connect to inner balls of the SoC, the decoupling capacitor should ideally be placed on the opposite side of the SoC, directly under the pin, with a via to connect them. If a via must be used to connect to a capacitor on the same surface as the SoC, the trace should be kept as short as possible	☐
A3	For the Buck inductors (SIMO Buck and BLE Buck), it is recommended to have solid ground underneath the traces and inductors.	☐
A4	SIMO and BLE Buck traces should be as thick and as short as possible. If it is not possible to minimize both inductor traces, the switch node (e.g., SIMOBUCK_SW) should be prioritized for the shortest trace length.	☐
A5	If using Bluetooth Low Energy and/or Audio, VDDAUDA should be routed in such a way to minimize its exposure to high frequency and noisy signals, such as MSPI clock signals or Buck converter outputs. It is recommended to have it shielded with ground.	☐
A6	Power connections should be routed with planes. If not possible, use traces that are as thick as possible within the design constraints.	☐

Table 14-2: Layout Review Checklist *(Continued)*

Layout Review Checklist		
Item	**Oscillators**	
B1	Oscillator traces and components should be shielded as much as possible with ground.	☐
B2	Maintain a solid ground plane on the layer adjacent to the oscillator circuitry, avoiding routing other signals directly underneath the crystal and capacitors.	☐
Item	**MSPI**	
C1	MSPI signals should be impedance matched to 50 Ω ± 20%, using a solid reference plane.	☐
C2	MSPI signals should not be routed over any discontinuities in the reference plane.	☐
C3	Ideally, all MSPI signals in a group should be routed on the same signal layer.	☐
C4	MSPI Data signals should be trace-length matched to within ± 500 mils of the Clock signal.	☐
C5	Minimize the use of vias as much as possible.	☐
C6	For Apollo3 Blue Plus, the capacitance loading on any MSPI signal (clock and data lines) is limited to no higher than 30 pF. For the Apollo4 Family, due to its higher data rates, the limit is 20 pF.	☐
Item	**IOM SPI**	
D1	IOM SPI can support clock rates up to 48 MHz; thus it is recommended to follow the MSPI layout guidelines above.	☐
D2	For Apollo3 Blue Plus, the capacitance loading on any IOM SPI signal (clock, MISO, and MOSI) is limited to no higher than 25 pF. The minimum MISO input data setup time is 4 ns.	☐
Item	**MIPI**	
E1	The MIPI clock and data signals should be impedance matched to 50 Ω ± 15% single-ended, 100 Ω ± 15% differential.	☐
E2	MIPI clock and data trace pairs should be trace-length matched as closely as possible.	☐
E3	Maintain a solid ground reference for the MIPI traces, avoid routing over any discontinuities in the plane.	☐

Table 14-2: Layout Review Checklist *(Continued)*

Layout Review Checklist		
E4	Minimize via use as much as possible.	☐
Item	**USB**	
F1	The USB signals should be impedance matched to 50 Ω ± 15% single-ended, 90 Ω ± 15% differential.	☐
F2	The USB trace pair should be trace-length matched as closely as possible, and should not exceed 50 mils in trace length difference.	☐
F3	Maintain a solid ground reference for the USB traces, avoid routing over any discontinuities in the plane.	☐
F4	Minimize via use as much as possible.	☐
Item	**Radio**	
G1	The RFIOP trace connecting to the matching network and antenna should be impedance controlled to 50 Ω.	☐
G2	Maintain a solid ground plane beneath and next to the matching components and traces leading to the antenna.	☐
Item	**eMMC**	
H1	eMMC signals should be impedance matched to 50 Ω ± 15%.	☐
H2	eMMC data and CMD signals should be trace-length matched to within ± 500 mils of the clock signal.	☐
H3	eMMC signals should be referenced to a solid plane (VDD or GND).	☐
H4	eMMC signals should not be routed over any discontinuities in the reference plane.	☐
Item	**AUDADC**	
I1	AUDADC positive and negative signals should be routed differentially, with ground surrounding and shielding the traces on the adjacent layer.	☐
I2	Match the routing of the AUDADC channels as closely as possible.	☐
I3	Minimize impedance by increasing AUDADC trace width.	☐
Item	**ETM**	
J1	Place the ETM connector as close as possible to the Apollo SoC.	☐
J2	Avoid sharing ETM trace pins with other GPIO functions.	☐

Table 14-2: Layout Review Checklist *(Continued)*

Layout Review Checklist		
J3	ETM signals should be impedance matched to 50 Ω ± 15%.	☐
J4	ETM signals should be referenced to a solid plane (VDD or GND).	☐
J5	To minimize overshoot and ringing, it is recommended to place series resistors at the output pins of the Apollo SoC. 27-33 Ω is a typical range.	☐
J6	ETM data signals should be length-matched within 390 mil of the clock signal to minimize calibration during setup.	☐

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