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Apollo3 Family
Power Consumption Optimization & Technical Details

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Power Consumption Optimization

Power Optimization: Sleep

- Apollo3 sleep modes are very flexible.
- Entering Normal or Deep Sleep does not automatically change the clock source for timers, nor does it stop or disable any peripherals or interrupt sources.
- Configure the peripherals and GPIO in the desired way and they will continue to operate in normal or deep sleep. Keeping peripherals active will result in higher deep sleep current, so for lowest power deep sleep, all peripherals not actively in use should be powered down.

Power Optimization: Sleep

- It is straightforward to enter sleep modes:
  - am_hal_sysctrl_sleep(AM_HAL_SYSCTRL_SLEEP_DEEP);
  - am_hal_sysctrl_sleep(AM_HAL_SYSCTRL_SLEEP_NORMAL);
- Any Apollo3 interrupt can be used as a wake trigger from normal or deep sleep.
- Common wake interrupt sources used in deep sleep include:
  - GPIO, Ctimer, Stimer, RTC Alarm, Comparator, ADC Window compare, I2C/SPI slave write, FIFO threshold interrupts for any serial interface, etc.

Power Optimization: Sleep

- The Binary counter example project is a good example of using LFRC as Timer count source and going to deep sleep with that timer running. The timer then generates a periodic wake interrupt.
- Keeping timers running from either XT or LFRC add <100nA to deep sleep current (plus the current of the clock source, which is ~300nA for XT and <100nA for LFRC).

Power Optimization: Sleep

- All Apollo3 GPIO can be used as a wake source.
- To configure a GPIO as a wake source, enable the interrupt for that GPIO. Please see the deepsleep_wake project for simple example of this.
- All GPIO have configurable interrupts, and any GPIO that has interrupt enabled will wake the MCU from deep sleep upon GPIO interrupt.
- All Timers can be used as a wake source.

Power Optimization: Tips

- The HFRC will be stopped automatically when entering deep sleep UNLESS there are peripherals or timers running that need HFRC.
  - For lowest power deep sleep, any timer or peripheral that is configured to use HFRC should be stopped before entering Deep Sleep.

Power Optimization: Tips

- On Apollo3, peripherals such as UART, IOM (SPI/I2C master), IOS (SPI/I2C Slave), MSPI, ADC, and PDM all have a peripheral power enable/disable bits.
  - All of these peripherals start powered off. This power-gates the peripheral for minimum leakage in deep sleep.
  - Each of these peripherals must be power-enabled before they can be used. Upon setting the power enable bit, the peripheral will start in default state and needs to be configured.
  - When going to deep sleep, any of these peripherals that is not active should be powered down to minimize deep sleep current.
- The AmbiqSuite HAL includes power_control functions that automate this process by saving the config setting before powering down the peripheral and write the saved settings to the peripheral when powering it back on.

Power Optimization: Tips

- To enable the MCU core to be put to sleep while peripherals are active, most Apollo3 peripherals have FIFOs, and many also have DMA and command queue support.
- Peripherals with FIFOs:
  - IOM I2C/SPI Master: 32Bytes TX and 32Bytes RX
  - MSPI: 16-entery FIFO (32 Bits Wide)
  - IOS I2C/SPI Slave: 256 Byte LRAM (Direct access / FIFO)
  - BLE: Virtual FIFO in BLE subsystem SRAM (42K total RAM)
  - ADC: 16-deep FIFO
  - PDM: 32 Words
- Peripherals with DMA support:
  - IOM I2C/SPI Master, MSPI, ADC, BLE, PDM
- Peripherals with Command Queue support:
  - IOM I2C/SPI Master, MSPI

Default Active State

- MCU core active with 48MHz core clock
- All Flash and RAM start powered/enabled, but cache starts disabled
- All Pins start with GPIO buffers disabled (High-Z) except for the two SWD pins and the SWO pin (GPIO41)
  - GPIO20 and GPIO21 are configured as SWDIO and SWDCK with no internal pull-up/down (i.e. floating) so these either need external pull-up/down as recommended in design guide or need to be reconfigured by software. All other pins can be left unconnected.
  - **Note**: all GPIO pins have ESD diodes that connect the GPIO pin to MCU VDD. Regardless of GPIO configuration, voltage applied to GPIO pin should not exceed VDD.
- XT and RTC clock start enabled at initial power-up. However, the standard bsp init code in the SDK stops both.
  - Unlike nearly all other registers, the state of XT and RTC are not cleared by any reset other than power-on reset (to allow RTC to operate through brownout or software resets without losing time). Therefore, it is prudent to explicitly initialize these to desired state after reset regardless of default power-on-reset state. (Low power init function disables XT and RTC)
- Peripherals (I2C/SPI, MSPI, UART, ADC, PDM) start powered-off (power-gated)

Normal Sleep

- When normal sleep mode is entered:
  - Clock is gated from the CPU Core
  - Flash remains powered in standby mode
    - Shutting down the upper block of Flash will reduce normal sleep power consumption)
  - Everything else that was active before the sleep command remains active. HFRC continues to run but is gated from the core.

Deep Sleep

- When Deep sleep is entered, anything that is not being used will be powered down:
  - All GPIO retain state, and any GPIO can be configured to generate an interrupt which will wake the MCU from deep sleep
  - Flash is shut down (so Flash power-down commands do not impact deep sleep power consumption)
  - SRAM transitions to a low-power retention state
    - Deep Sleep retention setting determines how much of the SRAM is retained.
  - If cache is enabled, it is retained or not based on cache deep sleep retention configuration
  - Any clocks (HFRC, XT, and LFRC) not being used by peripherals or timers will be stopped. Conversely, any clock that is being used will continue running.
  - Any peripheral that is powered on will stay on. For lowest power deep sleep, this is the most critical item, to power down as many peripherals as possible.
    - **Note**: this does not include RTC, CTimers, or STimer which are very low power as long as they are using LFRC, XT, or low frequency external timer input as clock sources. These can be left running in deep sleep. The XT and LFRC clocks are very low power.

Example Power Consumption @ 3.3V

- Apollo3 does not support reducing the CPU clock, so optimal power consumption is achieved by going to sleep whenever there is no active processing.
- Example application that wakes from Deep Sleep every 10ms to perform 100µs of processing @ 48MHz:
  - 2.7µA Deep Sleep
  - 2.9µA Transition current for waking up 100 times/second from Deep Sleep
    - Includes MCU wake-up energy consumption and active power consumption jumping to/from ISR
  - 5.8µA Active Processing
  - **11.4µA** Total
- Best competing processors will consume **>30µA** just for the active processing and most are much higher

Example Power Consumption @ 1.8V

- Apollo3 does not support reducing the CPU clock, so optimal power consumption is achieved by going to sleep whenever there is no active processing.
- Example application that wakes from Deep Sleep every 10ms to perform 100µs of processing @ 48MHz:
  - 3.8µA Deep Sleep
  - 3.6µA Transition current for waking up 100 times/second from Deep Sleep
    - Includes MCU wake-up energy consumption and active power consumption jumping to/from ISR
  - 8.9µA Active Processing
  - **16.4µA** Total
- Best competing processors will consume **>30µA** just for the active processing and most are much higher

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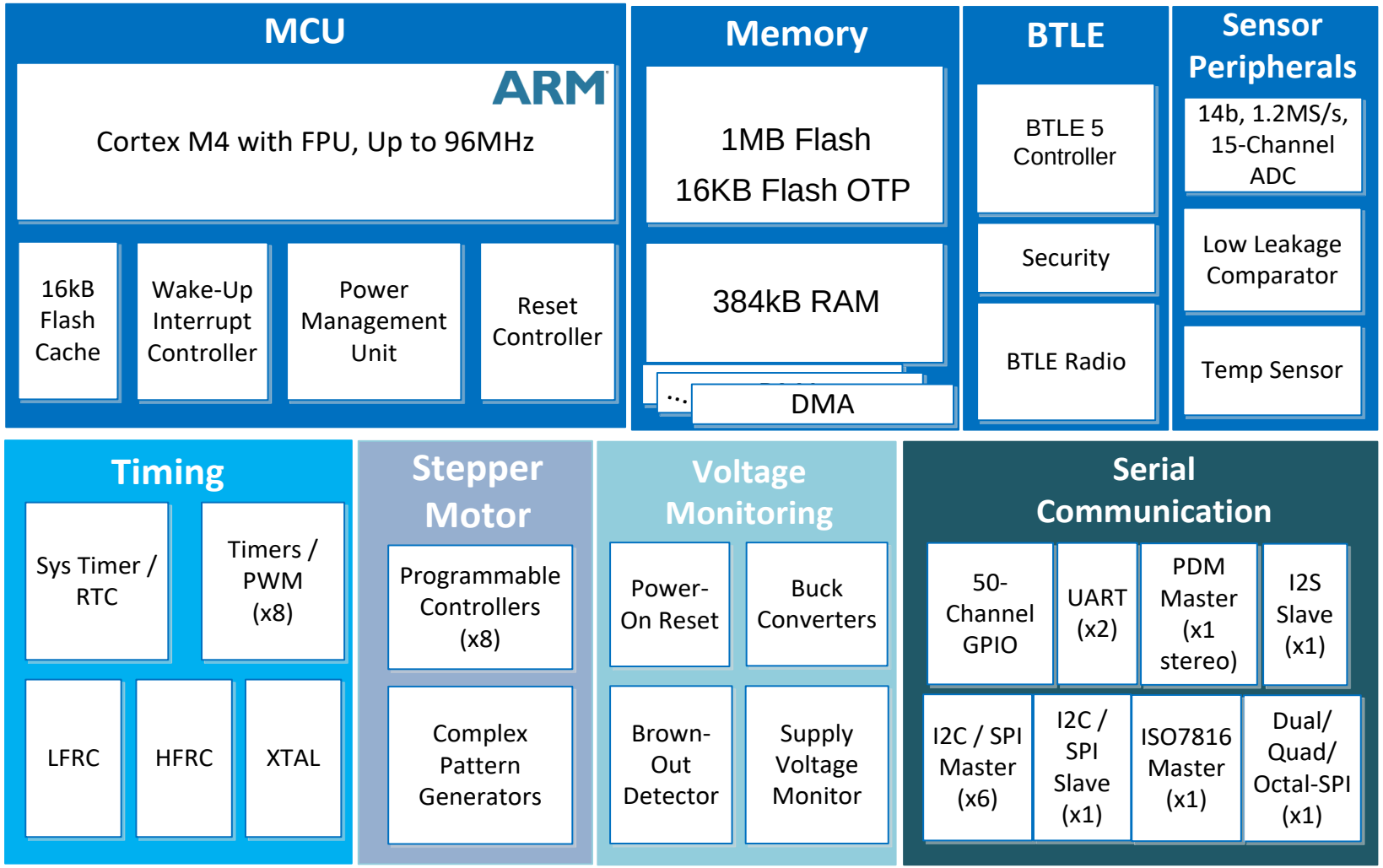
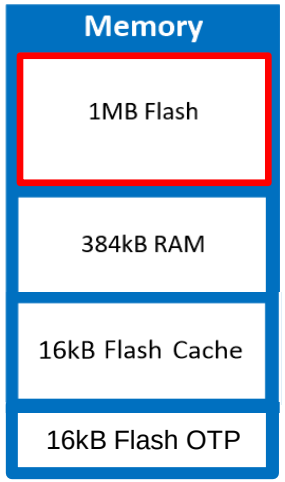
Apollo3 Blue Technical Details

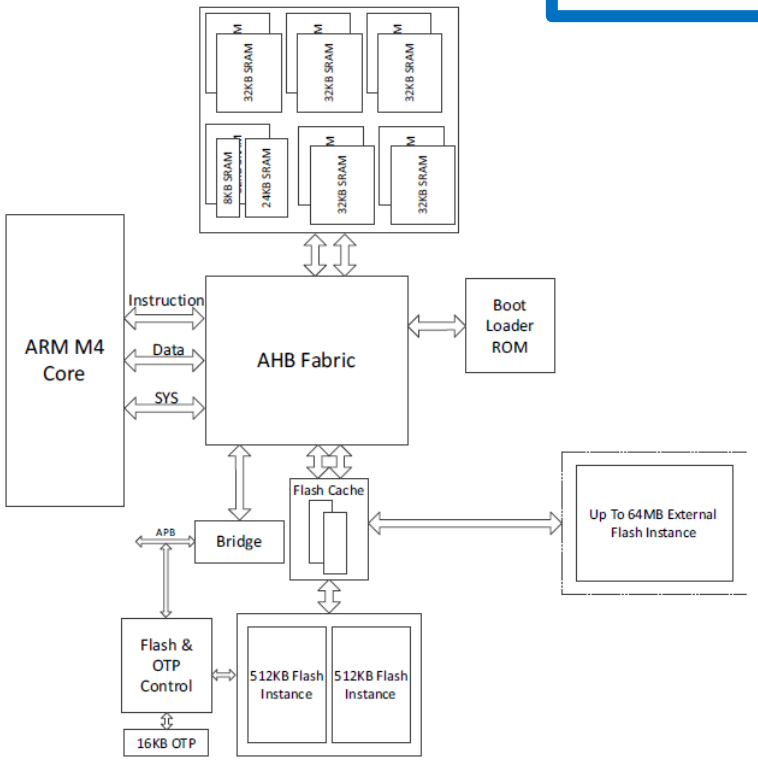
Apollo 3 Blue System Block Diagram



Memory: Flash

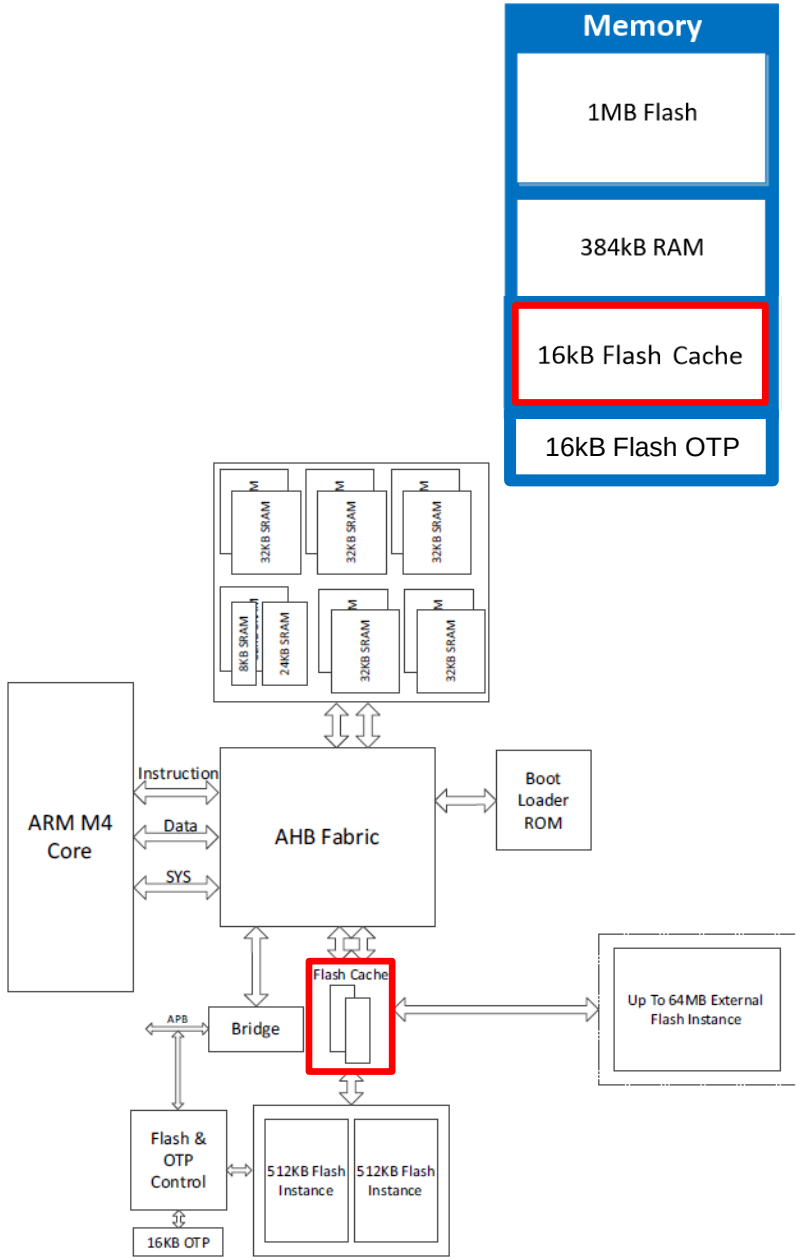
- 1MB of Flash
- 2x 512KB Flash Instances
  - Independent power control
  - Independent mass erase
- Flash Protection in 16KB Chunks
- Flash erase by 8KB Page





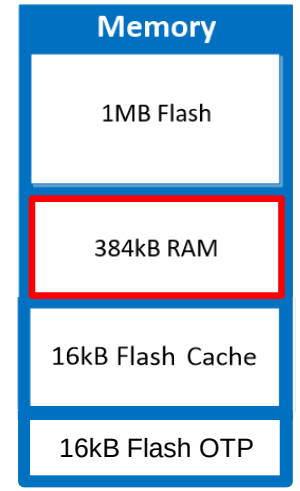
Memory: Cache

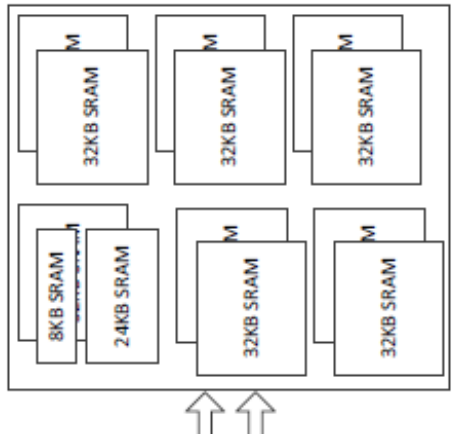
- 16KB Cache
  - 2-way set-associative or Direct Mapped
  - 512/1024 entry, 128b line size
- Unified ICode and DCode cache controller Configurable to cache Instruction, Data, or Both
- Caching is supported for the entire 1MB internal Flash and the 64MB external Flash aperture (via MSPI)
- Intended to provide single cycle read access to Flash and reduce overall accesses to the Flash to reduce power.
- Two regions can be designated as non-cacheable

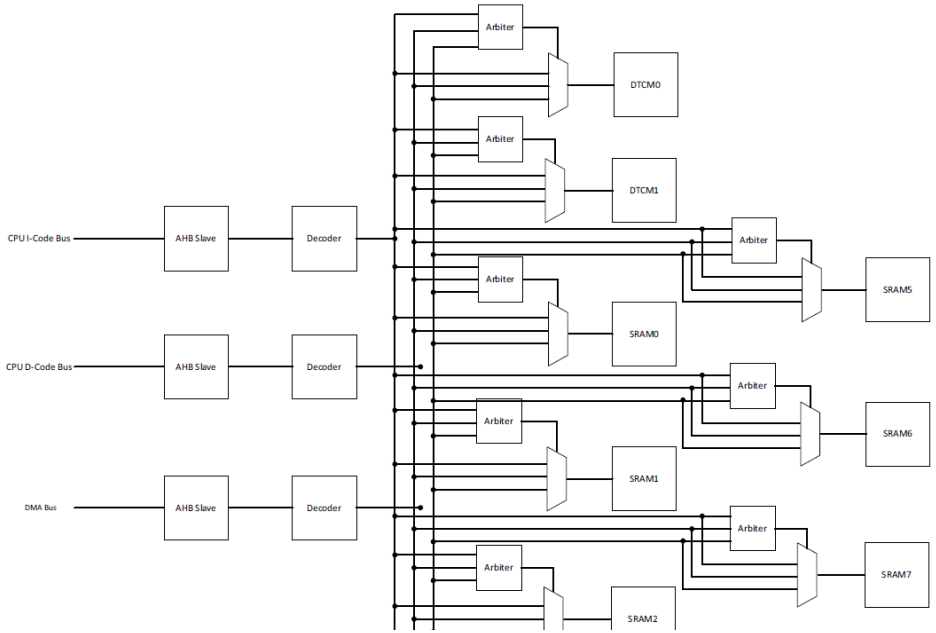


Memory: SRAM

- 384KB SRAM
- DTCM Banks (first 64KB) guaranteed zero wait-state unless there is contention for that specific memory array with another requestor (CPU I/D Bus or DMA Bus).
- Main SRAM banks (64K-384KB range) are zero wait-state for sequential accesses or 1-wait state for non-sequential accesses for I/D Bus accesses unless there is contention for that specific memory array
- DMA accesses to Main SRAM are always 0-wait state unless there is contention for that specific memory array
- Prefetching is used on the I/D Bus accesses to Main SRAM to minimize/eliminate wait-state bubbles. Prefetching can be enabled/disabled for I and/or D Bus accesses
- Arbitration logic for each SRAM instance allows one bus slave access to the SRAM on any given cycle.

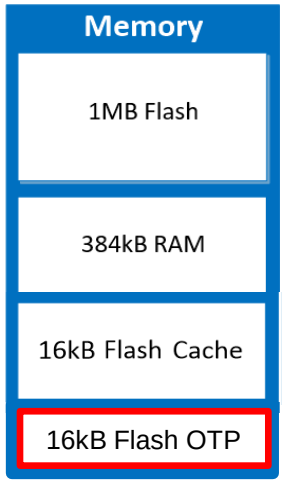


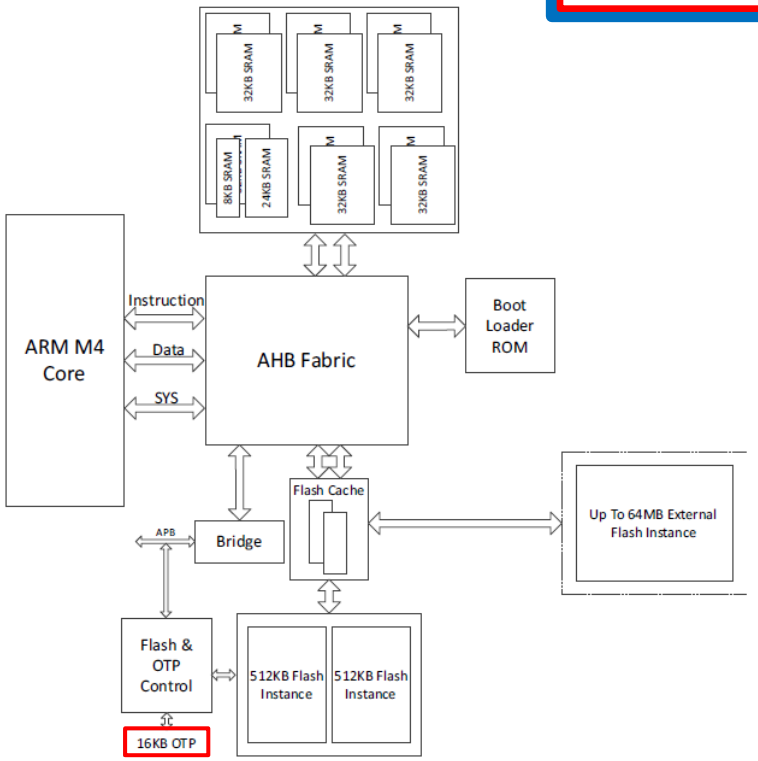




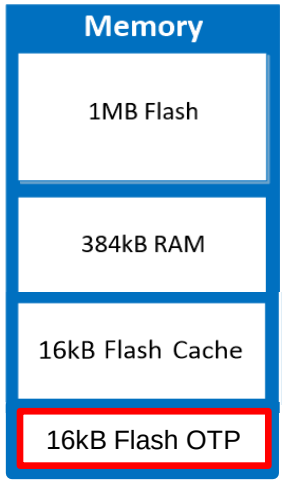
Memory: Flash OTP – INFO Space

- 16KB of Secure Flash “OTP”
- 8 KBytes contain factory preset chip trim values.
- 8 KBytes for customer use:
- Security
  - Secure Bootloader Configuration
  - Flash Protection
  - Debug Lockout
- Customer Options/Trims
  - Enable SIMO-Buck
  - Enable BLE
  - Enable BLE Buck
  - 32MHz XTAL Trim





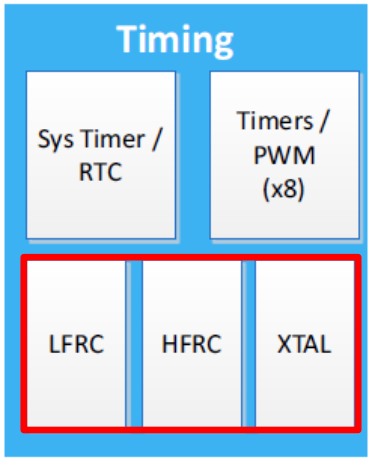
Memory: Flash OTP – INFO Space

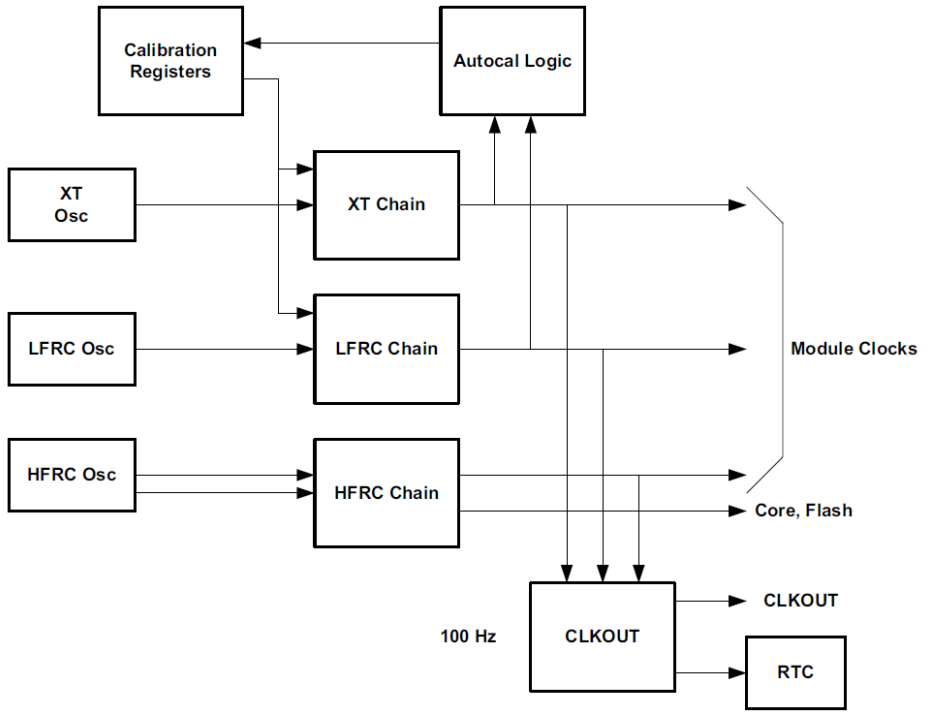


- Apollo3 EVBs ship with pre-configured customer INFO0 with these settings:
  - SIMO-Buck, BLE, and BLE Buck enabled
  - Secure Bootloader (SBL) set for non-secure mode
  - SBL configured to use UART at 115Kbaud and TX=GPIO22, RX=GPIO23 (which are connected to onboard USB-to-UART)
- Apollo3 parts ship with non-initialized customer INFO0
  - SIMO-Buck, BLE, and BLE Buck are disabled
  - SBL defaults to UART at 115Kbaud using GPIO

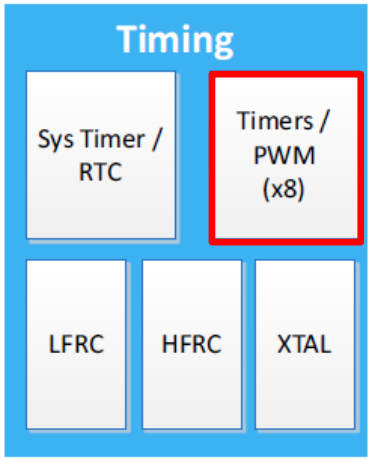
Timing: Clock Generation

- Multiple clock sources available for peripherals
  - All 3 sources can be divided down in most cases
- 32.768 kHz XTAL is most accurate, but requires crystal
- HFRC (High Freq. RC oscillator)
  - 48MHz or 96MHz
  - Consumes most power
  - 2% accurate at 25C across voltage (1.8V to 3.6V)
  - TBD accuracy across -40C to 85C
  - Autoadjust function continuously calibrates HFRC to XTAL to ensure < 1% error (<0.1% error at stable temp)
- LFRC (Low Freq. RC oscillator)
  - Nominally 1.024 kHz
  - Low power but inaccurate (25%+ error)
- Core and Flash only clocked via HFRC at 48MHz or 96MHz

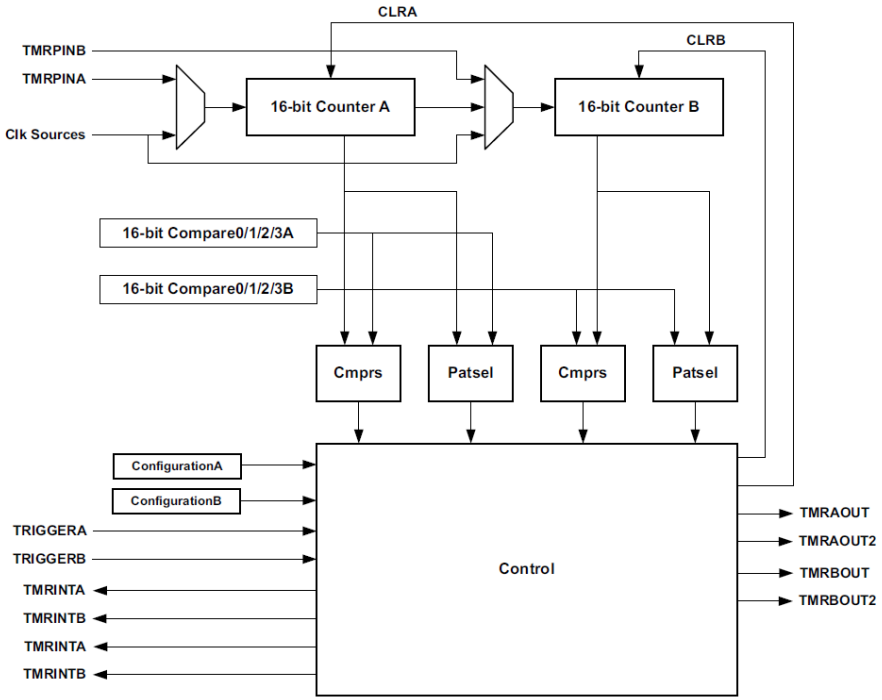




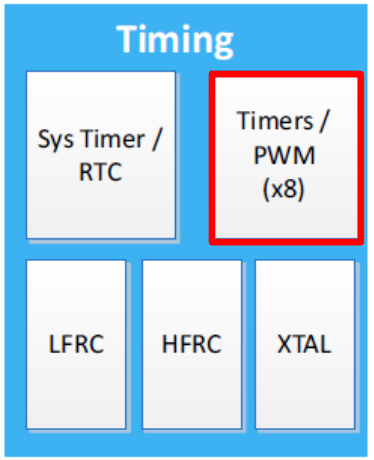
Timing: Counter/Timers - Ctimers



- Supports multiple clock sources
  - As fast as 12MHz (HFRC/4)
  - As slow as 1Hz (LFRC/1024)
- 8 total Ctimer Pairs
  - Up to 16, 16-bit timers
  - Up to 8, 32-bit timers
- 4 compare modules per Ctimer
- Standard Counter functionality:
  - Interrupt after a specified delay
  - Interrupt periodically with a specified period
  - Generate an external pulse of a specified width, after a configured delay
  - Generate an external PWM signal with a specified period and duty cycle

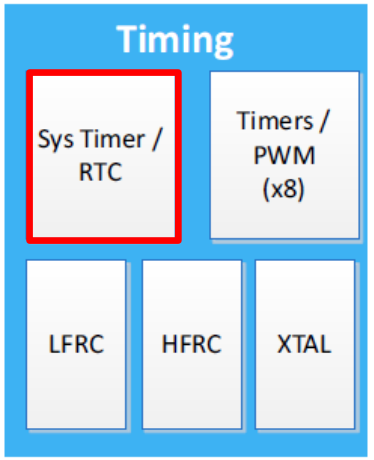


Timing: Counter/Timers - Ctimers



- Advanced Ctimer Features:
  - Arbitrary pattern generation
    - Up to 128-bits in HW register
    - Longer continuous pattern supported by updating when half of pattern register has been output (i.e. interrupt generated every 64-bits for MCU to service)
    - Timer-synchronization features so pattern outputs from multiple timers can be perfectly aligned
    - Applications include stepper motor control, streaming serial data such as PDM audio output, etc.
  - Alternating PWM pulse output (can be used as double-buffered PWM)
    - Improved PWM “DAC” output for LED dimming, PWM audio output, etc.
  - Timers can select the output of other Ctimers as their clock source (in addition to LFRC, XT, and HFRC derived clock sources)

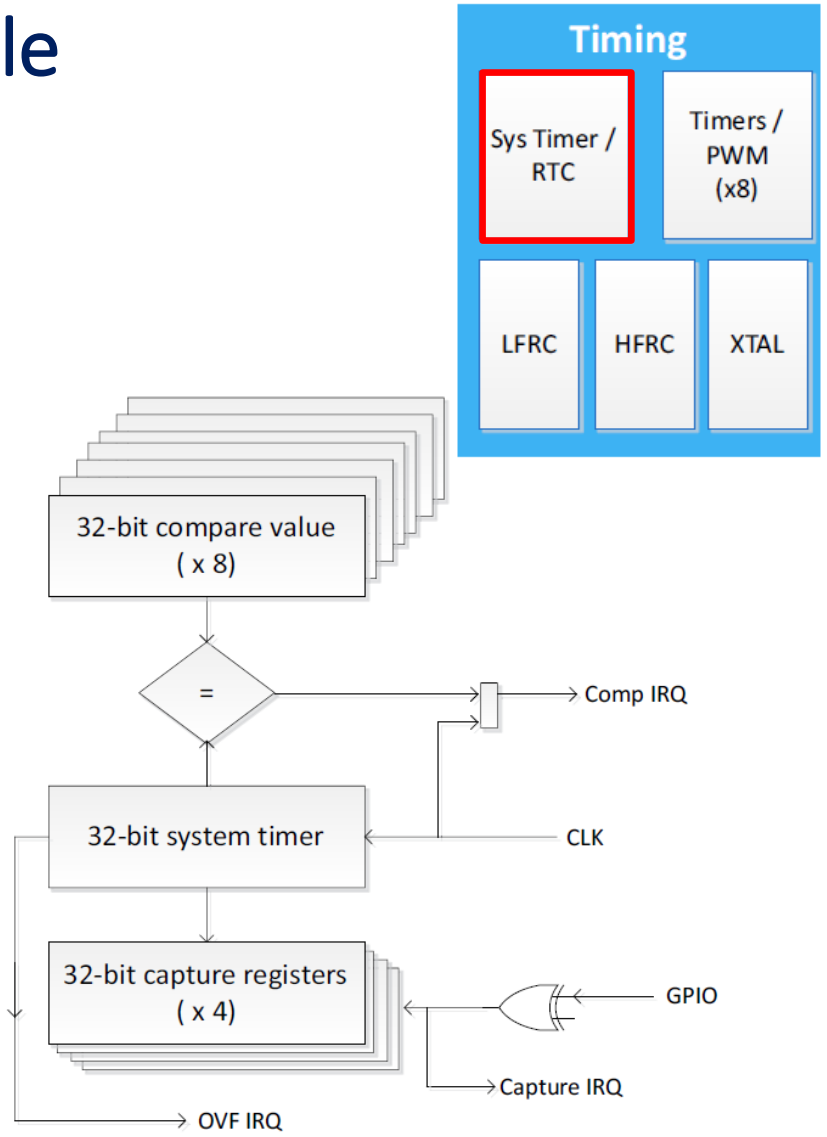
Timing: Real Time Clock (RTC) Module



- Same RTC IP as AMx8x5 devices
- Clocked from XTAL or LFRC
- 100th of a second resolution (10ms)
- Automatic leap year calculation
- Programmable alarm interrupts
  - Every 100th sec., 10th sec., sec., min., hour, day, week, month, or year
- Continues to operate through all resets except POA power-on reset which occurs at TBD voltage (~1.3V) so time is retained through all other resets including brownout

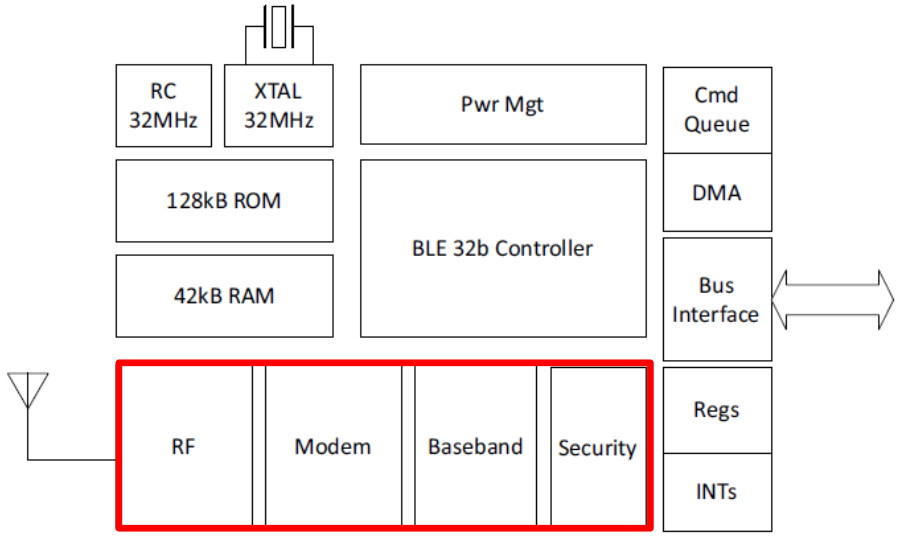
Timing: System Timer (Stimer) Module

- 32bit System Timer
- Clocked from XTAL, LFRC, or HFRC/16
- 8x 32bit compare registers with interrupts
- Offsets from “NOW” are written to compare registers and compare register value is determined by HW
- Only reset by POA (Power On Analog - system cold reset). Retains time across all POI and POR (system warm reset) events except full power cycle.
- Contains three 32-bit NVRAM registers that are only reset by POA



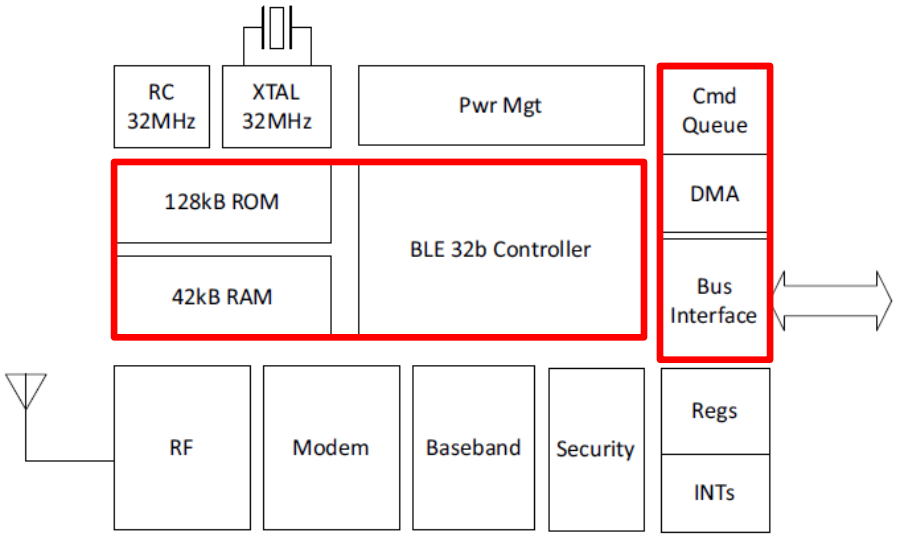
Bluetooth Low Energy BLE 5

- Bluetooth 5 Compliant (QDID: 115953)
  - Secure connection (AES-128 HW Encryption)
  - Extended packet length support
  - Up to eight simultaneous connections
- -93 dBm sensitivity
- -20 to +4 dBm TX output power range
- Power amplifier controls enable higher TX power with external PA
- Single ended output
  - Integrated Balun and antenna matching network



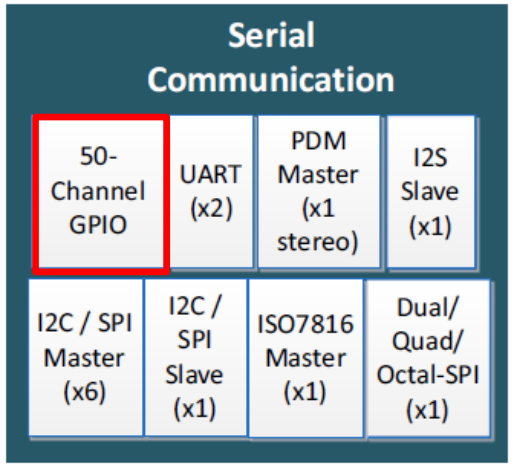
Bluetooth Low Energy BLE 5

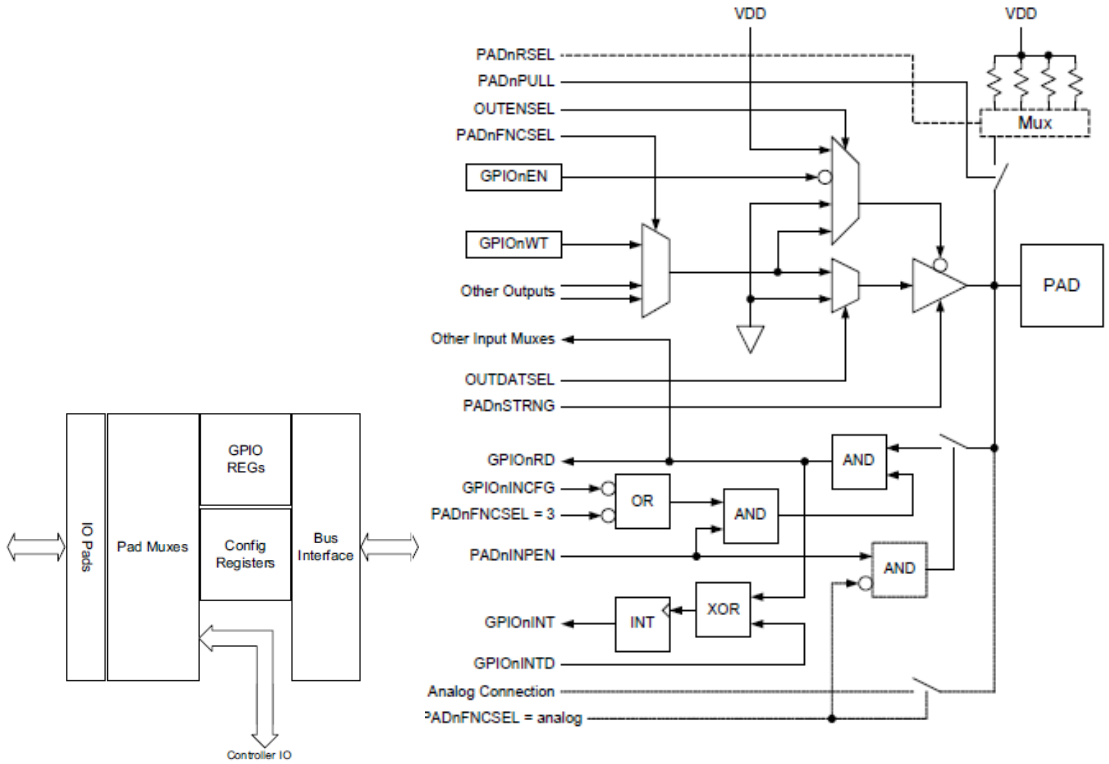
- Dedicated 32bit processor for BLE Controller
  - 128K ROM and 42K RAM
- BLE Controller Stack runs on BTLE controller
- HCI interface to main processor.
  - HCI interface has FIFO, DMA, and command queue to minimize interruption of host processor
- Cordio-B50 BLE 5 Compliant Host Stack (QDID: 91368) runs on main CM4 processor
- Basic application including FreeRTOS, BLE Host Stack, plus basic BLE profile such as HRM requires approximately 80K Flash and 35K SRAM



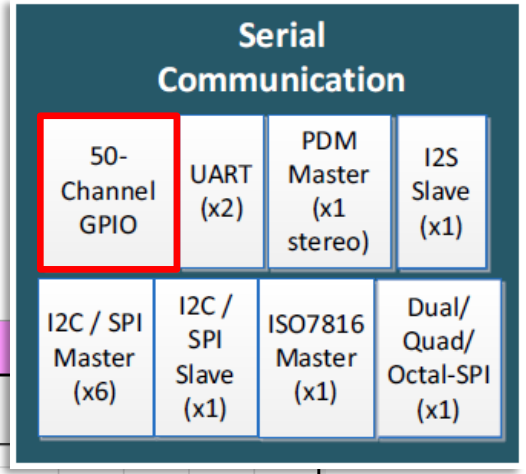
Serial Communication: GPIO

- 50 GPIO on BGA, 37 GPIO on CSP
- Configurable
  - Tristate, Open Drain, or Push Pull
  - Configurable drive strength or 2, 4, 8, or 12mA
  - Many pin function mapping options
- Integrated pull up/down
- 3 power GPIOs (2 source, 1 sink)
  - Each can support up to a 50mA continuous load





Serial Communication: GPIO

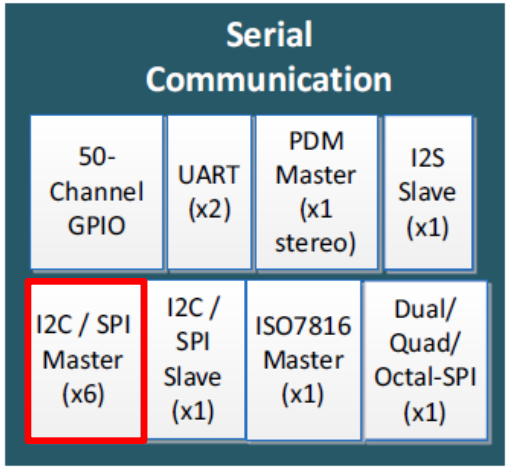


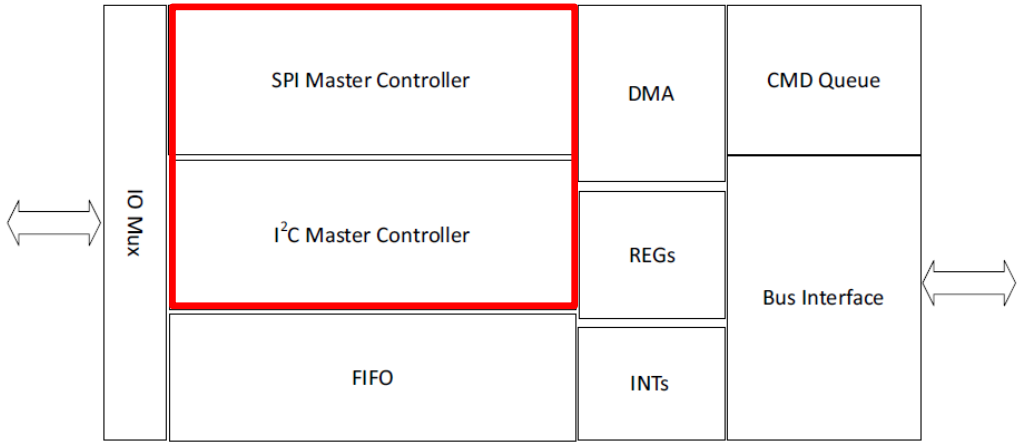
- Flexible Pin-Function mapping:

	Pad Function Select Number (PADnFNCSEL)										NCE Chip Select Mux				CT CTimer Input Selection							
Pad	0	1	2	3	4	5	6	7	CSP PKG	Max Drive Streng	0	1	2	3	0	1	2					
0	SLSCL	SLSCK	CLKOUT	GPIO00	-	MSPI4	-	NCE0	X	12mA	M3.2	M4.2	M5.2	M1.3								
1	SLSDAWIR3	SLMOSI	UART0TX	GPIO01	-	MSPI5	-	**NCE1**	X	12mA	M0.2	M1.2	M2.2	MSPI.0								
2	UART1RX	SLMISO	UART0RX	GPIO02	-	MSPI6	-	NCE2	X	12mA	M3.3	M4.3	M5.3	M2.1								
3	UA0RTS	SLnCE	NCE3	**GPIO03"**	-	MSPI7	TRIG1	I2S_WCLK	X	12mA	M3.0	M4.0	M5.0	M2.0								
4	UA0CTS	SLINT	NCE4	GPIO04	-	UART1RX	CT17	MSPI2	X	12mA	M3.1	M4.1	M5.1	M1.1		A4	A4OUT2	B7OUT	A4OUT	A1OUT2	A6OUT2	A7OUT2
5	M0SCL	**M0SCK**	UA0RTS	GPIO05	-	-	-	CT8	X	12mA	-	-	-	-	A2		A2OUT	A3OUT2	A4OUT2	B6OUT	A6OUT2	A7OUT2
6	M0SDAWIR3	**M0MISO**	UA0CTS	GPIO06	-	CT10	-	I2S_DAT	X	12mA	-	-	-	-	B2		B2OUT	B3OUT2	B4OUT2	A6OUT	A6OUT2	A7OUT2
7	NCE7	**M0MOSI**	UA0SCLK	GPIO07	TRIG0	UART0TX	-	CT13	X	12mA	M3.1	M4.1	M5.1	MSPI.0		B4	B4OUT2	A2OUT	B4OUT	B1OUT2	A6OUT2	A7OUT2
8	M1SCL	M1SCK	NCE8	GPIO08	SCCCLK	-	UART1TX	-	X	12mA	M3.0	M4.0	M5.0	M0.0								
9	M1SDAWIR	M1MISO	NCE9	GPIO09	SCCIO	-	UART1RX	-	X	12mA	M3.3	M4.3	M5.3	M2.3								
10	UART1TX	M1MOSI	NCE10	GPIO10	PDM_CLK	UA1RTS	-	-	X	12mA	M3.2	M4.2	M5.2	MSPI.0								
11	ADCSE2	NCE11	**CT31**	GPIO11	SLINT	UA1CTS	UART0RX	PDM_DATA	X	12mA	M0.0	M1.0	M2.0	M3.0		B7	B7OUT2	A6OUT	B7OUT	B3OUT2	A6OUT2	A7OUT2
12	ADCD0NSE3	NCE12	**CT0**	GPIO12	SLnCE	PDM_CLK	UA0CTS	UART1TX	X	12mA	M3.0	M4.0	M5.0	MSPI.1	A0		A0OUT	B2OUT2	A5OUT2	A6OUT	A6OUT2	A7OUT2
13	ADCD0PSE8	NCE13	CT2	GPIO13	I2S_BCLK		UA0RTS	UART1RX	X	12mA	M3.1	M4.1	M5.1	M0.1	B0		B0OUT	B1OUT2	B6OUT2	A7OUT	A6OUT2	A7OUT2
14	ADCD1P	NCE14	UART1TX	GPIO14	PDM_CLK		SWDCK	32KHz_XT	X	12mA	M0.2	M1.2	M2.2	M4.2								
15	ADCD1N	NCE15	UART1RX	GPIO15	PDM_DATA		SWDIO	SWO	X	12mA	M0.3	M1.3	M2.3	MSPI.0								
16	ADCSE0	NCE16	TRIG0	GPIO16	SCCRST	CMPIN0	UART0TX	UA1RTS	X	12mA	M0.0	M1.0	M2.0	M5.0								
17	CMPRF1	NCE17	TRIG1	GPIO17	SCCCLK	-	UART0RX	UA1CTS	X	12mA	M0.1	M1.1	M2.1	M4.1								
18	CMPIN1	NCE18	CT4	GPIO18	UA0RTS		UART1TX	SCCIO	X	12mA	M0.2	M1.2	M2.2	M3.2	A1		A1OUT	A2OUT2	A5OUT2	B5OUT	A6OUT2	A7OUT2
19	CMPRF0	NCE19	CT6	GPIO19	SCCCLK		UART1RX	I2S_BCLK	X	12mA	M0.3	M1.3	M3.3	MSPI.0	B1		B1OUT	A1OUT	B5OUT2	B7OUT	A6OUT2	A7OUT2
20	**SWDCK**	NCE20	-	GPIO20	UART0TX	UART1TX	I2S_BCLK	UA1RTS	X	4mA	M3.1	M4.1	M5.1	M2.1								
21	**SWDIO**	NCE21	-	GPIO21	UART0RX	UART1RX	SCCRST	UA1CTS	X	12mA	M3.2	M4.2	M5.2	M2.2								
22	UART0TX	NCE22	CT12	GPIO22	PDM_CLK		MSPI0	SWO	X	12mA	M3.3	M4.3	M5.3	M0.3	A3		A3OUT	B1OUT	B0OUT2	B6OUT2	A6OUT2	A7OUT2
23	UART0RX	NCE23	CT14	GPIO23	I2S_WCLK	CMPOUT	MSPI3	-	X	12mA	M0.0	M1.0	M2.0	M4.0	B3		B3OUT	B1OUT	B7OUT2	A7OUT	A6OUT2	A7OUT2
24	UART1TX	NCE24	MSPI8	GPIO24	UA0CTS	CT21	32KHz_XT	SWO	X	12mA	M0.1	M1.1	M2.1	M5.1		A5	A5OUT2	A1OUT	B5OUT	A0OUT2	A6OUT2	A7OUT2
25	UART1RX	NCE25	CT1	GPIO25	M2SDAWIR3	M2MISO	-	-	X	12mA	M3.2	M4.2	M5.2	M0.2		A0	A0OUT2	A0OUT	A5OUT	B7OUT2	A6OUT2	A7OUT2
26		NCE26	CT3	GPIO26	SCCRST	MSPI1	UART0TX	UA1CTS	X	12mA	M3.3	M4.3	M5.3	M1.3		B0	B0OUT2	B0OUT	A1OUT	A6OUT	A6OUT2	A7OUT2
27	UART0RX	NCE27	CT5	GPIO27	M2SCL	M2SCK	-	-	X	12mA	M3.0	M4.0	M5.0	M1.0		A1	A1OUT2	A1OUT	B6OUT	A7OUT	A6OUT2	A7OUT2
28	I2S_WCLK	NCE28	CT7	GPIO28	-	M2MOSI	UART0TX	-	X	12mA	M3.1	M4.1	M5.1	MSPI.0		B1	B1OUT2	B1OUT	B5OUT	A7OUT	A6OUT2	A7OUT2
29	ADCSE1	NCE29	CT9	GPIO29	UA0CTS	UA1CTS	UART0RX	PDM_DATA	X	12mA	M3.2	M4.2	M5.2	M1.2		A2	A2OUT2	A2OUT	A4OUT	B0OUT	A6OUT2	A7OUT2
30	-	NCE30	CT11	GPIO30	UART0TX	UA1RTS		I2S_DAT		12mA	M3.3	M4.3	M5.3	M0.3		B2	B2OUT2	B2OUT	B4OUT	B5OUT2	A6OUT2	A7OUT2
31	ADCSE3	NCE31	CT13	GPIO31	UART0RX	SCCCLK		UA1RTS		12mA	M0.0	M1.0	M2.0	M4.0		A3	A3OUT2	A3OUT	A6OUT	B4OUT2	A6OUT2	A7OUT2
32	ADCSE4	NCE32	CT15	GPIO32	SCCIO			UA1CTS		12mA	M0.1	M1.1	M2.1	MSPI.1		B3	B3OUT2	B3OUT	A7OUT	A4OUT2	A6OUT2	A7OUT2
33	ADCSE5	NCE33	32KHz_XT	GPIO33		UA0CTS	CT23	SWO		12mA	M0.2	M1.2	M2.2	M5.2		B5	B5OUT2	A7OUT	A5OUT	B0OUT2	A6OUT2	A7OUT2
34	ADCSE6	NCE34	UA1RTS	GPIO34	CMPRF2	UA0RTS	UART0RX	PDM_DATA		12mA	M0.3	M1.3	M2.3	M3.3								
35	ADCSE7	NCE35	UART1TX	GPIO35	I2S_DAT	CT27	UA0RTS			12mA	M0.0	M1.0	M2.0	M3.0		B6	B6OUT2	A1OUT	B6OUT	B2OUT2	A6OUT2	A7OUT2
36	TRIG1	NCE36	UART1RX	**GPIO36"**	32KHz_XT	UA1CTS	UA0CTS	PDM_DATA		12mA	M3.1	M4.1	M5.1	MSPI.1								
37	TRIG2	NCE37	UA0RTS	**GPIO37"**	SCCIO	UART1TX	PDM_CLK	CT29		12mA	M3.2	M4.2	M5.2	M0.2		A7	B5OUT2	A1OUT	A7OUT	A3OUT2	A6OUT2	A7OUT2
38	TRIG3	NCE38	UA0CTS	GPIO38	-	M3MOSI	UART1RX	-		12mA	M0.3	M1.3	M2.3	M5.3								
39	UART0TX	UART1TX	CT25	GPIO39	M4SCL	M4SCK	-	-	X	12mA	-	-	-	-		A6	B4OUT2	B2OUT	A6OUT	A2OUT2	A6OUT2	A7OUT2
40	UART0RX	UART1RX	TRIG0	GPIO40	M4SDAWIR3	M4MISO	-	-	X	12mA	-	-	-	-								
41	NCE41		SWO	**GPIO41"**	I2S_WCLK	UA1RTS	UART0TX	UA0RTS	X	12mA	M0.1	M1.1	M2.1	MSPI.1								
42	UART1TX	NCE42	CT16	GPIO42	M3SCL	M3SCK	-	-		12mA	M0.0	M1.0	M2.0	M5.0	A4		A4OUT	A0OUT	A0OUT2	B3OUT2	A6OUT2	A7OUT2
43	UART1RX	NCE43	CT18	GPIO43	M3SDAWIR3	M3MISO	-	-		12mA	M0.1	M1.1	M2.1	MSPI.1	B4		B4OUT	B0OUT	A0OUT	A3OUT2	A6OUT2	A7OUT2

Serial Communication: I/O Masters (IOM)

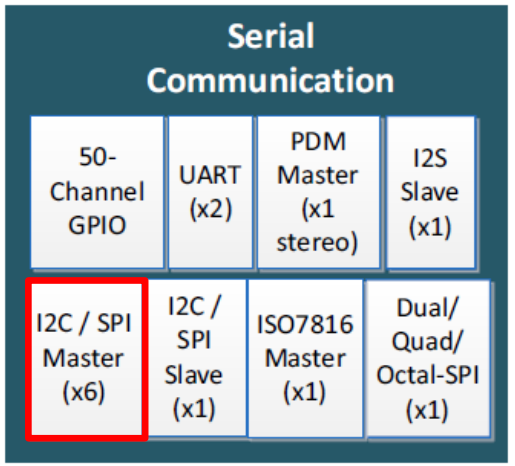
- 6 total IOMs (I/O Masters) available
  - Each can be configured for SPI or I2C
- I2C mode
  - Supports 7 and 10-bit addressing
  - Multi-master arbitration
  - 100KHz, 400KHz, and 1MHz
  - Integrated pull-up resistors
- SPI mode
  - 8 Chip Selects per IOM
  - 3 and 4-wire modes
  - Up to 24 MHz
  - Supports all 4 standard SPI modes
  - Standard embedded address (command byte) operations
  - Also supports raw read/write operations

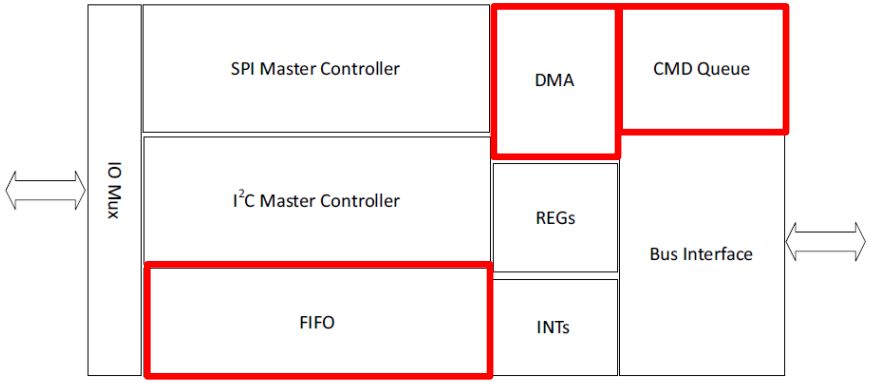




Serial Communication: I/O Masters

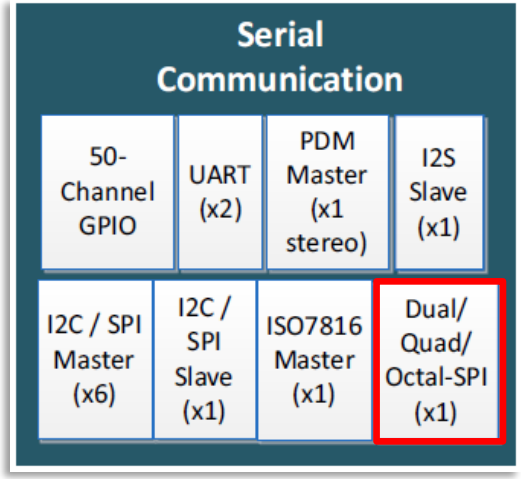
- Each IOM contains independent Read and Write FIFOs of 32Bytes
- Each IOM has a DMA controller that supports IOM to SRAM, and SRAM/Flash to IOM transfers
- Each IOM supports command queues which can schedule multiple transactions to occur without CPU intervention.
  - Used in combination with DMA.
- CPU can go to sleep while IOM is performing direct reads/writes to/from FIFO or transferring data by way of DMA

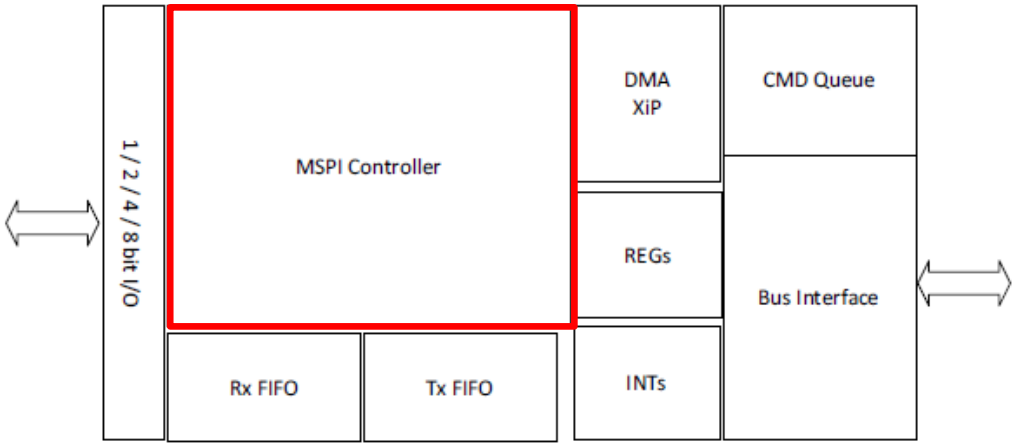




Serial Communication: MSPI

- One MSPI Master Module
- Supports Serial, Dual, Quad, and Octal modes
- 2 Chip Selects
- Up to 24 MHz Clock
- Supports all 4 standard SPI modes





Serial Communication: MSPI

- Unified 16-entry FIFO (32 bits wide) for reads and writes
- DMA Support
  - Simple DMA model where software sets internal (SRAM or flash) address and external device address, transfer direction, and transfer size
  - MSPI DMA controller automatically handles sequencing of instructions and address to serial flash device.
  - Software configures registers to specify device read/write command bytes and address bytes (1 to 4).
- Command Queue
  - Software can construct a buffer of operations and MSPI w execute the series of operations autonomously
  - Used in combination with DMA

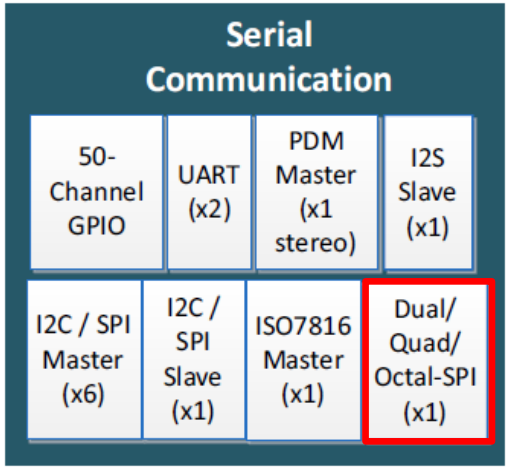
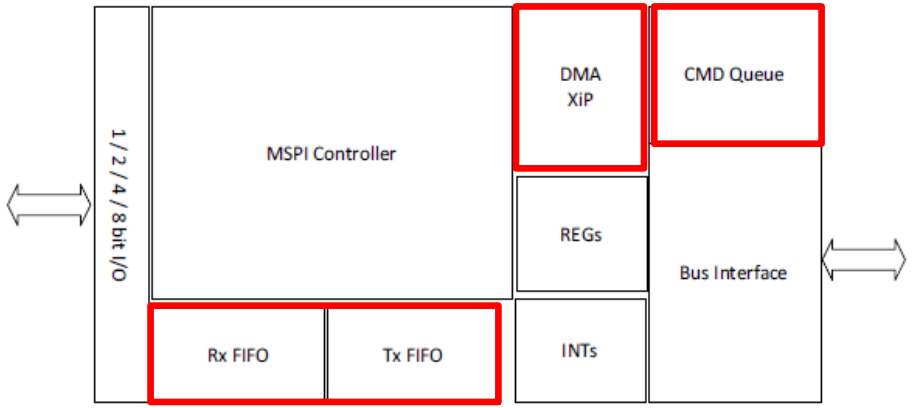


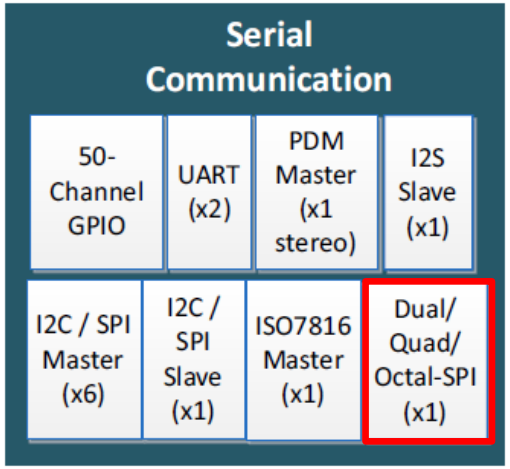
Table 363: FLASH Register

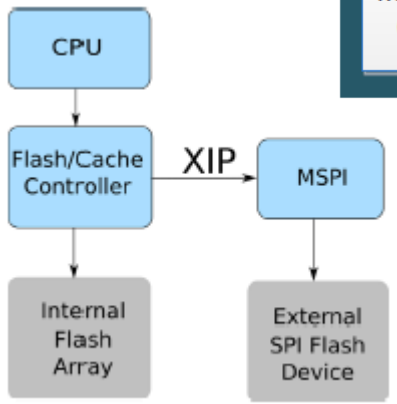
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
READINSTR								WRITEINSTR								RSVD					XIPMIXED			XIPSENDI	XIPSENDA	XIPENTURN	XIPBIGENDIAN	XIPACK		RSVD	XIPEN

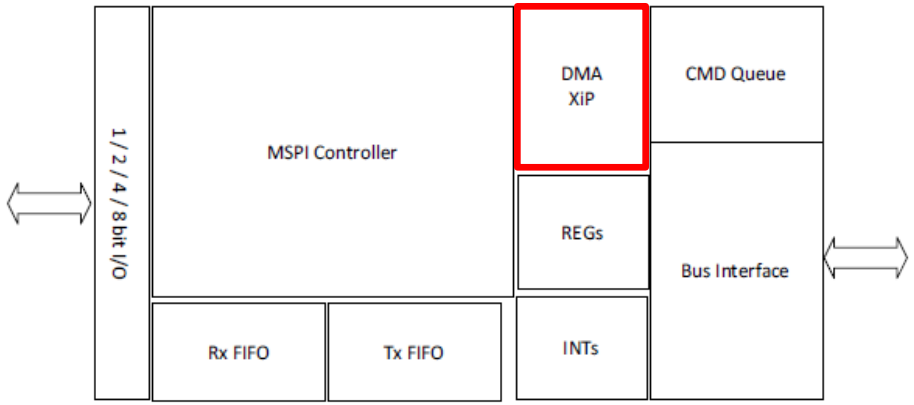


Serial Communication: MSPI

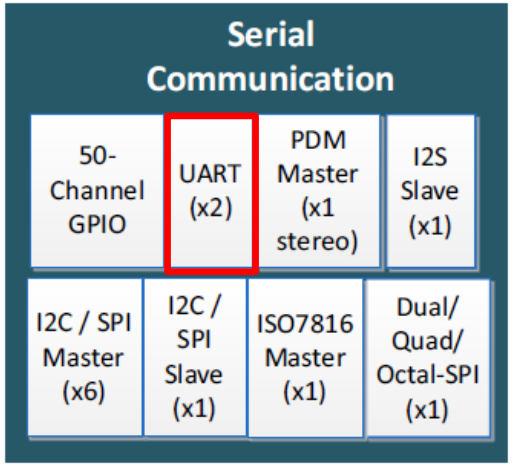
- MSPI supports Execute in Place (XIP) Operations
- MSPI connected devices can be mapped into flash cache's address space and appear as extension to the internal flash. The flash/cache module will decode the address region and forward operations to the MSPI interface for completion.
- XIP and DMA/PIO operations can be interleaved. MSPI controller will allow current operation to complete before performing the XIP operation.
  - Exception: XIP mode may have to be disabled during flash programming operations.



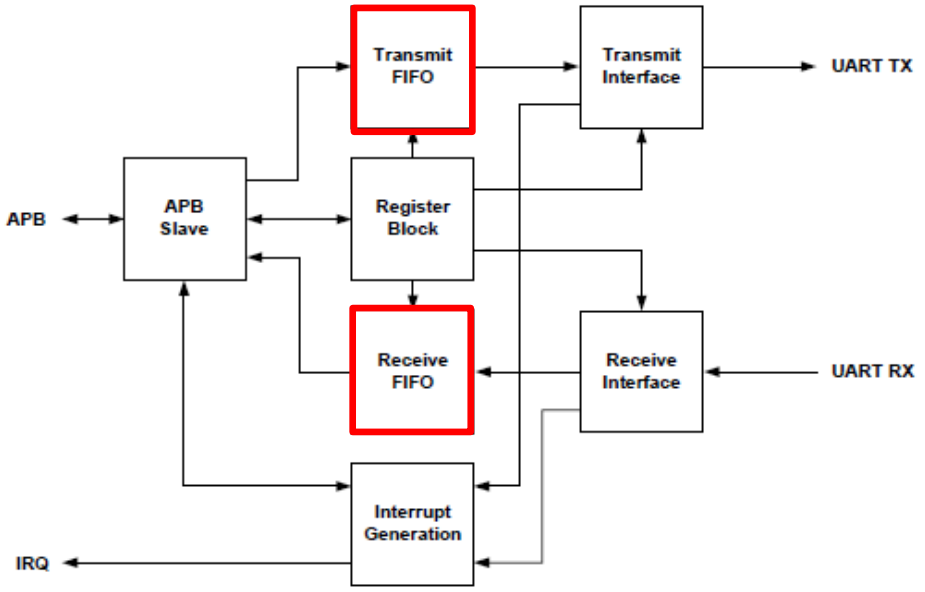




Serial Communication: UART

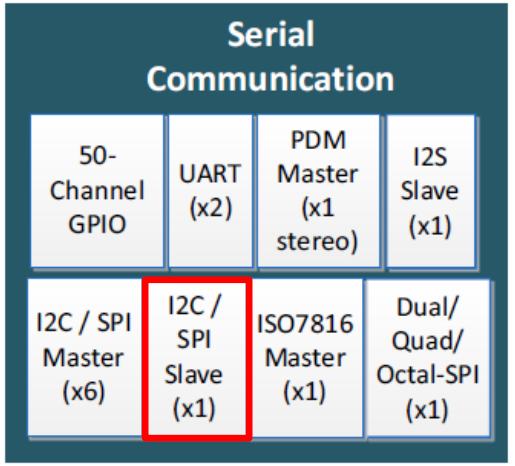


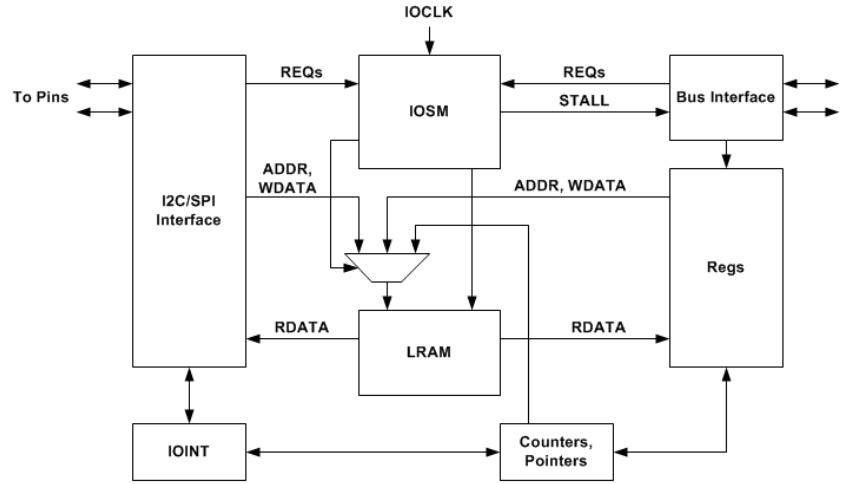
- 2 UARTs
  - MCU can enter **sleep mode** during transfers
  - 32Byte Transmit and 32Byte receive FIFOs reduce MCU active time
- Configurable baud rate generator
  - Maximum rate of 921,600 bps
- Highly programmable
  - Data size, parity, and stop bit length
  - Hardware flow control
  - Full-duplex and half-duplex modes
- Loopback functionality for diagnostics and testing



Serial Communication: I/O Slave

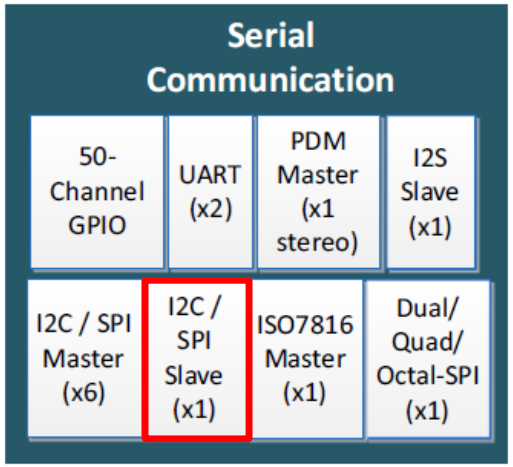
- 1 IOS (I/O Slave)
  - I2C or SPI mode
- I2C mode:
  - configurable 7 and 10-bit addressing
  - interface freq. up to 1.2 MHz
- SPI mode:
  - Supports all polarity/phase combinations
  - interface freq. up to TBD MHz

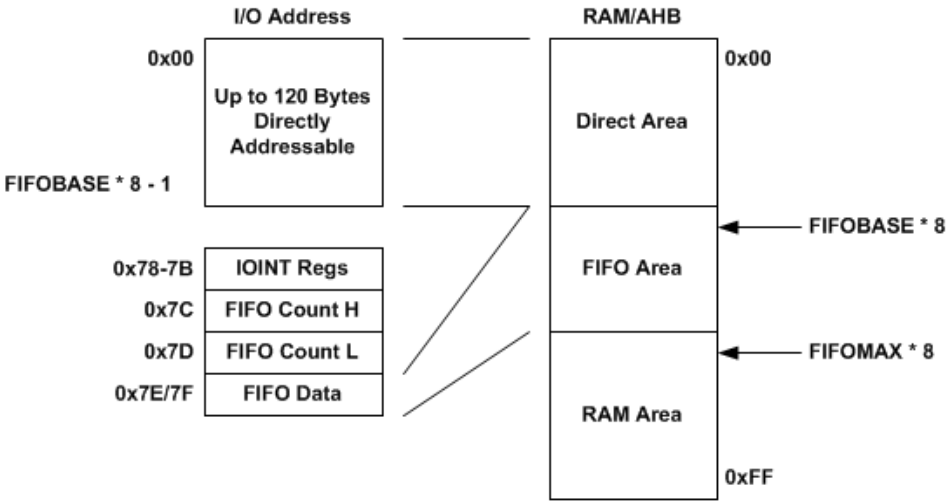




Serial Communication: I/O Slave

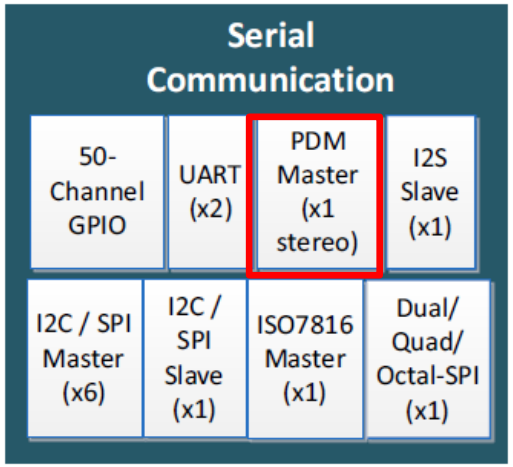
- IOS LRAM is 256 bytes
- Broken up into 3 sections:
  1. Directly addressable RAM up to 120 Bytes which can be accessed by external IOM host while MCU is asleep
  2. Status and Config Registers & FIFO. FIFO size up to 256 Bytes
  3. Any LRAM not configured as direct access or FIFO is left as RAM accessible by Apollo SW only

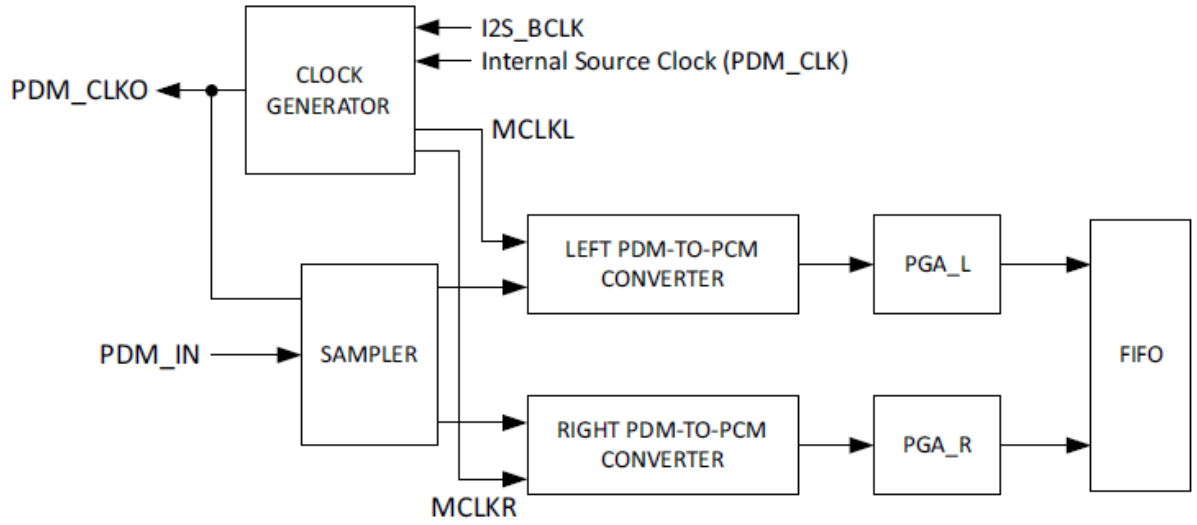




PDM Master Interface

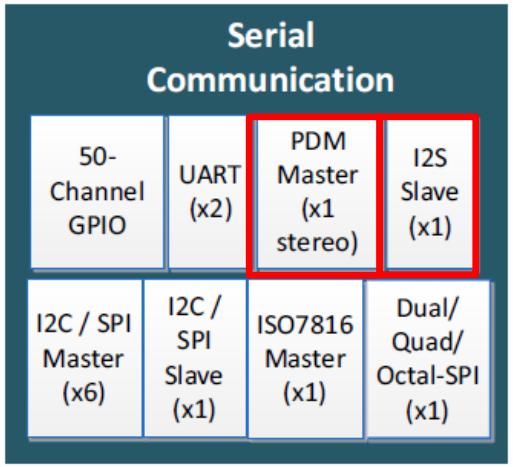
- Stereo or mono PDM input, with variable PDM output clock rates (750-768kHz, 1.5-1.536MHz, 3-3.072MHz
- Hardware performs 64x Decimation of PDM bitstream input to 16bit PCM
- 32 Sample FIFO
- DMA can efficiently transfer audio samples from FIFO to SRAM

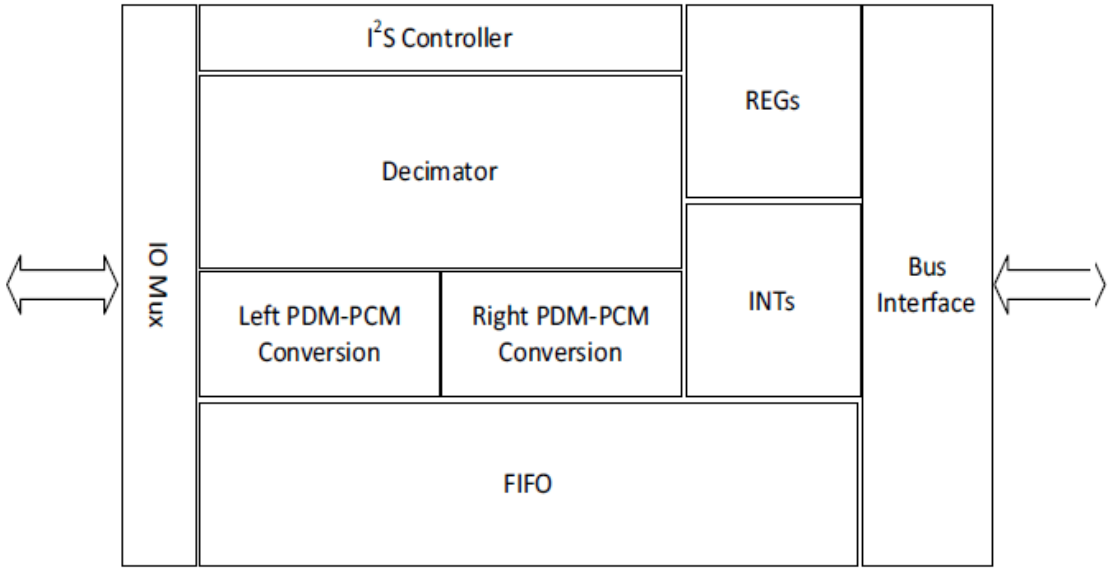




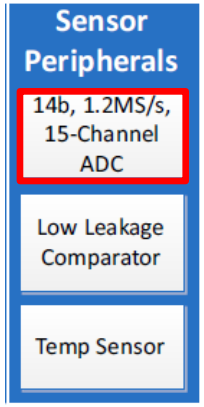
I2S Slave Interface

- I2S Slave interface is limited to direct pass-through output of audio data from PDM input (after PDM-to-PCM conversion)
- Audio data from PDM input can be simultaneously buffered in FIFO (for use by MCU) and output on I2S
- I2S does not support audio input, or output of arbitrary audio from MCU core

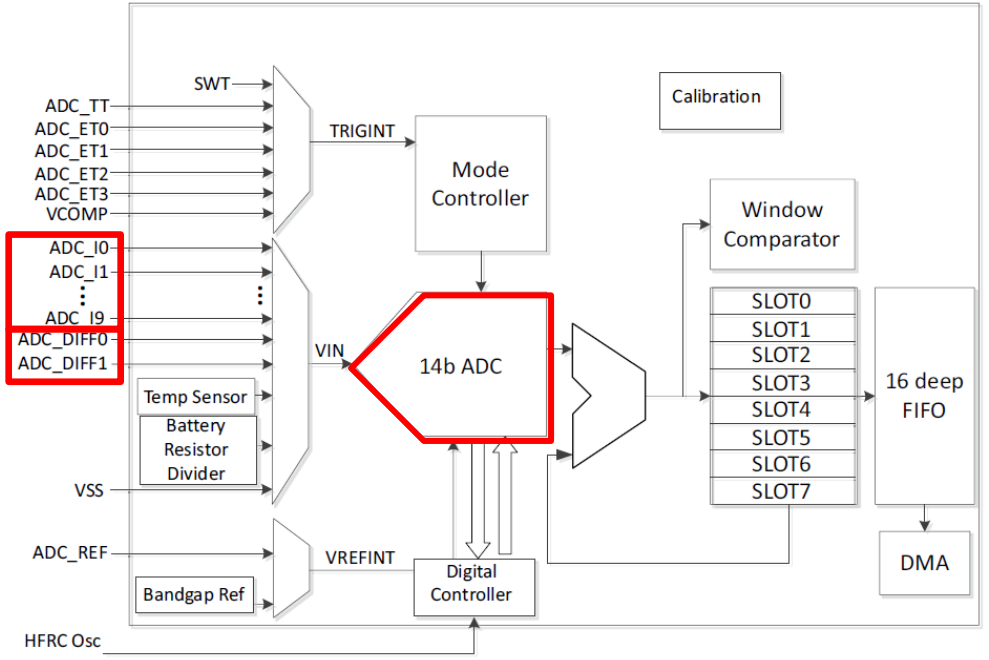




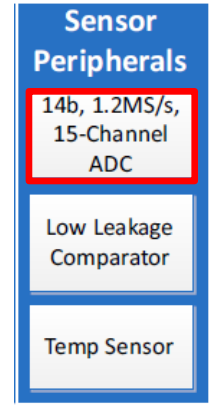
Sensor Peripherals: ADC



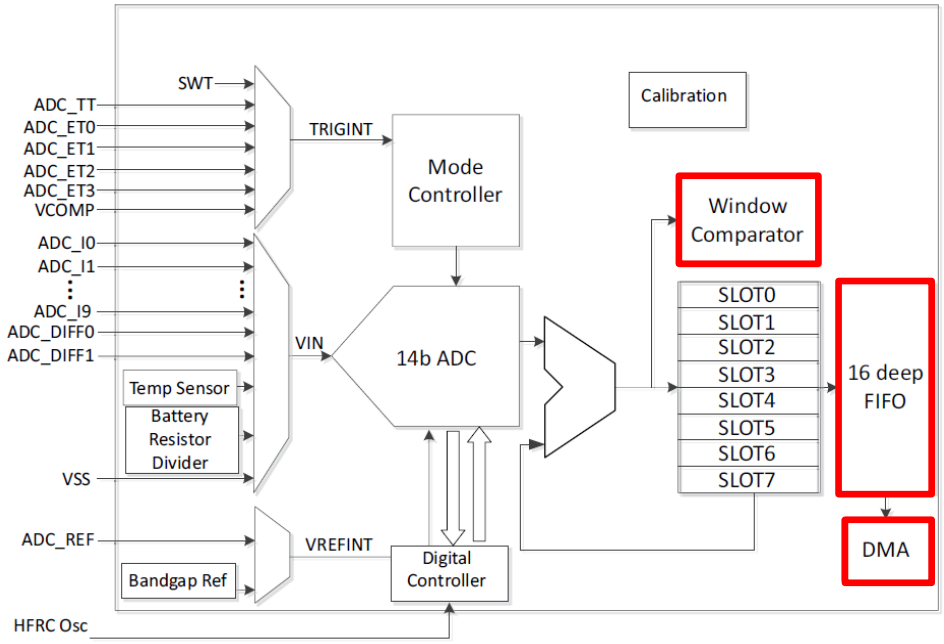
- 14-bit SAR architecture (successive approximation register)
- 10 Single-ended and 2 Differential external inputs
- 3 internal inputs: VSS, Temp Sensor, and VDD/3
- On-chip bandgap or external reference voltage (2.0V or 1.5V)
- Single shot, repeating single shot, scan, and repeating scan modes
- User-selectable clock source for variable sampling rates



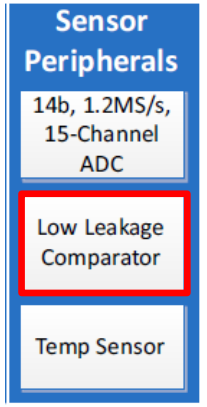
Sensor Peripherals: ADC



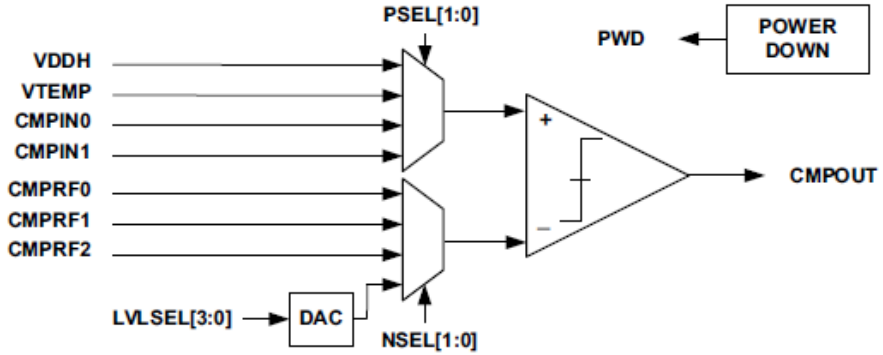
- Multiple conversion triggers: External pins, Ctimer, SW trigger
- Window comparator for monitoring voltage excursions into or out of selectable thresholds
- 16-entry FIFO and DMA for storing measurement results and maximizing MCU sleep time
- Multiple low power modes
  - Selectively shut down portions of the ADC between conversions
- Sample rate up to 1.2Msps at 14bit and up to 2.8Msps at 8bit
- Built-in accumulate and scale module
  - Automatically accumulate up to 128 samples (Per-slot 21bit accumulation register)
  - Scaling capability for automated averaging



Sensor Peripherals: Voltage Comparator

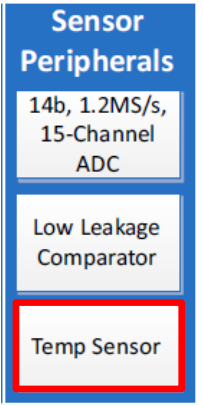


- Interrupt and register access to comparator output
- If V_+ rises above or falls below threshold: generates interrupt
- Programmable compare threshold:
  - 4-bit DAC
  - 3 different external pins
- Power consumption TBD (~2µA)



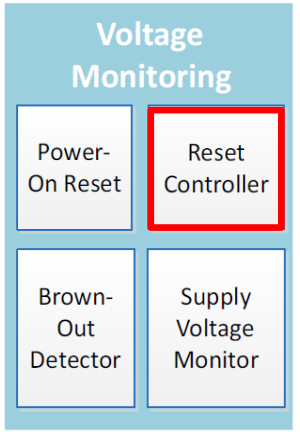
0P58V = 0x0 - Set Reference input to 0.58 Volts.
0P77V = 0x1 - Set Reference input to 0.77 Volts.
0P97V = 0x2 - Set Reference input to 0.97 Volts.
1P16V = 0x3 - Set Reference input to 1.16 Volts.
1P35V = 0x4 - Set Reference input to 1.35 Volts.
1P55V = 0x5 - Set Reference input to 1.55 Volts.
1P74V = 0x6 - Set Reference input to 1.74 Volts.
1P93V = 0x7 - Set Reference input to 1.93 Volts.
2P13V = 0x8 - Set Reference input to 2.13 Volts.
2P32V = 0x9 - Set Reference input to 2.32 Volts.
2P51V = 0xA - Set Reference input to 2.51 Volts.
2P71V = 0xB - Set Reference input to 2.71 Volts.
2P90V = 0xC - Set Reference input to 2.90 Volts.
3P09V = 0xD - Set Reference input to 3.09 Volts.
3P29V = 0xE - Set Reference input to 3.29 Volts.
3P48V = 0xF - Set Reference input to 3.48 Volts.

Sensor Peripherals: Temperature Sensor



- Built-in sensor, accessible via ADC channel or Comparator
- ± 3˚C accuracy (if calibrated)
- 3.8mV/C sensor slope
- 3 calibration values needed
  - Offset
  - Voltage
  - Temp. during calibration

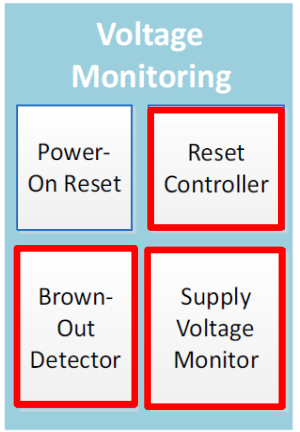
Reset Controller



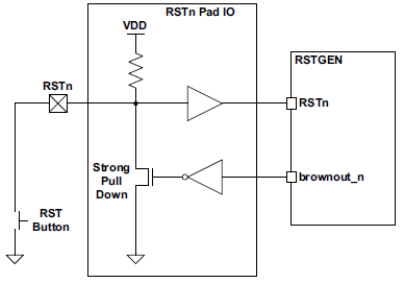
- Three levels of Reset
  - POR = POR Software Reset = HRESET = SYSRESETn
  - POI = POI Software Reset
  - POA = Power-on Reset
- Most resets trigger POR reset, which is the shallowest Reset
- POI Software reset is slightly deeper reset that triggers INFO space settings to be reloaded from Flash
- POA is the deepest reset, and is only triggered by voltage going below POA voltage (~1.3V – see datasheet for the exact voltage)

Reset Level	CPU	GPIO	INFO Settings (Trims, Options, and Security)	Peripherals (Except XT, LFRC, RTC, and Stimer)	XT, LFRC, RTC, and Stimer
POR (HRESET/SYSRESETn)	Reset	Reset	Not Reset	Reset	Not Reset
POI	Reset	Reset	Reset	Reset	Not Reset
Power-on Reset (POA)	Reset	Reset	Reset	Reset	Reset

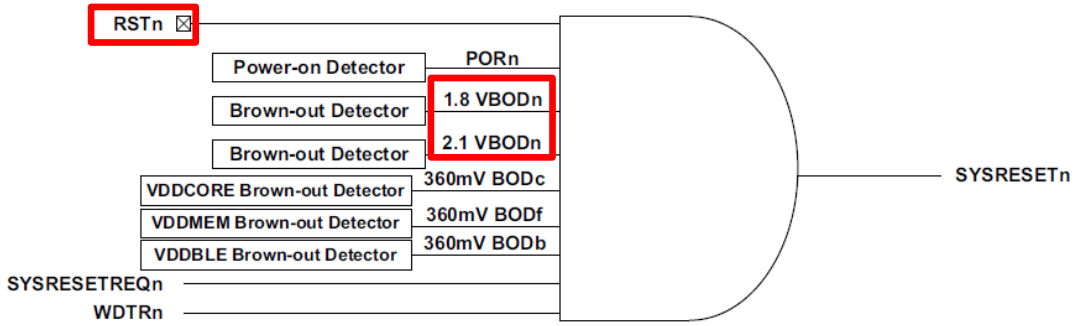
Reset: Voltage Monitoring and nRST pin



- BOD Reset max threshold 1.755V
- Optional BODH 2.1V brownout configurable for Reset or Interrupt
- External RSTn pin has built-in weak pull-up resistor
- RSTn pin is driven low when brownout is detected



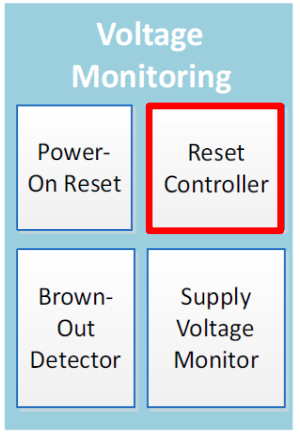
RSTn Pin

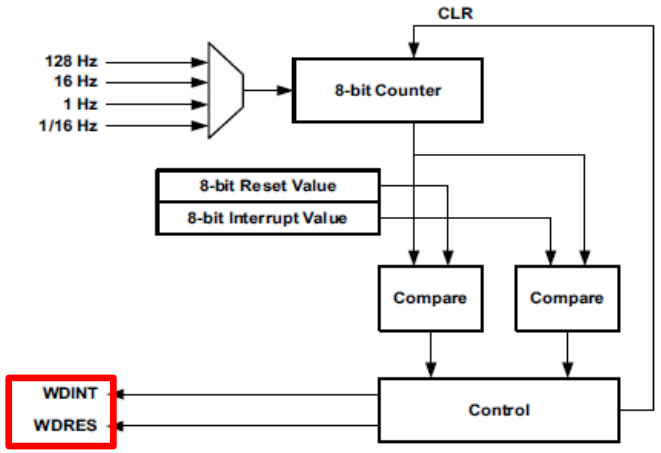


SYSRESET Sources

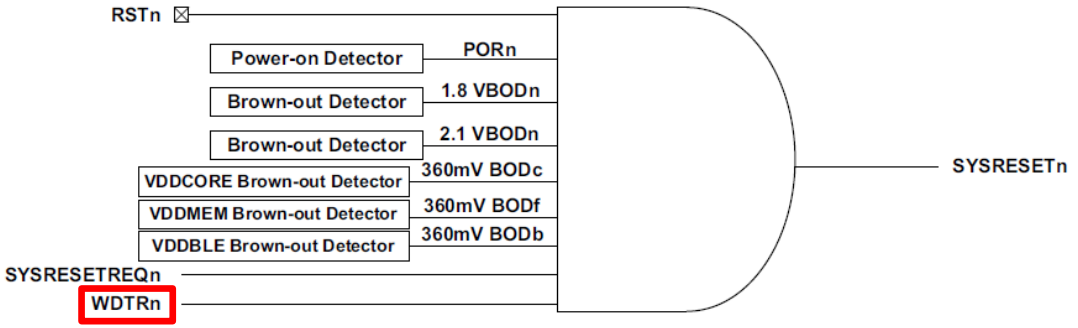
Reset: Watchdog Timer

- WDT (watchdog timer)
  - Clocked from LFRC with divider options from 1/16Hz to 128Hz
  - Two configurable WDT 8-bit register compare values:
    - One compare for Interrupt
    - One compare for Reset



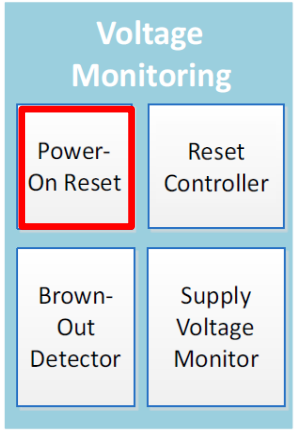


Watchdog Timer



SYSRESET Sources

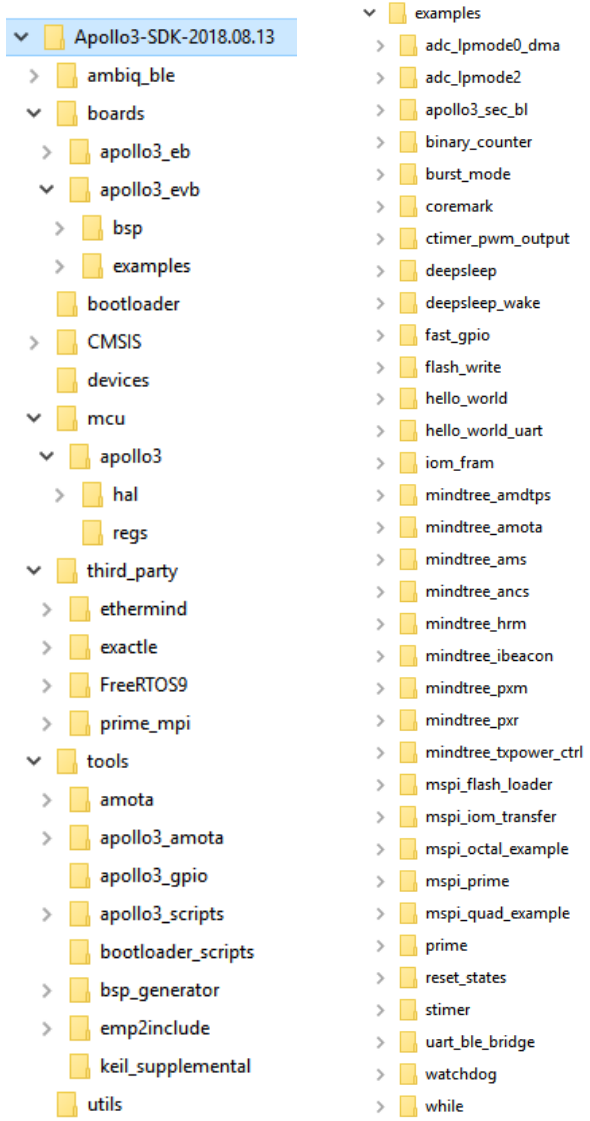
Reset: Power on Reset (POA)



- Some registers are only reset by System Power-Down (POA) which occurs ~1.3V (see datasheet for the exact voltage)
- During all other resets, including RSTn, BOD, WDT, and POR and POI Software resets, the following are retained:
  - All RTC registers retain state
  - RTC and STIMER counters continue operation from 32kHz XTAL or from LFRC (if below BODL). If clock sources stop oscillating at very low voltage, the RTC and STIMER will continue to maintain state.
  - Clock configuration registers retain state

AmbiqSuite SDK

- Register files (CMSIS compatible)
- HAL source code
- Mindtree Ethermind BLE Stack
- BSP source code for each EVB
- Extensive software examples
  - Source code
  - Keil, IAR, and GCC project files
- Application Notes
- API documentation



Ambiq Suite: HAL

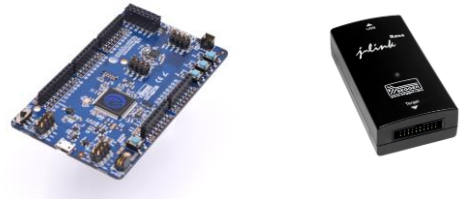
- HAL (hardware abstraction layer) makes using Apollo easier
- Abstraction provides simple functions and macros for enabling and using peripherals
- HAL also provides macros that make constants easier to read and use
  - AM_HAL_ADC_CLOCK_12MHZ instead of 0x01000000
- Several functions based on C macros that minimize number of executed instructions

Ambiq Suite: BSPs

- A BSP (board support package) contains additional functions and macros for use with specific board hardware
- Each EVK board has its own BSP
- BSPs make prototyping with Ambiq evaluation materials easier
- All Ambiq Suite code examples include use of BSP functions

Ambiq Debug Tools

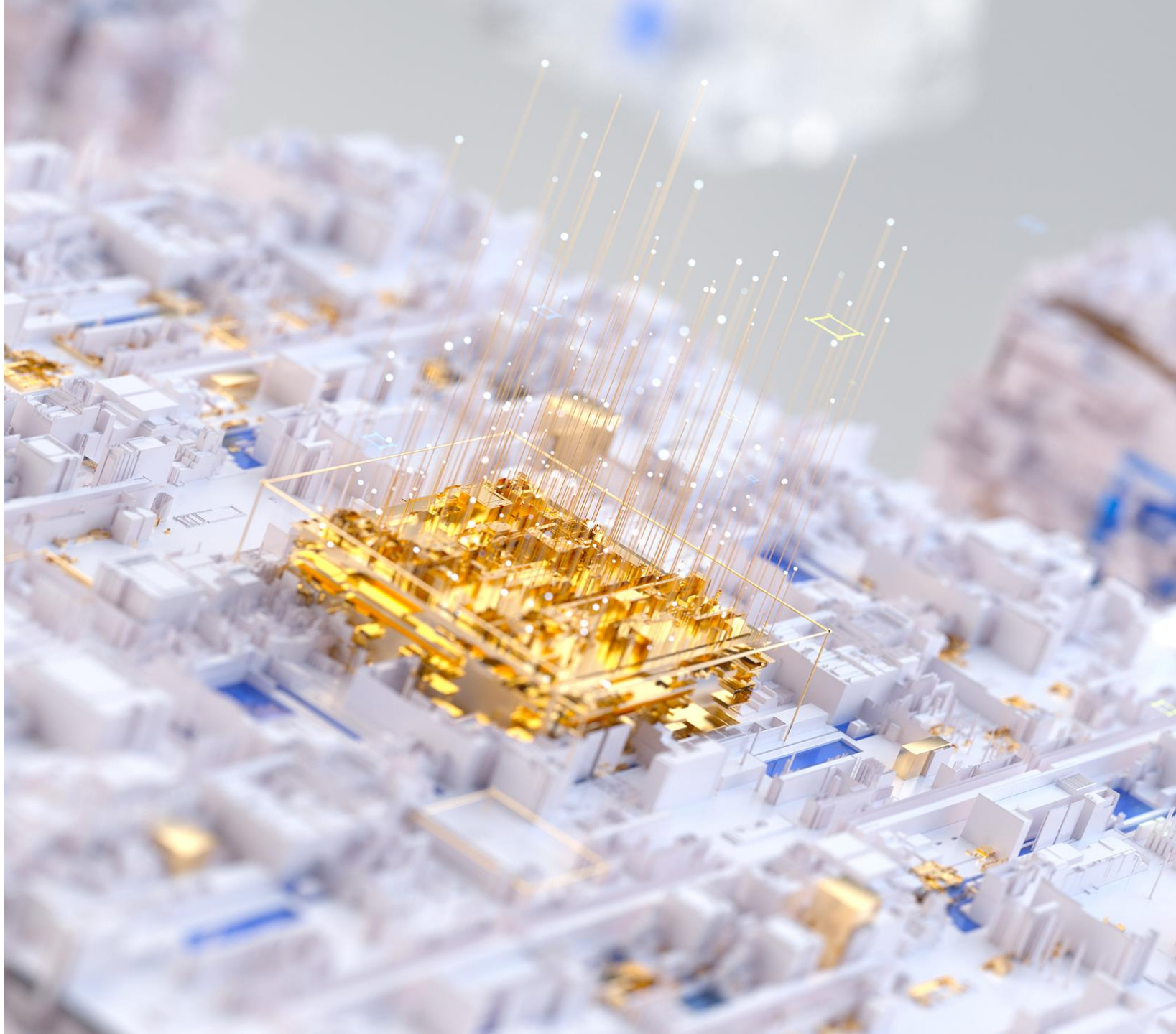
- Ambiq Micro MCUs are supported by industry standard tools
- Standard Cortex SWD debug interface.
  - Support for Apollo MCU family included in Segger J-Link software
  - Apollo family EVBs have onboard J-Link interface. Just connect USB.



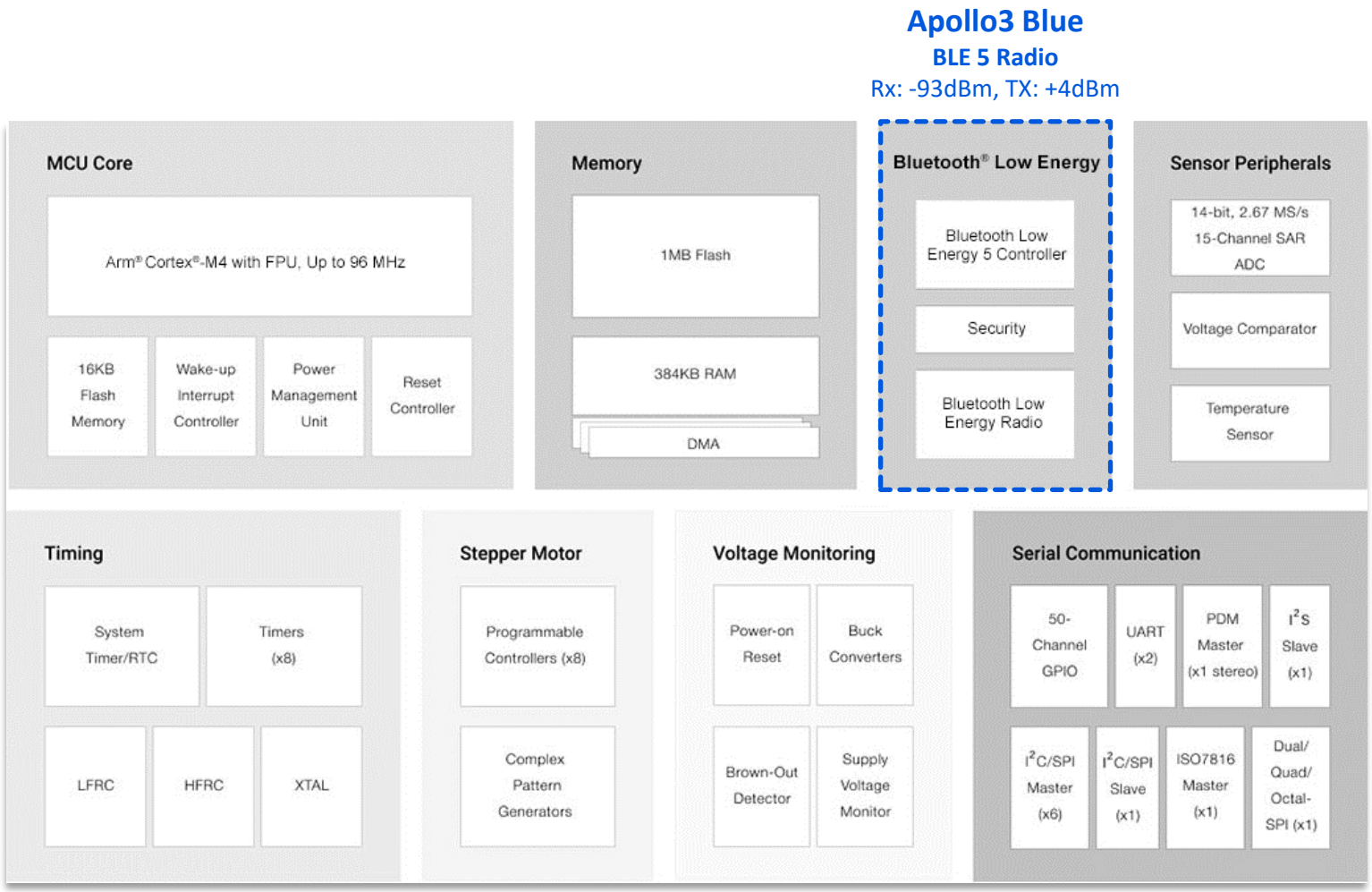
- All example code provided in Ambiq SDK come with Keil and IAR projects and GCC Makefile
- Keil and IAR downloads with Apollo family support built-in provided by their respective manufacturers

endpoint intelligence

Appendix



Apollo3 / Apollo3 Blue Features



Ultra-Low Supply Current

- 6 µA/MHz executing from flash or RAM at 3.3 V
- 1 µA deep sleep mode (Bluetooth Low Energy Off) with RTC at 3.3 V (Bluetooth Low Energy in SD)

High-Performance Arm Cortex-M4 Processor

- Up to 48 MHz nominal clock frequency with 96 MHz performance TurboSPOT Mode
- Floating Point Unit (FPU)
- Memory Protection Unit (MPU)
- Wake-up interrupt controller with 32 interrupts

Ultra-Low Power Memory

- Up to 1MB of flash memory for code/data
- Up to 384KB of low power RAM for code/data
- 16KB 2-way Associative/Direct-Mapped Cache

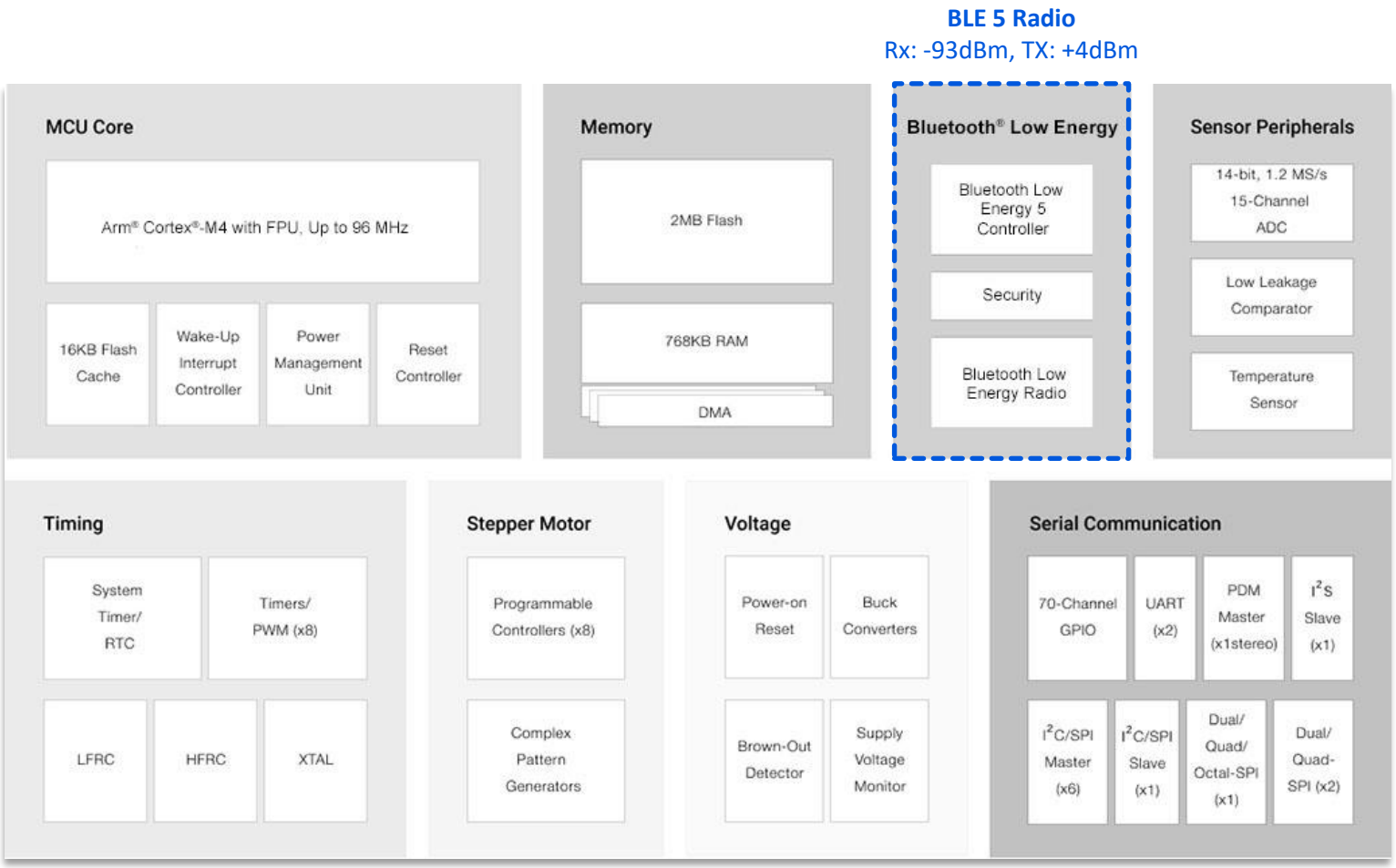
Ultra-Low Power Flexible Serial Peripherals

- ISO7816 Secure interface
- 1x 2/4/8-bit SPI master interface (MSPI)
- 6x I^2C/SPI masters for peripheral communication
- 1x I^2C/SPI slave for host communications
- 2x UART modules with 32-location Tx and Rx FIFOs
- PDM for mono and stereo audio microphones
- 1x I^2S slave for PDM audio pass-through

Package Options

- 5 mm x 5 mm, 81-pin BGA with 50 GPIO
- 3.25 mm x 3.37 mm, 66-pin WLCSP with 37 GPIO

Apollo3 Blue Plus Features



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- PDM for mono and stereo audio microphones
- 1x I^2S slave for PDM audio pass-through

Package Options

- 5.3 mm x 4.3 mm x 0.8 mm, 108-pin BGA with 74 GPIO

Apollo3 Blue Plus Voice-on-SPOT™ Kit

Hardware

Ultra-Low Power
- Apollo3 Blue Plus

High Performance Cortex-M4F Processor
- 48 MHz nominal clock frequency with 96 MHz TurboSPOT Mode

Integrated Bluetooth Low Energy
- RF Sensitivity: -93dBm
- TX Power: +4dBm max

Boards
- Digital MIC Click Boards – Vesper & Memsensing
- Apollo3 mikroBUS Audio Shield
- Apollo3 Blue Plus EVB

Software

Ambiq
- VoS SDK
- AmbiqSuite SDK

Communication
- Amazon Mobile Accessory (AMA)
- Google Android TV Voice Service - ATVV over BLE
- Audio stream over RTT, AMU2S (SPI to USB)

ambiq

endpoint intelligence

Thank You!