APPLICATION NOTE

Apollo4 Blue BLE Controller

XTAL32MHz CLK Request

A-SOCA4B-ANGA01EN v1.0

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Revision History

Revision	Date	Description
1.0	September 1, 2021	Initial release

Reference Documents

Document ID	Description

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SECTION

1

Introduction

The Apollo4 Blue BLE Controller supports crystal-based clock sources at 32MHz (for normal operation and synthesis of RF signals), and at 32kHz (for sleep mode and wakeup logic). When coupled with the Apollo4 SoC, these clocks are sourced from the SoC to the BLE Controller. In this configuration, the 32MHz clock is driven on XO32M and the 32kHz clock is driven on XO32k, both as single-ended signals. This document describes how the XTAL32MHz clock is sourced from the Apollo4 to the BLE controller.

SECTION

2

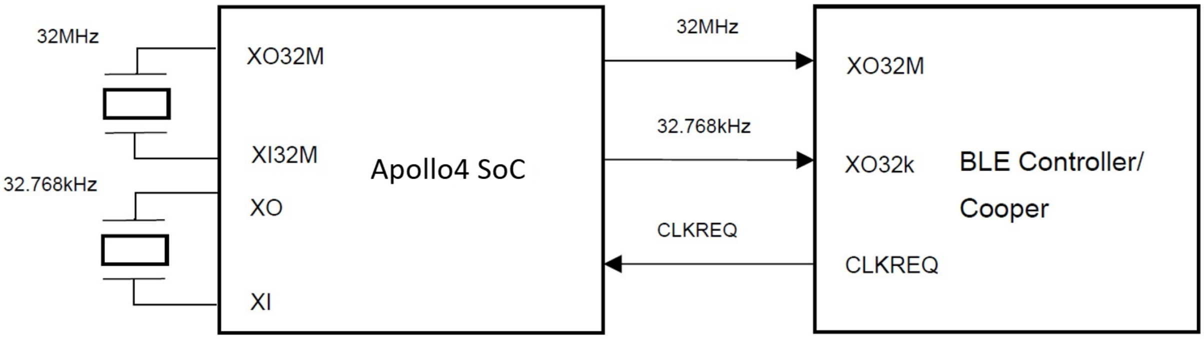
Clock Diagram

The Apollo4 Blue has inputs for 32MHz and 32kHz crystals. The 32MHz crystal is connected to the XO32M/XI32M pins, and the 32kHz crystal is connected to the XO/XI pins. The clocking configuration needs to be set in the MCUCTRL_XTALHSCTRL and MCUCTRL_XTALCTRL registers.

NOTE: The am_hal_mcuctrl_control() initializes the configuration of MCUCTRL_XTALHSCTRL and MCUCTRL_XTALCTRL registers to enable/disable the XTAL32MHz and XTAL32kHz.

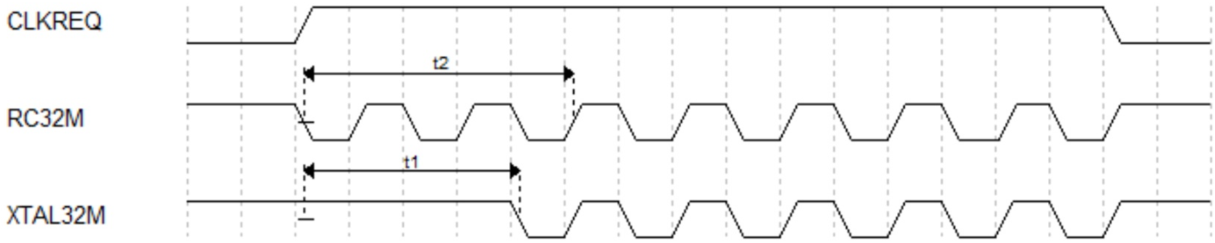
The 32MHz clock of the BLE Controller is sourced from XO32M as a single-ended signal, and the 32kHz clock is sourced from XO32k as a single-ended signal. The CLKREQ (GPIO) signal is used to assert a clock request to the SoC. This allows the SoC to power down the 32MHz crystal to save power. The 32kHz source is always on after the BLE controller in the Apollo4 Blue is initialized and turned on.

Figure 2-1: SoC Clock Source Configuration



The handshake of XTAL32MHz is described as below:

Figure 2-2: Clock Timing Diagram



On a “wake” event:

- BLE controller utilizes internal RC32MHz and asserts CLKREQ
- The Apollo4 SoC initiates XTAL32MHz startup after receiving the CLKREQ interrupt
- XTAL32MHz is stable after 't1' delay time and available to be provided to XO32M of BLE controller
- BLE controller switches to use XTAL32MHz after asserting CLKREQ for 't2' delay.

NOTE: The 't1' delay must be shorter than the 't2' delay, meaning that the XTAL32MHz must become stable before the BLE controller switches from the RC32MHz source to XTAL32MHz.

On a “sleep” event:

- BLE controller switches to the low frequency clock and de-asserts CLKREQ
- Apollo4 SoC gates XTAL32MHz and optionally powers down XTAL32MHz

NOTE: The XTAL32MHz is powered down by default when CLKREQ is de-asserted. The XTAL32MHz should be kept on if other modules of Apollo4 SoC are using it, and is to be powered down when not in use.

SECTION

3

Clock Configuration

3.1 Configure CLKREQ GPIO

Initialize the GPIO configuration of CLKREQ pin and enable it in **am_devices_cooper_pins_enable()**.

```
am_hal_gpio_pincfg_t g_AM_DEVICES_COOPER_CLKREQ =
{
    .GP.cfg_b.uFuncSel             = AM_HAL_PIN_40_GPIO,
    .GP.cfg_b.eGPInput             = AM_HAL_GPIO_PIN_INPUT_ENABLE,
    .GP.cfg_b.eGPRdZero         = AM_HAL_GPIO_PIN_RDZERO_READPIN,
    .GP.cfg_b.eIntDir                  = AM_HAL_GPIO_PIN_INTDIR_LO2HI,
    .GP.cfg_b.eGPOutCfg          = AM_HAL_GPIO_PIN_OUTCFG_DISABLE,
    .GP.cfg_b.eDriveStrength     = AM_HAL_GPIO_PIN_DRIVESTRENGTH_12MA,
    .GP.cfg_b.uSlewRate            = 0,
    .GP.cfg_b.ePullup                 = AM_HAL_GPIO_PIN_PULLUP_NONE,
    .GP.cfg_b.uNCE                   = 0,
    .GP.cfg_b.eCEpol                 = AM_HAL_GPIO_PIN_CEPOL_ACTIVELOW,
    .GP.cfg_b.uRsvd_0               = 0,
    .GP.cfg_b.ePowerSw            = AM_HAL_GPIO_PIN_POWERSW_NONE,
    .GP.cfg_b.eForceInputEn      = AM_HAL_GPIO_PIN_FORCEEN_NONE,
    .GP.cfg_b.eForceOutputEn   = AM_HAL_GPIO_PIN_FORCEEN_NONE,
    .GP.cfg_b.uRsvd_1               = 0,
};

void am_devices_cooper_pins_enable(void)
{
am_hal_gpio_pinconfig(AM_DEVICES_COOPER_CLKREQ_PIN, g_AM_DEVIC-
ES_COOPER_CLKREQ);
…
}
```

3.2 Initialize CLKREQ Interrupt Service

Initialize the CLKREQ interrupt and corresponding service handler in **HciDrvRadioBoot()**.

```
uint32_t HciDrvRadioBoot(bool bColdBoot)
{
    …
    uint32_t IntNum = AM_DEVICES_COOPER_CLKREQ_PIN;
    am_hal_gpio_interrupt_register(AM_HAL_GPIO_INT_CHANNEL_0, IntNum,
      ClkReqIntService, NULL);
    am_hal_gpio_interrupt_control(AM_HAL_GPIO_INT_CHANNEL_0,
                                  AM_HAL_GPIO_INT_CTRL_INDV_ENABLE,
                                  (void *)&IntNum);
    …
}

static void ClkReqIntService(void *pArg)
{
   if(am_devices_cooper_clkreq_read(g_IomDevHdl))
   {
     // Power up the 32MHz Crystal
     am_hal_mcuctrl_control(AM_HAL_MCUCTRL_CONTROL_EXTCLK32M_KICK_START,
    0);
}
else
{
     am_hal_mcuctrl_control(AM_HAL_MCUCTRL_CONTROL_EXTCLK32M_DISABLE,
    0);
}
     am_hal_gpio_intdir_toggle(AM_DEVICES_COOPER_CLKREQ_PIN);
}
```

3.3 Initialize XTAL32MHz Startup

The **am_hal_mcuctrl_control()** is used to enable and disable the 32MHz crystal. The trim codes for CAP1/CAP2 are to be modified by setting the MCUCTRL_XTALHSTRIMS_XTALHSCAPTRIM and MCUCTRL_XTALHSTRIMS_XTALHSCAP2TRIM fields of MCUCTRL_XTALHSTRIMS register based on the specific XTAL32M model on your board in the case of AM_HAL_MCUCTRL_CONTROL_EXTCLK32M_KICK_START, AM_HAL_MCUCTRL_CONTROL_EXTCLK32M_DISABLE and AM_HAL_MCUCTRL_CONTROL_EXTCLK32M_NORMAL.

```
uint32_t am_hal_mcuctrl_control(am_hal_mcuctrl_control_e eControl, void
*pArgs)
{
         volatile uint32_t ui32Reg;
         switch ( eControl )
         {
      …
          case AM_HAL_MCUCTRL_CONTROL_EXTCLK32M_KICK_START:
                 // Set the specific trim code for CAP1/CAP2, it impacts
                    frequency accuracy and should be retrimmed
          ui32Reg = _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSCAP2TRIM, 44) |
              _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSCAPTRIM, 4)      |
               // Set the transconductance of crystal to maximum, it
accelerate the startup sequence
              _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSDRIVETRIM, 3)      |
              // Choose the power of clock driver to be the cleanest one
              _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSDRIVERSTRENGTH, 0) |
              // Tune the bias generator
                 _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSIBIASCOMP2TRIM, 3) |
                 _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSIBIASCOMPTRIM, 15) |
             // Set the bias of crystal to maximum
                 _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSIBIASTRIM, 127)    |
                  _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSRSTRIM, 0)        |
                      _VAL2FLD(MCUCTRL_XTALHSTRIMS_XTALHSSPARE, 0);
              MCUCTRL->XTALHSTRIMS = ui32Reg;
            …
            break;
            …
            }
}
```

The **am_devices_cooper_crystal_trim_set()** can be also used to set the CAP1/CAP2 to test the 32MHz crystal frequency on your board to find a suitable values for good accuracy.

3.4 Wakeup Time Configuration

The "t1" delay mentioned in *Section 2 Clock Diagram on page 6*, which should be greater than 750µs, is intended to allow the XTAL32MHz time to start up and become available to provide clock to the BLE Controller.

The "t2" delay, mentioned in *Section 2 Clock Diagram on page 6,* is intended to keep the BLE Controller waiting for that time after asserting CLEREQ, before switching to use the XTAL32MHz clock. If "t1" is longer than "t2", the BLE Controller will enter an unknown state, which is to be avoided. The "t2" can be set by modifying the EXT_WAKEUP_TIME_VALUE and OSC_WAKEUP_TIME_VALUE in am_devices_cooper.h.

NOTE: The EXT_WAKEUP_TIME_VALUE determines the time before switching to XTAL32MHz from RC32MHz when the BLE Controller is woken up by an external signal, whereas OSC_WAKEUP_TIME_VALUE determines the time before switching to XTAL32MHz from RC32MHz when the BLE Controller is woken up by its internal timer.

The BLE Controller may not be able to determine the wakeup source at the next wakeup instance so it will choose the maximum of these two parameters to determine the time 't2'. These two parameters are always set to be the same and written to BLE Controller NVDS field. The default value is 1000µs.

```
#ifndef EXT_WAKEUP_TIME_VALUE
#define EXT_WAKEUP_TIME_VALUE           1000 // microsecond
#endif
#ifndef OSC_WAKEUP_TIME_VALUE
#define OSC_WAKEUP_TIME_VALUE           1000 // microsecond
#endif
```

The Apollo4 Blue SoC needs to execute the ClkReqIntService() within "t2-t1" after receiving the CLKREQ interrupt. In some systems, there may be other GPIO interrupts in the same GPIO group with CLKREQ, which may block the executing of ClkReqIntService(). In such case, a higher "t2" delay would have to be set to ensure that the BLE Controller's wait time is sufficient.

NOTE: The longer wakeup time will result in an earlier wake up for the BLE Controller, which may result in higher power consumption.

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