QUICK START GUIDE

Apollo4 Blue Plus (KBR) EVB

(EVB Revision 1.0)

Ultra-low Power Apollo SoC Family

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1. Introduction

This document provides guidance for setting up the Apollo4 Blue Plus (KBR) Evaluation Board (EVB), revision 1, part number AMA4BPEVB, to get started executing code examples, measuring power consumption in various configurations, and beginning software development.

This version of the EVB contains silicon version C0 of the Apollo4 Blue Plus (KBR) which supports Bluetooth 5.1 Low Energy[1].

FCC Regulatory Notice

This kit has not been authorized under the rules of the FCC. It is designed to:

1. Allow product developers to evaluate electronic components, circuitry or software associated with the kit to determine whether to incorporate such items in a finished product.
2. Enable software developers to write software applications for use with the end product.

This kit is not a finished product and may not be resold or otherwise marketed unless all required FCC authorizations are first obtained. **Developers using this reference design in their product are responsible for obtaining all required FCC equipment authorizations.**

Operation of this kit is subject to the condition that it does not cause harmful interference to licensed radio stations and that it accepts any harmful interference received. Unless the assembled kit is designed to operate under part 15, part 18, or part 95 of 47 CFR Chapter I - FCC, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of the latter chapter.

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2. Document Revision History

Rev #	Date	Description
1.0	Sep 2022	Document initial public release
1.1	Nov 2022	Noted CE Mark is pending
1.2	Mar 2023	Updated section “Software Development Tools” on page 15
1.3	Jul 2024	FCC regulatory statement added/amended.

Table 1: Document Revision History

3. Reference Documents and Software

The following items, which can be downloaded from the Apollo4 Blue Plus Product Page link on https://ambiq.com/, may be useful in understanding and using the EVB.

- EVB Schematic
- Apollo4 Blue Plus Datasheet
- Apollo4 Family Programmer's Guide
- Apollo4 Plus/Blue Plus Errata List
- AmbiqSuite SDK

4. Quick Start

The EVB Kit comes with the following items:

- Apollo4 Blue Plus (KBR) Evaluation Board (EVB), revision 1
- USB Type C cable
- Four adhesive-backed rubber feet
- Extra jumpers

Caution: The EVB has components loaded on the back of the board. Care should be taken to not damage these components. The included rubber feet should be applied to the bottom of the board to prevent direct contact between the components and a desk surface.

The EVB comes with jumpers pre-configured for default operation. Also, it has been pre-programmed with the FreeRTOS Fit example program. To start EVB program execution, connect the USB-C cable from a USB port on a PC to the J-Link USB connector (J6) on the EVB, and turn on the power switch (SW4). The blue LED under the power switch should illuminate.

To observe program execution, do the following steps:

- Start a Bluetooth explorer application such as LightBlue Explorer on a mobile phone or other device that can serve as a Bluetooth host device.
- If diagnostic message are desired, start a SWO session by bringing up a Segger J-Link SWO Viewer (see Software Development Tools section for link to Segger tools download site). For "device" select "AMA4B2KP-KBR" and set SWO clock to 1000 KHz.
- Reset the board by pressing switch SW3.
- After reset, the Apollo4 Blue Plus (KBR) will start advertising and Bluetooth traffic will appear in the SWO viewer. One of the messages in the SWO viewer will indicate that this device called "Fit" (EVB) is advertising.
- The device "Fit" will appear in the list of devices in the host application (App). By selecting it, the host will connect to the "Fit" device on the EVB.
- The App and Fit will exchange several commands and responses (events) until the SWO message reports that "Fit got evt 41").

The AmbiqSuite SDK provides many example programs that may be run on the EVB. To run these examples, download the SDK via the link provided above and select any of the pre-built examples in the SDK at /boards/apollo4p_blue_kbr_evb/examples.

5. Overview of the Apollo4 Blue Plus (KBR) EVB

The Apollo4 Blue Plus (KBR) EVB, version 1, features signal-accessible headers and an integrated J-Link debugger. The following figures show the board layout, its major features and the location of all components.

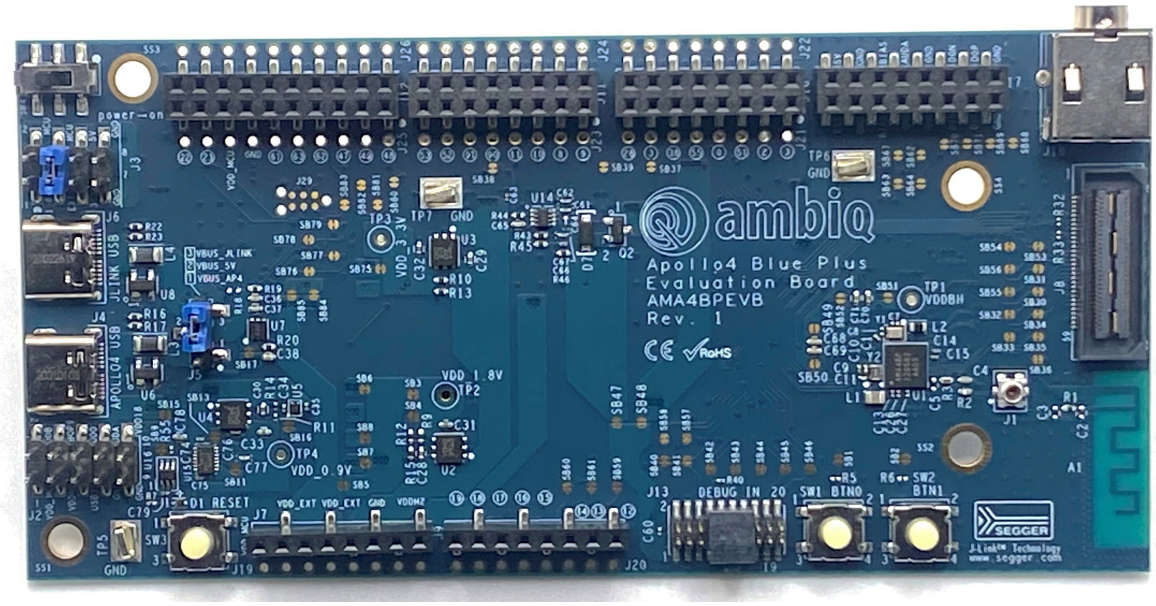

Figure 1. Apollo4 Blue Plus (KBR) EVB

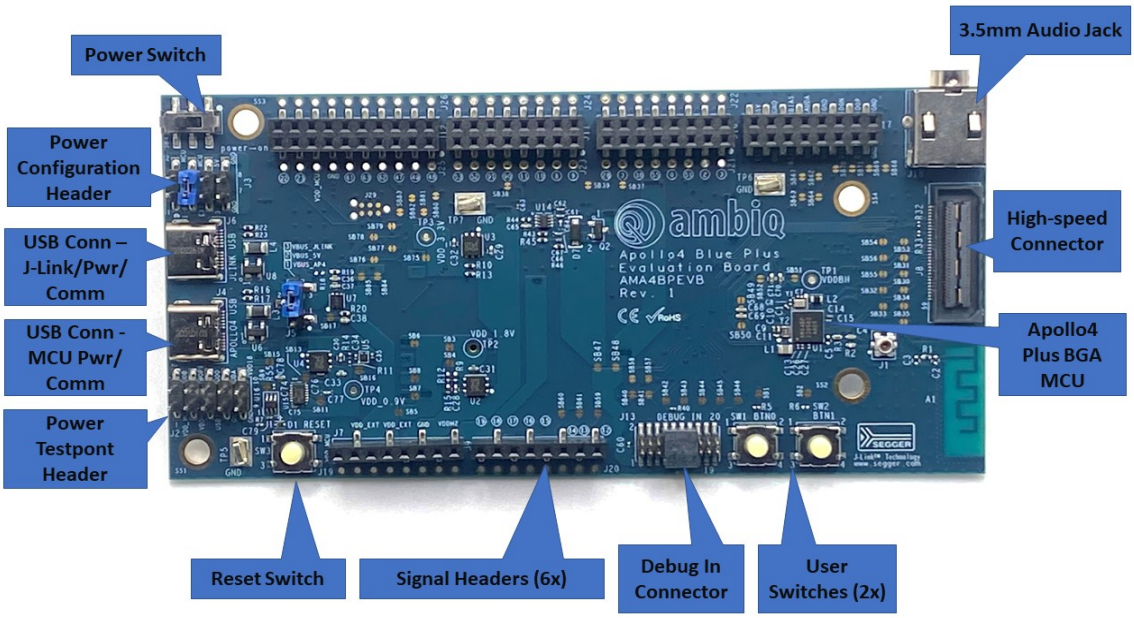

Figure 2. Apollo4 Blue Plus (KBR) Plus EVB - Major Top Side Components

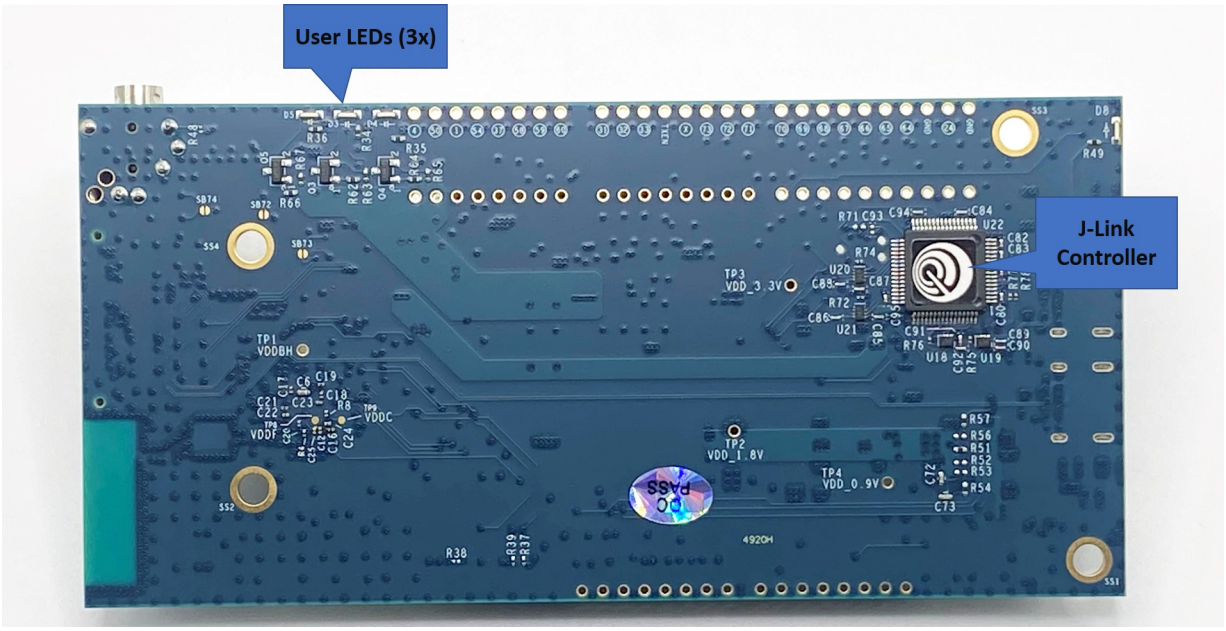

Figure 3. Apollo4 Blue Plus (KBR) Plus EVB - Major Bottom Side Components

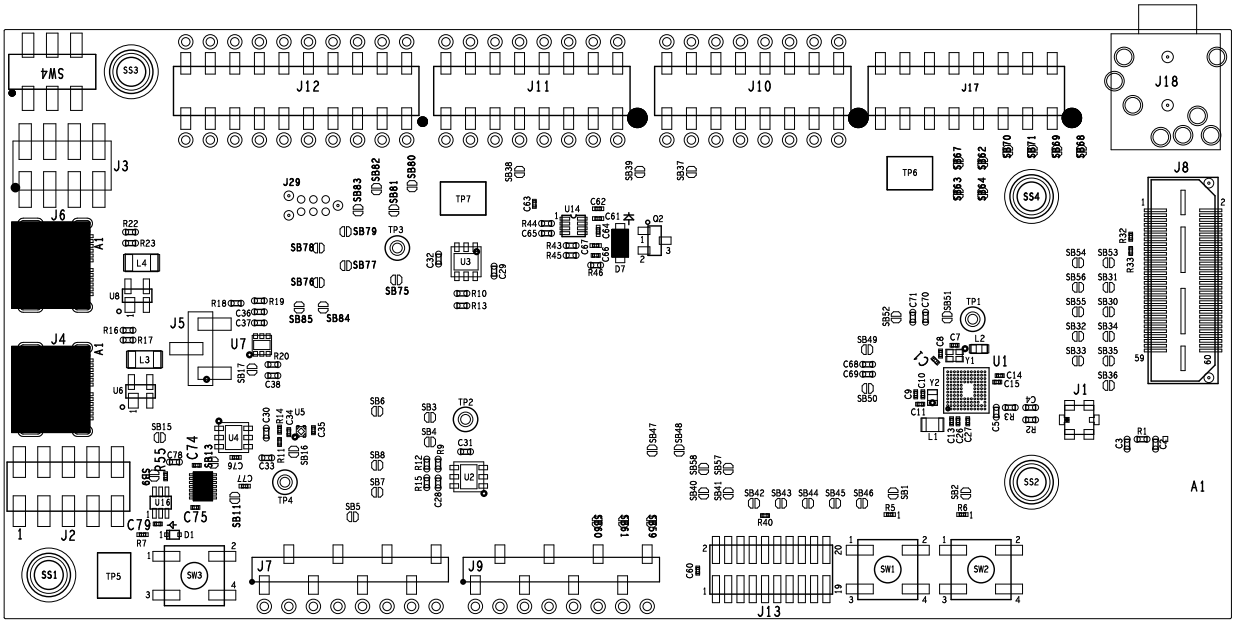

Figure 4. Apollo4 Blue Plus (KBR) Plus EVB - Top Side Parts Location

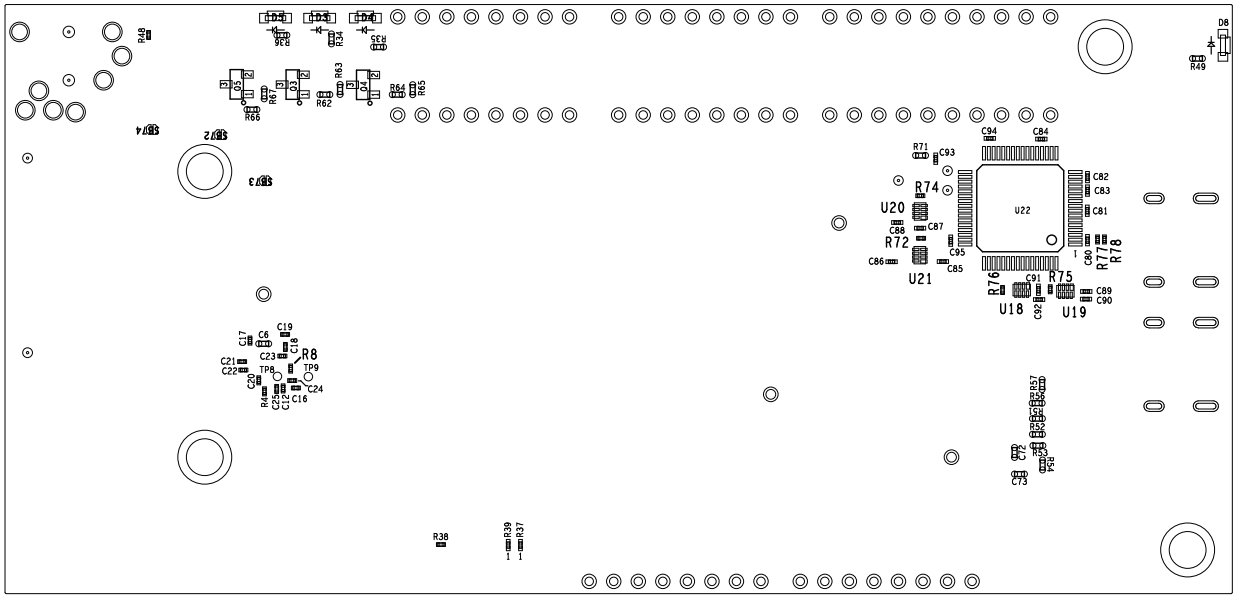

Figure 5. Apollo4 Blue Plus (KBR) Plus EVB - Bottom Side Parts Location

The EVB has these features:

- Apollo4 Blue Plus (KBR) SoC in the BGA package (AMA4B2KP-KBR)
- Low power reference design
- Multiple power/clock options
- USB Type C connector for power/download/debug
- USB Type C connector for power/data to Apollo4 Blue Plus (KBR)
- On-board PCB (MIFA) antenna
- Segger J-Link debugger
- Debugger-in port (J13) (SWD or ETM)
- Three user-controlled LEDs
- Two push buttons for application use, plus a reset push button
- Power slide switch with LED power indicator
- Five headers (J7, J9-J12) for pin/power access to a shield board
- Test points for power measurements
- High-speed connector (J8 - QSH-030-01-L-D-A) for interfacing to displays and/or high-speed memory
- RF switch/connector (Murata MM8430-2610RA1) for BLE PHY testing
- Multiple solder-bridge options for power supply flexibility and peripheral access options
- 3.5 mm audio jack (SJ-435107) for evaluating low-power analog audio interface
- RoHS compliant

CAUTION: The EVB has components loaded on the back of the board. Care should be taken to not damage these components.

5.1 Secure Boot on the Apollo4 Blue Plus (KBR) SoC

Apollo4 Blue Plus (KBR) SoC parts from the Ambiq factory are preprogrammed with a Secure Bootloader and an uninitialized Customer Info Space, referred to as INFO0. Initial provisioning of the part would include programming a valid INFO0 and programming the main firmware image in the flash. The Apollo4 Blue Plus (KBR) EVB is shipped with the INFO0 configuration pre-programmed with optimal settings for the EVB layout:

1. Default boot to non-secure mode
2. Enable Boot Override to Push Button on GPIO18 (OTP setting) - BTN0/SW1.
3. Enable wired updates over UART0
   A. UART0 is mapped to J-Link (OTP Setting).
   B. Baud rate is 115200 bps, no-parity, 8-bit data length, no flow control.
   C. Timeout is 3 seconds.

For reference, the following settings are programmed into INFO0 on the Apollo4 Blue Plus (KBR) SoC resident on the EVB:

- SIMO Buck is NOT enabled.
- Secure Bootloader (SBL) interface is configured to UART using GPIO47 and GPIO60, which allows secure boot to be performed over the J-Link COM interface of the EVB.
- SBL override pin is configured to GPIO18 which is BTN0/SW1 on the EVB.
- All Flash and Debugger protection features are disabled.

For information on changing the INFO0 settings as well as using the Secure Bootloader, please refer to the *README.txt* file, which can be found in the tools\apollo4b_scripts folder of the latest SDK release supporting the Apollo4 family. This folder contains a number of python scripts to demonstrate generation of INFO0 settings, customer main images, and the creation of images for the Wired Update protocol over UART.

6. Debug Interface

Figure 6 shows the Apollo4 Blue Plus (KBR) EVB set up for standard debug using the on-board J-Link debugger and on-board power supply.

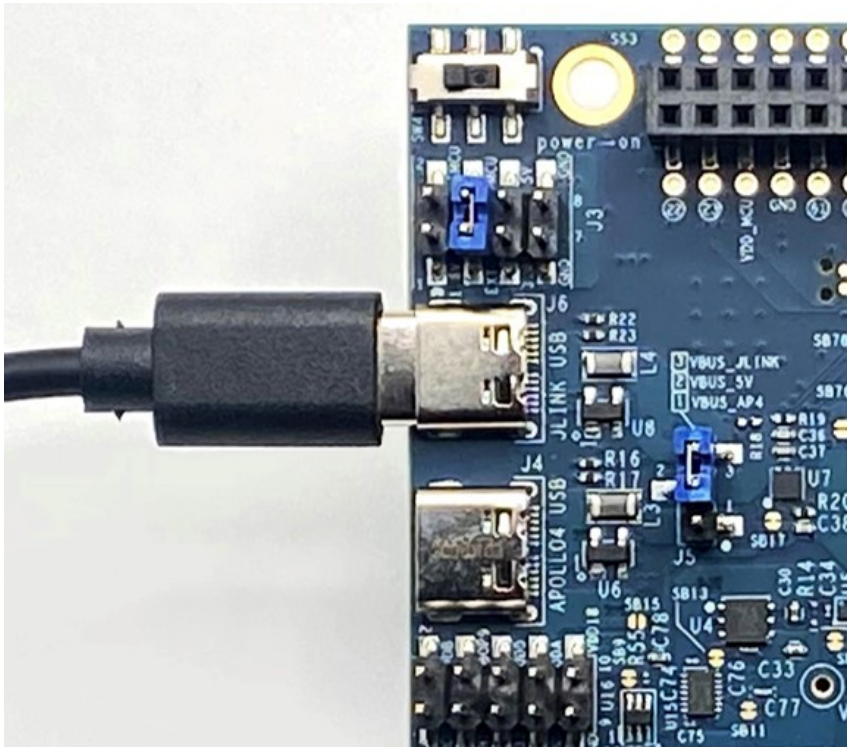

Figure 6. Apollo4 Blue Plus (KBR) EVB Using On-board J-Link Debugger

The debug interface is supported by standard J-Link drivers from Segger. Please refer to “Software Development Tools” on page 15 for more details on J-Link debug support.

6.1 Use of External Debugger

This EVB also supports the use of an external Cortex SWD debug interface through a 20-pin debug header (DEBUG IN - J13) as shown in Figure 7. See the EVB schematic for connector pinout.

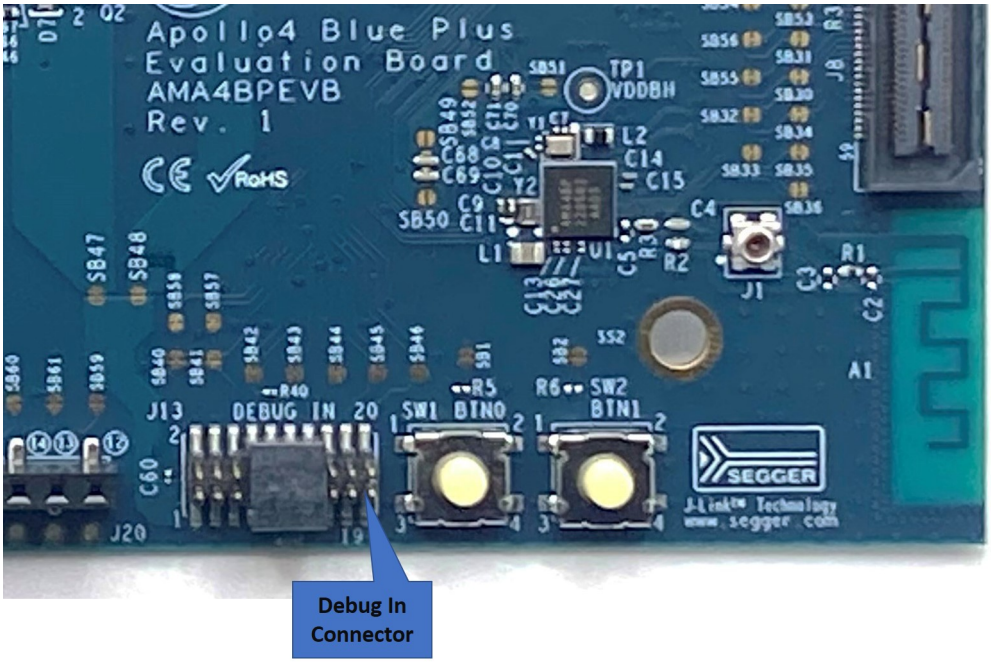

Figure 7. Apollo4 Blue Plus (KBR) EVB's DEBUG IN Header (J13)

No jumper changes are required to use an external debug adapter. Simply connect the external debug adapter with a ribbon cable connector to the "DEBUG IN" header.

NOTE: Remove protective guard before attempting to connect to the DEBUG IN header.

7. Software Development Tools

The standard Segger J-Link debug interface is used on the Apollo4 Blue Plus (KBR) EVB. Please install the latest Segger J-Link software, and configure your preferred development IDE (Keil, IAR, or Eclipse) to use the J-Link debug interface. Please consult the release notes of the latest/applicable SDK release for the version of the tools used during testing of the SDK and which are recommended for development with the SDK.

Links to the supported development tools are listed below.

- SEGGER J-Link Software: https://www.segger.com/downloads/jlink
- KEIL uVision 5 (ARM Compiler 5): https://www.keil.com/demo/eval/arm.htm
- Latest Keil Pack (CMSIS Ambiq Pack): http://www.keil.com/dd2/pack/#/third-party-download-dialog
- IAR IDE/Compiler: https://www.iar.com/iar-embedded-workbench/tools-for-arm/arm-cortex-m-edition/
- GCC (GNU Arm Embedded Toolchain): https://gcc.gnu.org

Regardless of IDE used, please install the Segger J-Link software. All of the above development environments support J-Link, but you must have the latest J-Link software installed. Most alternate development environments also support J-Link.

Please refer to the AmbiqSuite SDK Getting Started Guide for more details on setting up development IDEs to use J-Link.

8. Power Supply Options and Measuring Current

The Apollo4 Blue Plus (KBR) EVB is intended to operate off of a 5 V supply, which is used to generate downstream voltages.

There are two power supply options for the EVB SoC:

- Operate at 1.9 V by default as provided by the on-board power supply (referred to as nominal "VDD_1.8V"). This can be adjusted to 1.8 V by shorting SB4 shown on the Power Supplies page of the EVB schematic(1).
- Provide externally supplied power.

The EVB utilizes solder-bridges for connecting and disconnecting rails from power supplies, whether generated on-board or off-board. Figure 8 shows the solder-bridge connection strategy between various on-board power supplies and the SoC's power rails.

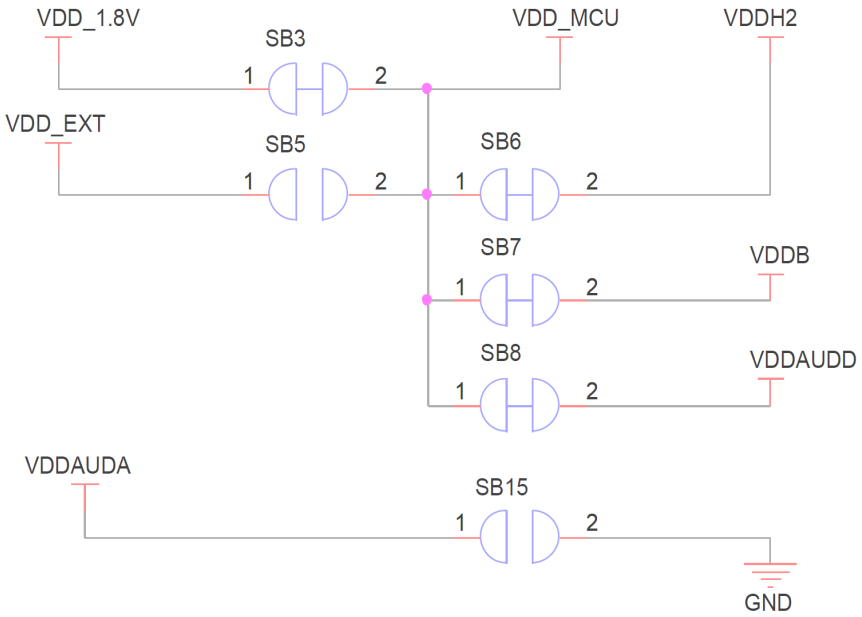

Figure 8. Apollo4 Blue Plus (KBR) EVB Power Supplies Solder Bridge Connection

Figure 9 shows the USB load switch circuit producing the voltage supplied to VDDUSB33 and VDDUSB0_9 through solder-bridges SB13 and SB11, respectively. These solder bridges are shorted by default.

1. Refer to the EVB schematic and assembly drawing for purpose and location of all solder bridges on the EVB.

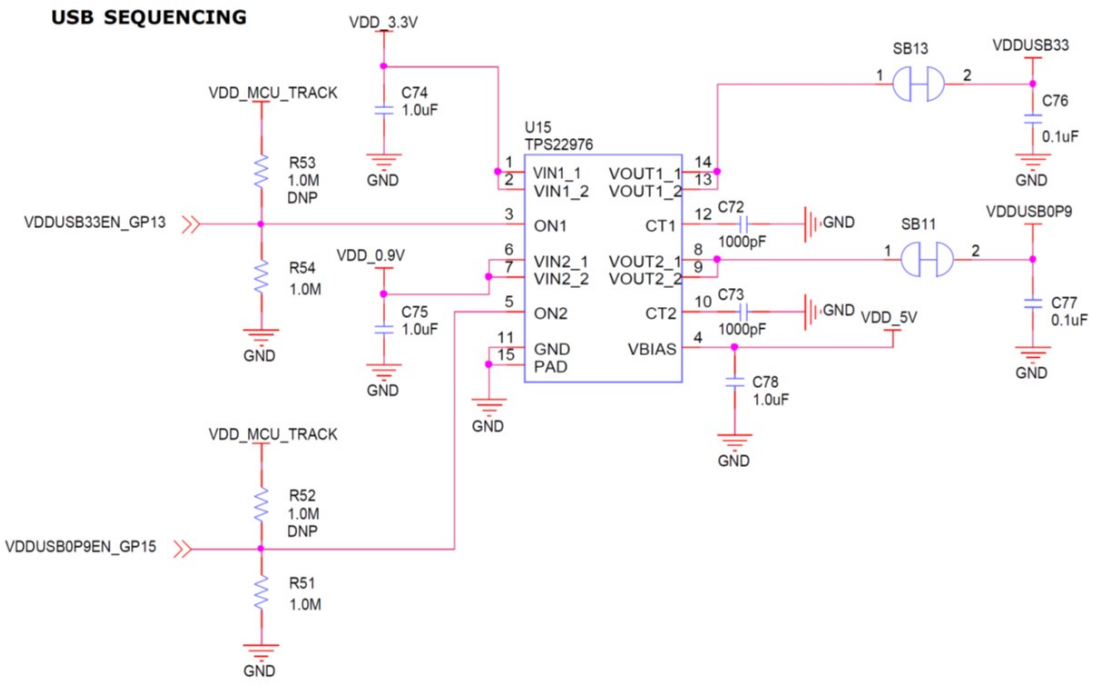

Figure 9. Apollo4 Blue Plus (KBR) EVB USB Load Switch Circuit

Similarly, Figure 10 shows the load switch circuit producing the voltage supplied to the MIPI DPHY VDD18 supply through solder-bridge SB9. This solder bridge is also shorted by default.

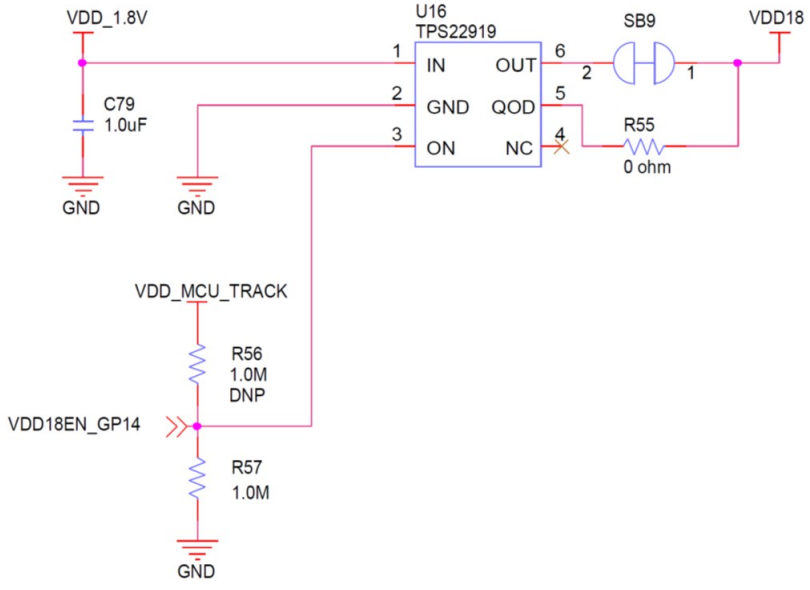

Figure 10. Apollo4 Blue Plus (KBR) EVB VDD18 Load Switch Circuit

As shown in the following figures, headers J2 and J3 provide easy access to the various system and chip-level power supplies present on the EVB. These can be used in conjunction with the above solder-bridges to measure current, monitor voltage, or provide externally generated power to each specific rail.

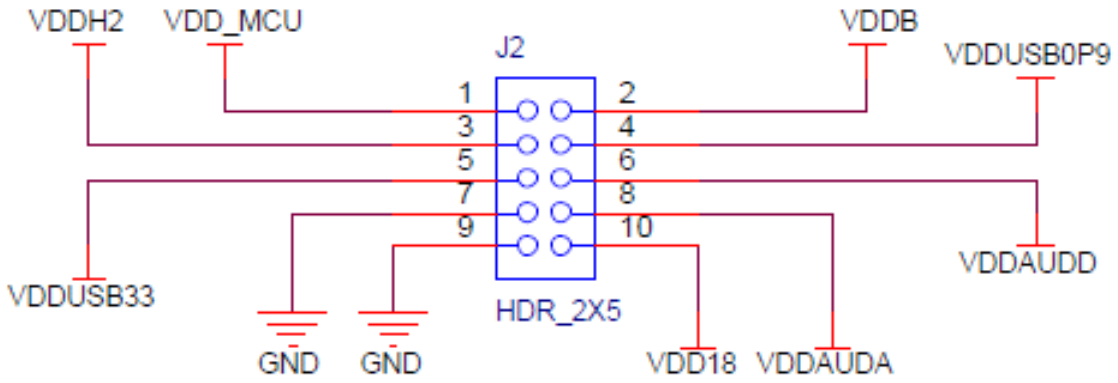

Figure 11. Apollo4 Blue Plus (KBR) EVB Voltage Test Points on Header J2

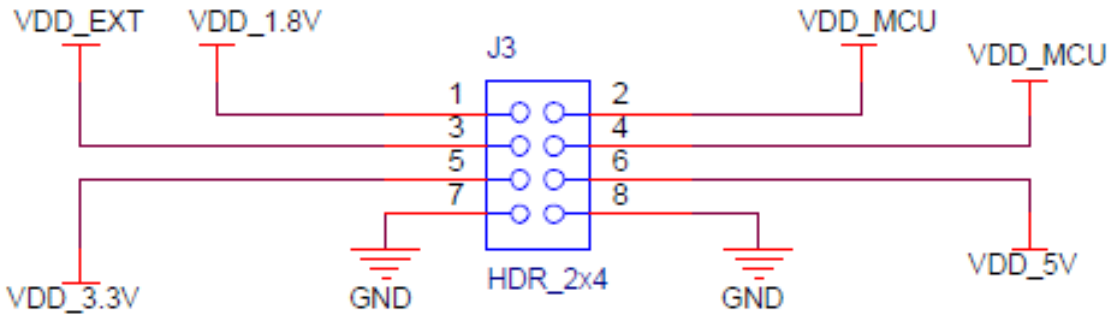

Figure 12. Apollo4 Blue Plus (KBR) EVB Voltage Selection on Header J3

8.1 Measuring Current

If the user wants to use a separate power supply for the EVB, then SB3 shown above should be open, and either SB5 should be shorted or pins 3 and 4 of J3 should be jumped. The external power rail can be applied to VDD_EXT on J3, pin 3. Consult the electrical specifications in the Apollo4 Blue Plus (KBR) Datasheet for the acceptable operating range for VDD_MCU.

Note: The J-Link I/O voltage should be set to the new VDD_IO of the chip, and therefore SB84 (not shown in the figure) should be opened and SB85 should be shorted (soldered).

Current consumption of the Apollo4 Blue Plus can be measured by connecting an ammeter between pins 1 and 2 of J3 after SB3 has been cut. For increased accuracy of this current measurement, especially when measuring Deep Sleep current, SB76 also needs to be cut on revision 1 of the EVB - see Figure 4 for location. This disconnects the RSTn line from the J-LINK controller to the MCU. J-LINK can still communicate with and program the Apollo4 Plus, but cannot reset the device after reprogramming. To

prevent having to manually reset the device after reprogramming, SB76 can be re-shorted to allow J-LINK to reset the device.

Use of the EVB using the on-board SoC supply may be restored by disconnecting the external supply (if connected) and either shorting SB3 or jumping between pins 1 and 2 of J3. The J-Link I/O voltage also should be restored.

9. Non-Power Solder Bridges

9.1 Solder Bridges for Reducing Trace Length to Optimize Performance

The following peripherals support solder-bridge connections, which allow for optimized performance by reducing overall trace length at the cost of losing connectivity to their respective GPIO headers. Note that these connections can be reset by applying solder across the solder-bridge.

Peripheral	GPIO	Description
Display Controller, MSPI0	37, 64-73	Opening the following corresponding solder-bridges shown in Figure 4 connects these GPIO exclusively to J8, with minimal trace stubs: SB36, SB56, SB55, SB30 - SB35, SB53, SB54.
ETM	50-54, 55 (open by default)	Opening the following corresponding solder-bridges shown in Figure 4 connect these GPIO exclusively to J13: SB42 - SB46, SB57. SWO is default connection to J13. (shared with GP55, SWTRCTL)

Table 2: Peripherals Supporting Solder Bridge Connections

Additionally, the LED indicators can be disconnected from GPIO30, GPIO90 and GPIO91 by opening their respective solder-bridges (SB37, SB38, and SB39). GPIO47, GPIO58, GPIO59 and GPIO60 are used for UART communication with the on-board J-Link. Opening SB80-SB83 frees these pins for exclusive use with the standard GPIO headers J10 and J12.

9.2 Solder Bridges for Audio Selectivity

As shown in Figure 13, a single audio jack, J18, provides stereo audio input routed to AUDADC (also referred to as LPADC) inputs on the SoC. Alternatively, up to 4 single-ended or 2 differential pair audio signals as shown in Figure can be input on connector J17 which is routed on the EVB as differential pair(s) to AUDADC inputs. The default (shorted) solder bridge configuration enables either of these input options.

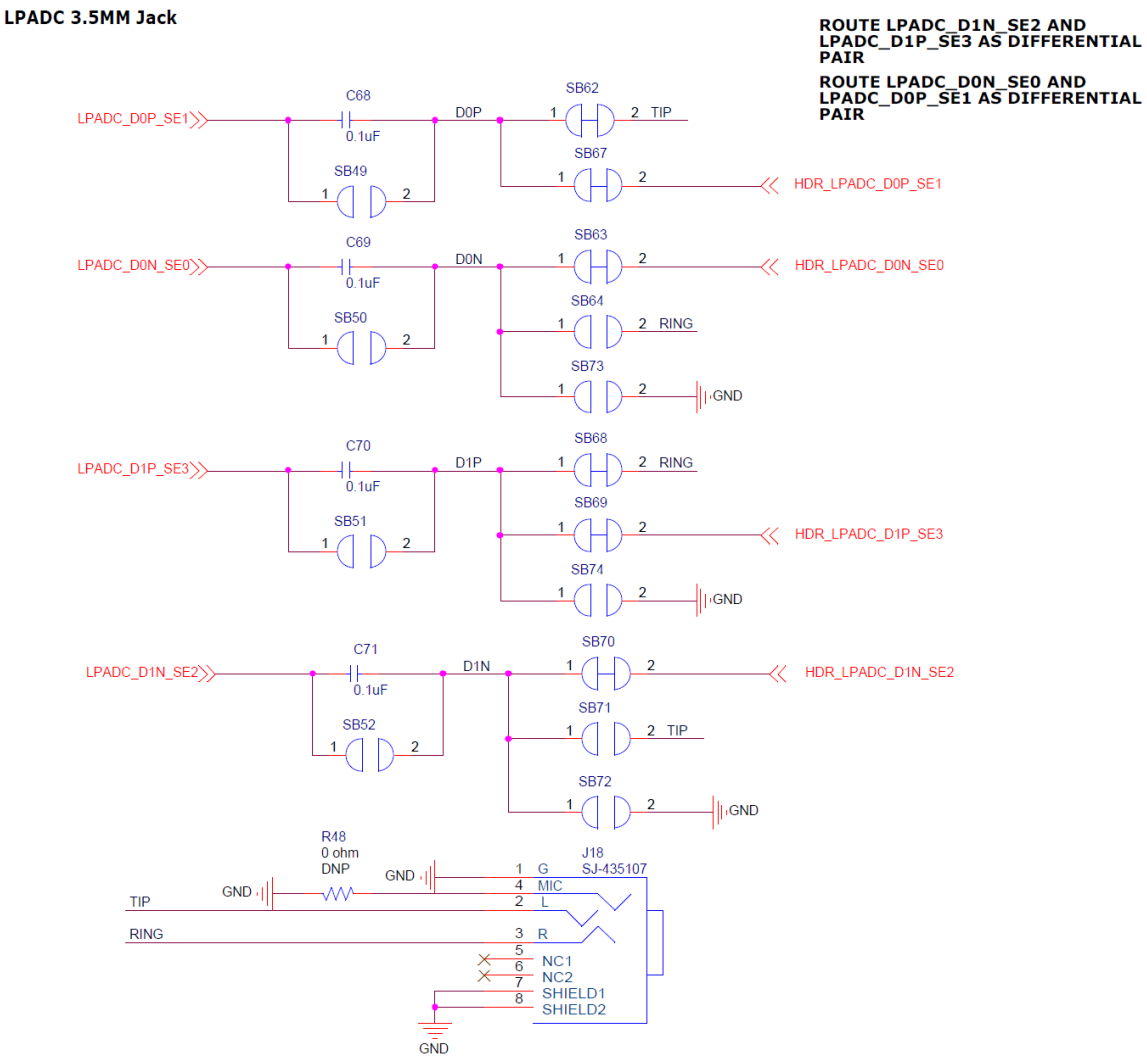

Figure 13. Audio Jack J18 and AUDADC Audio Source Selections

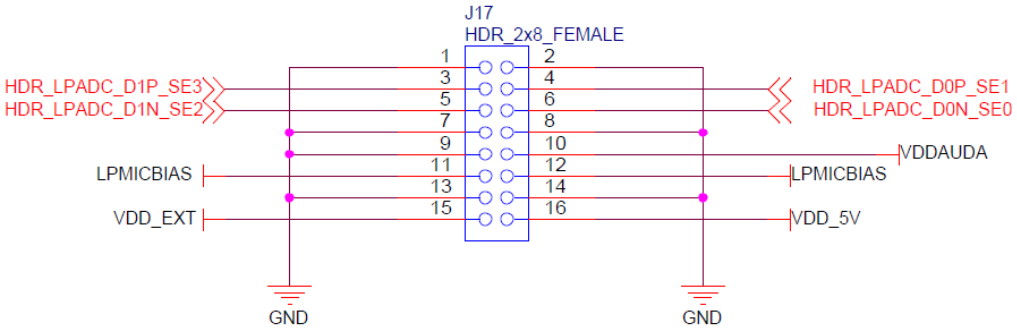

Figure 14. Audio Header J17

10. Ordering Information

Device Name	Orderable Part Number	EVB Revision	SoC	SoC Package	Temperature Range
Apollo4 Blue Plus EVB	AMA4BPEVB	1	Apollo4 Blue Plus - KBR Pkg	131-pin BGA	–20 to 60°C

Table 3: EVB Ordering Information

Device Name	Orderable Part Number	MRAM	RAM	Package	Packing	Temperature Range
Apollo4 Blue Plus SoC	AMA4B2KP-KBR	2 MB	2.75 MB	4.7 x 4.7 131-pin BGA	Tape and Reel	–20 to 60°C

Table 4: SoC Ordering Information

Ambiq Micro, Inc.
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