# Apollo4 Plus

## PRODUCT/PROCESS CHANGE NOTICE (PCN)

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|---|---|---|---|
| PCN Number: | CN-AP4C0-08232022 | Effective Date of Change: | June 10, 2022 |
| Issue Date: | 08/23/2022 | Running Change? | ☐ *Yes ☒ No |
| Contact: | Yvonne Chen | *If yes, add notes: | |
| Email: | ychen@ambiq.com | Attachment? | ☐ Yes ☒ No |

### Subject of Change

Updates to the Apollo4 Plus SoC final test program.

### Description of Change

☐ Design ☐ Assembly ☐ Electrical Specification ☐ Other:
☐ Wafer Fab ☒ Test ☐ Mechanical Specification

### Reason for Change

Updated final test program revision to version 4 for better test coverage.

### Part Numbers Affected

AMAP42KP-KBR

The first clean cut-off date code for the new test program is 222106. Material marked after this code is not affected by the changes described in this product notification.

### Change Identification

☐ Product Mark ☐ Label ☐ Data Code

☒ Other: No identification on top marking or shipping label. The Apollo4 Plus may be queried using AmbiqSuite to read back the trim revisions shown in Table 1. See product datasheet for more information.

### Risk Assessment:

Use AmbiqSuite revision 4.2 or later to implement VDDC_LV and temperature compensation power optimization. No code changes are required to maintain functionality from product tested with final test program version 3.

### Reliability/Qualification Summary

All units pass with new program.

### Customer Acknowledgement of Receipt

- Ambiq requires your acknowledgement of this notification within 30 days
- As this change belongs to notification-only PCN, no customer approval is required
- Ambiq will implement the change after the effective date

## Summary of Changes

1. PCM table update:
   - Boost VDDF active target by 20mV for crypto stability.
   - After the SBR/SBL has run, reduce VDDF (memldo active and simobuck VDDF active) by 3 codes (20mV) during power init on parts with trim version 6 and higher.
2. New crypto RSA functional screen binary:
   - Run crypto RSA functional screen with 7 codes of margin (~50mV) in LDO mode.
3. Update the DCOVER binary
4. FT1_GDR=4, Trim Rev=6
5. Update HFRC_CV=1; HFRC_CV=1
6. PatchWord = 0xFFFFFFF8
7. Summary:

Table 1: Final Test Update Summary of Changes

| Test Program Version | Version 3 | Version 4 |
|---|---|---|
| Description | Current Production | • Test program includes additional margin testing that supports VDDC_LV. It also enables power optimization for temperature compensation. This option can be configured via software using the AmbiqSuite SDK.<br>• Includes the crypto RSA screen |
| VDDC Trim Target | Current PCM Table (Trim Version 5) | • Current PCM table (trim version 5)<br>• Update dcover and SRAM walking test (LP and HP mode) to margin down VDDC by 30mV<br>• VDDC in active mode can be reduced by 10mV in software for the MSPI DMA restriction for additional power savings |
| VDDF Trim Target | Current PCM Table (Trim Version 5) | • Current PCM table (trim version 5) +20mV (for the crypto RSA screen)<br>• Update dcover and SRAM walking tests (LP and HP mode) to margin down VDDF by 60mV |
| Trim Version | 5 | 6 |
| GDR Test Program Version | 3 | 4 |
| Patch Tracker | | Patch tracker = 0xFFFFFFF8 (VDDF 20mV boost and HFRC CV bit) |