

ERRATA LIST

Artasie AMX8X5 RTC ER0007

Real-Time Clock devices with certain date codes

A-RTCA85-ELGA02EN v2.0



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Revision History

Revision	Date	Description
1.0	January 2020	Initial version
1.1	February 2020	Updated introduction, erratum details, and erratum expiration sections of the document.
1.2	August 2020	Updated scope of erratum to include the additional delay when existing from sleep mode. Updated date code list of affected devices (Added 1948, 1949, 1950, 1952, 2002, and 2004).
2.0	January 13, 2023	Updated document template.

Reference Documents

Document ID	Description

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SECTION

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Introduction

This document describes a silicon erratum which exists on AM0805B, AM0815B, AM1805B and AM1815B real-time clock (RTC) devices with certain date codes. For the devices affected by this erratum, the nRST power-up delay timing was trimmed differently which extends the nRST delay after power on and after exiting from sleep mode by an additional 100-300 ms.

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Affected Devices

This erratum applies to AM0805, AM0815, AM1805, and AM1815 RTC revision B silicon devices which have any of the following date codes: 1926, 1927, 1929, 1930, 1931, 1933, 1936, 1937, 1937, 1940, 1943, 1944, 1945, 1946, 1947, 1948, 1949, 1950, 1952, 2002 or 2004.

The date code of a device can be ascertained by reading the top marking on the IC. The top markings for each of the affected devices are shown below. The date code is highlighted in blue and is of the format YYWW, where YY is a two-digit representation for the year of production, and WW is the two-digit week number.

Figure 2-1: Package Top Marking Data Code

Part Number	AM0805AQ	AM0815AQ	AM1805AQ	AM1815AQ
IC top marking	AMBIQ 0805B AYYWW	AMBIQ 0815B AYYWW	AMBIQ 1805B AYYWW	AMBIQ 1815B AYYWW

For devices which are still packaged in the original shipping container, the date code is listed as shown on the example shipping label below, with the same YYWW format.

Figure 2-2: Shipping Label Date Code



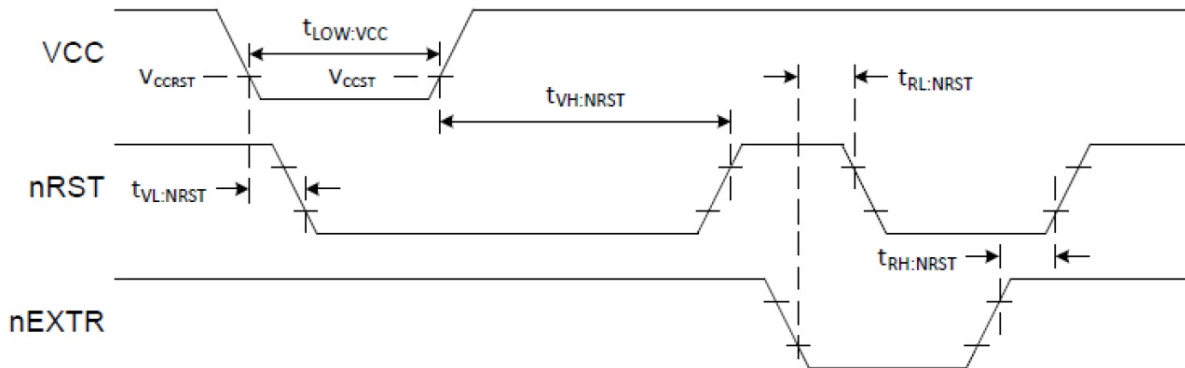
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Erratum Details

The nRST AC electrical characteristics are specified in the latest version of the datasheet. The timing diagram is shown below:

Figure 3-1: Normal nRST Timing Diagram



For the affected devices specified by this erratum, the delay to nRST high will be extended over the current datasheet specification due to different nRST delay timing on these devices. This increases the delay for nRST high after power-up reset ($t_{VH:NRST}$) as shown in Figure 3-2 on page 8, and after exit from sleep (t_{RSTIM}) as shown in Figure 3-3 on page 8, by an additional 100 – 300 ms.

Figure 3-2: VCC High to nRST High ($t_{VH:NRST}$) Delay Extension

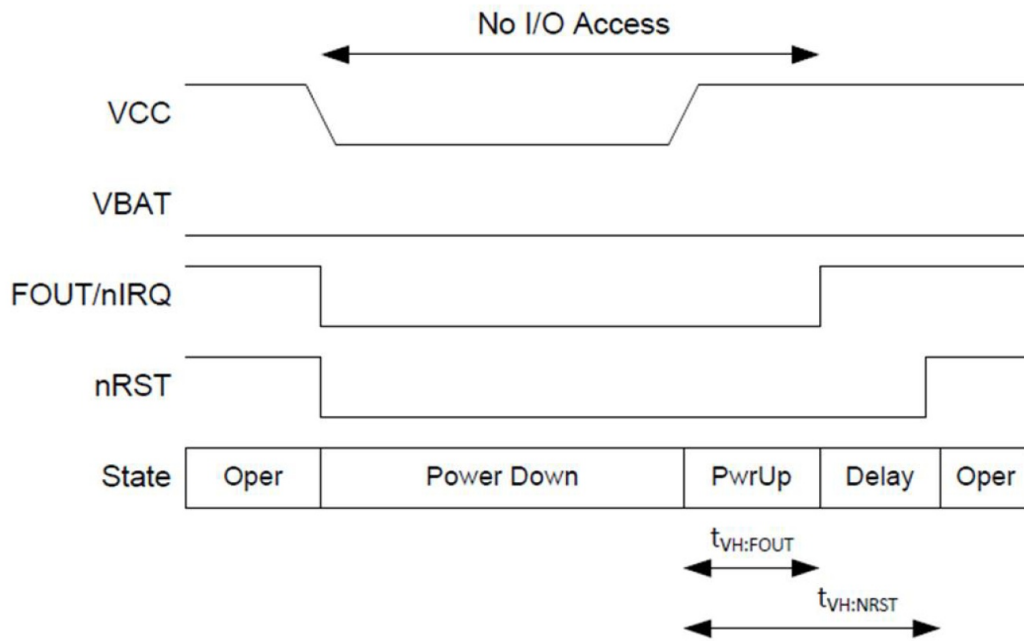
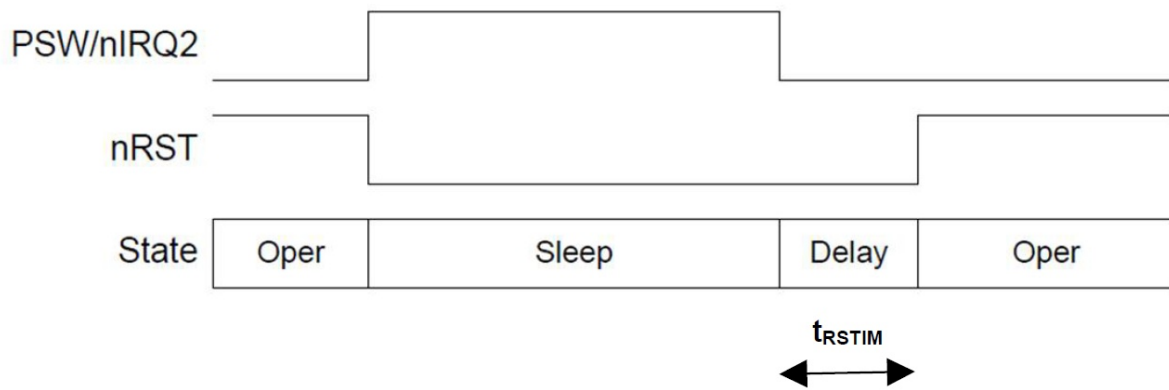


Figure 3-3: Sleep Exit (PSW/nIRQ2 Low) to nRST High (t_{RSTIM}) Delay Extension



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Application Impact

After power up and after exiting from sleep mode, there is an additional 100-300 ms delay before the nRST pin is de-asserted.

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Erratum Expiration

This silicon erratum applies only to the devices with date codes listed herein. Devices produced subsequent to these dates have been corrected and the described issue does not exist. If this issue is found to exist on devices of other date codes, this erratum will be updated accordingly.



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6500 River Place Boulevard, Building 7, Suite 200, Austin, TX 78730

www.ambiq.com

sales@ambiq.com

+1 (512) 879-2850

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