QUICK START GUIDE

Apollo510B EVB

(EVB Revision 2.0)

Ultra-low Power Apollo SoC Family

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1. Introduction

This document provides guidance for setting up the Apollo510B Evaluation Board (EVB), revision 2.0, part number AP510BEVB, to get started executing code examples, measuring power consumption in various configurations, and beginning software development.

FCC Regulatory Notice

This kit has not been authorized under the rules of the FCC. It is designed to:

1. Allow product developers to evaluate electronic components, circuitry or software associated with the kit to determine whether to incorporate such items in a finished product.
2. Enable software developers to write software applications for use with the end product.

This kit is not a finished product and may not be resold or otherwise marketed unless all required FCC authorizations are first obtained. **Developers using this reference design in their product are responsible for obtaining all required FCC equipment authorizations.**

Operation of this kit is subject to the condition that it does not cause harmful interference to licensed radio stations and that it accepts any harmful interference received. Unless the assembled kit is designed to operate under part 15, part 18, or part 95 of 47 CFR Chapter I - FCC, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of the latter chapter.

2. Document Revision History

Rev #	Date	Description
1.0	Sep 2025	Document initial public release
1.1	Nov 2025	Added important note about installing the Segger J-Link software in Software Development Tools section.

Table 1: Document Revision History

3. Reference Documents and Software

The latest version of the following items, which can be acquired through your Ambiq Sales contact, may be useful in understanding and using the EVB.

- EVB Schematic
- Apollo510B Datasheet
- Apollo510/Apollo510B Errata List
- AmbiqSuite SDK

4. Quick Start

The EVB Kit comes with the following items:

- Apollo510B Evaluation Board (EVB), revision 2.0
- USB Type C cable
- Four adhesive-backed rubber feet
- Extra jumpers

Caution: The EVB has components loaded on the back of the board. Care should be taken to not damage these components. The included rubber feet should be applied to the bottom of the board to prevent direct contact between the components and a desk surface.

The EVB comes with jumpers pre-configured for default operation. To start EVB program execution, connect the USB-C cable from a USB port on a PC to the J-Link USB connector (J16) on the EVB, and turn on the power switch (SW4). The green LED next to the power switch should illuminate.

The AmbiqSuite SDK provides many example programs that may be run on the EVB. To run these examples, download the SDK from the Ambiq Content Portal (https://contentportal.ambiq.com/login) and select any of the pre-built examples in the SDK at /boards/apollo510b_evb/examples. The examples should be programmed at address 0x410000.

5. Overview of the Apollo510B EVB

The Apollo510B EVB has the following features:

- Apollo510B Arm® Cortex®-M55 based SoC in the BGA package (AP510BFA-CBR)
- USB Type C connector for power/download/debug (J16)
- USB Type C connector for power/data to Apollo510B SoC (J18)
- On-board Segger J-Link debugger
- Debug-in port (J2) (SWD or ETM)
- Three user-controlled LEDs
- Two push buttons for application use, plus a reset push button
- Power slide switch with LED power indicator
- On-board interfaces:
  - MSPI x16 (Hex) PSRAM (AP Memory APS512XXN-AOB4BI-WBRZ)
  - SDIO 8 GB eMMC (ISSI IS21EF08G-JCLI)
  - High-speed expansion connector
  - MikroBUS socket interface
- General purpose male header (J8) for I/O and power access to a shield board
- High-speed connector (J7 - QSH-060-01-X-D-A) for interfacing to displays and/or high-speed memory
- RF switch/connector (Murata MM8430-2610RA1) for BLE PHY testing
- Test points for voltage measurements and jumpers for current measurements
- Solder bridge options for power supply flexibility and peripheral access options
- RoHS compliant

CAUTION: The EVB has components loaded on the back of the board. Care should be taken to not damage these components.

NOTE: This EVB may be used for non-BLE applications and in this use case, simply disregard the BLE features.

The following figures show the board layout, its major components and the location of all components.

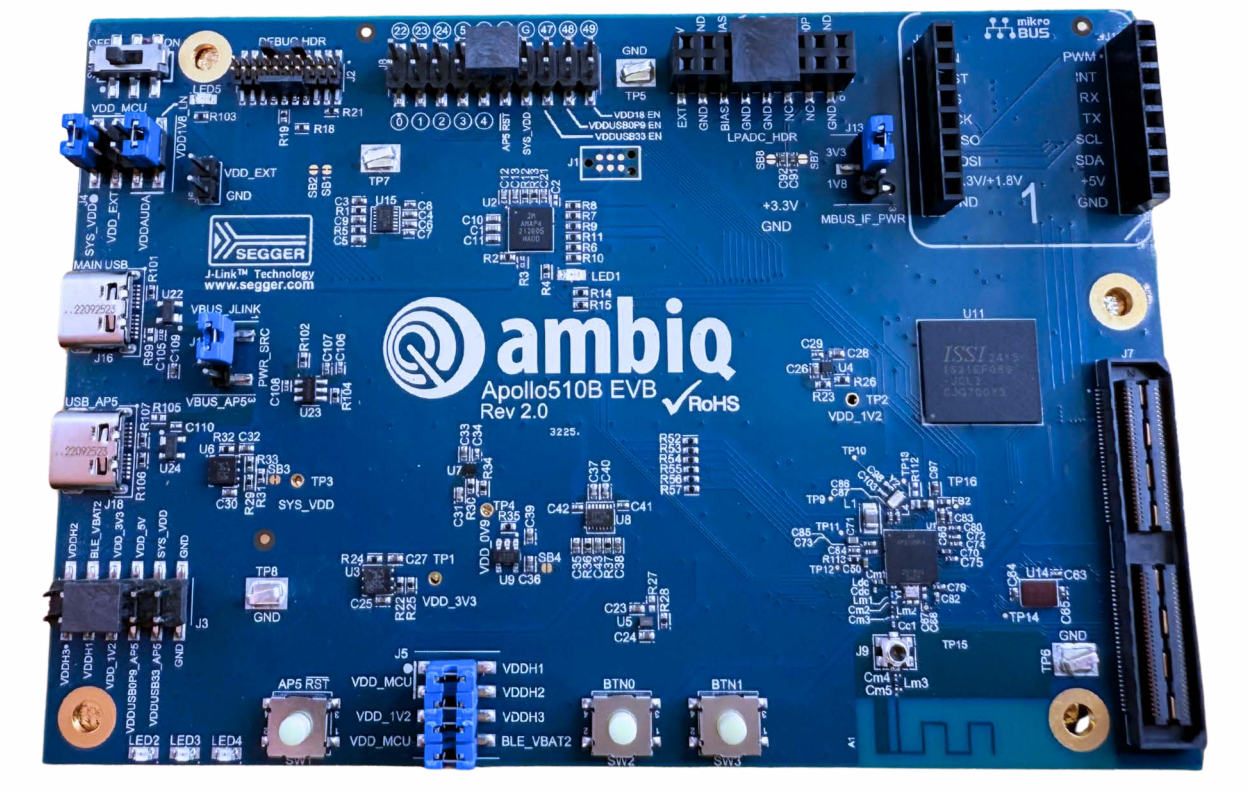


Figure 1. EVB Top View

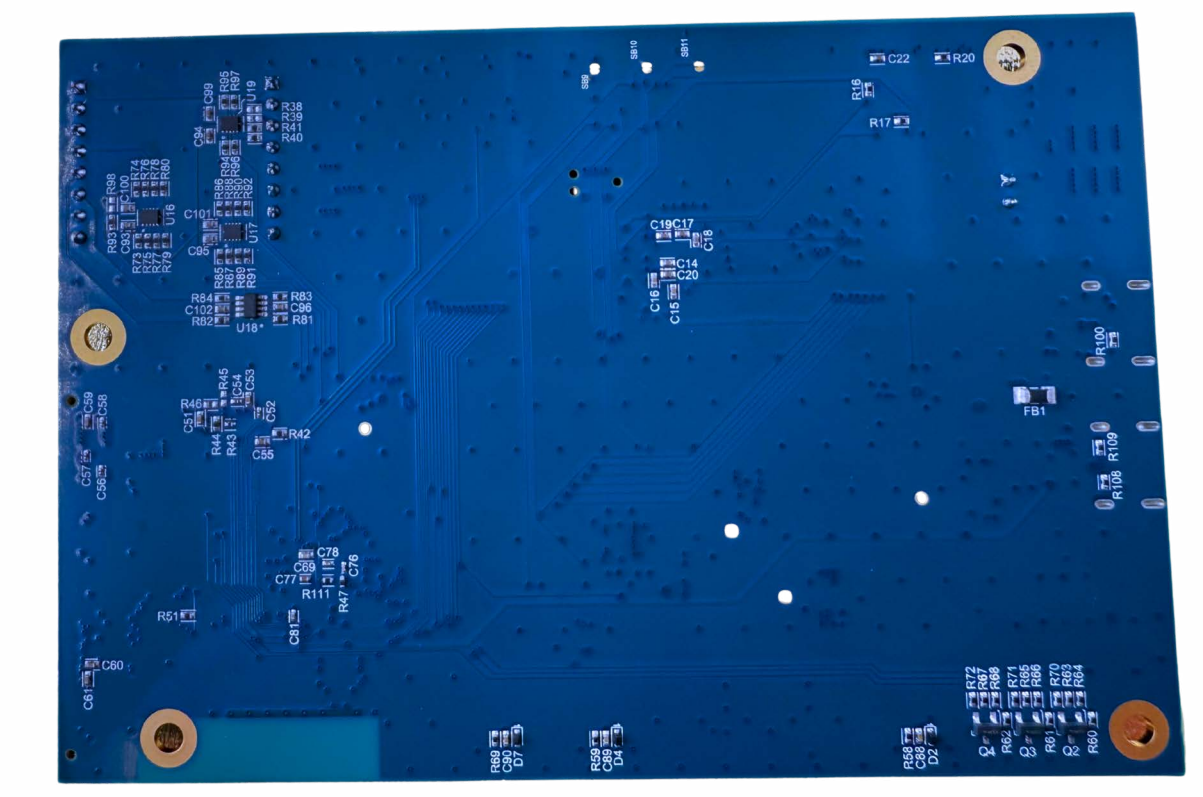
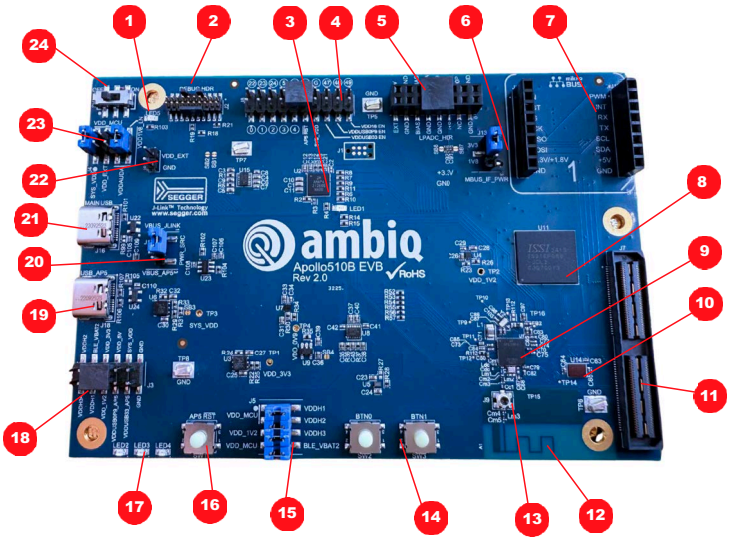


Figure 2. EVB Bottom View



1. Power LED
2. Debug in Connector
3. JLINK Controller
4. Dual-Row Header
5. Voice-on-SPOT (VOS) Connector
6. MikroBUS I/F Voltage Header
7. MikroBUS Conectors (2x)
8. eMMC0 - IS21EF08G-JCLI
9. Apollo510B BGA SoC (AP510BFA-CBR)
10. MSPI0 - APS512XXN-AOB4BI-WBRZ
11. High Speed Connector
12. PCB Trace Antenna
13. RF Switch/Connector
14. User Buttons (2x)
15. Power Configuration Header
16. Reset Switch
17. User LEDs (3x)
18. Power Test Points Header
19. Apollo5 USB Connector
20. Power Source Header
21. JLINK USB Comm
22. External Power Connector
23. SoC Supply Selection Header
24. Power Switch

Figure 3. EVB Major Components

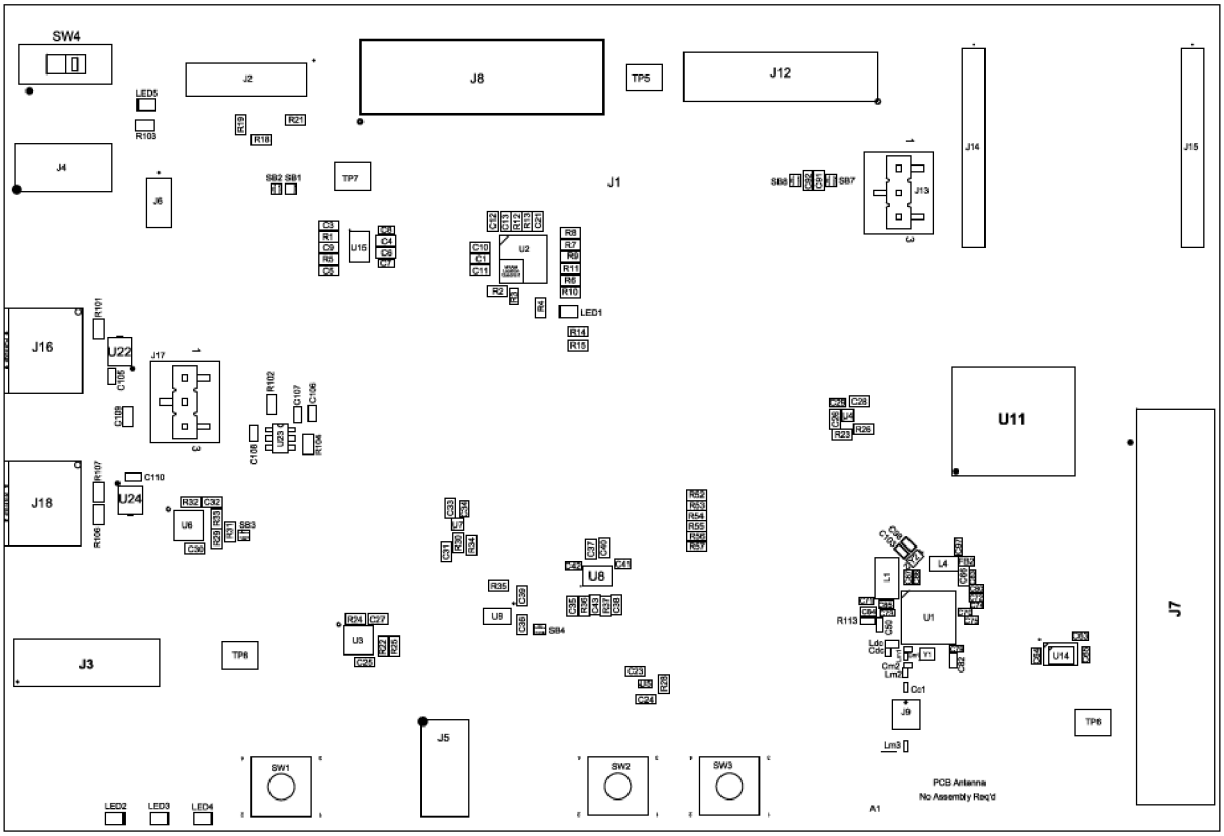


Figure 4. EVB Top Side Components

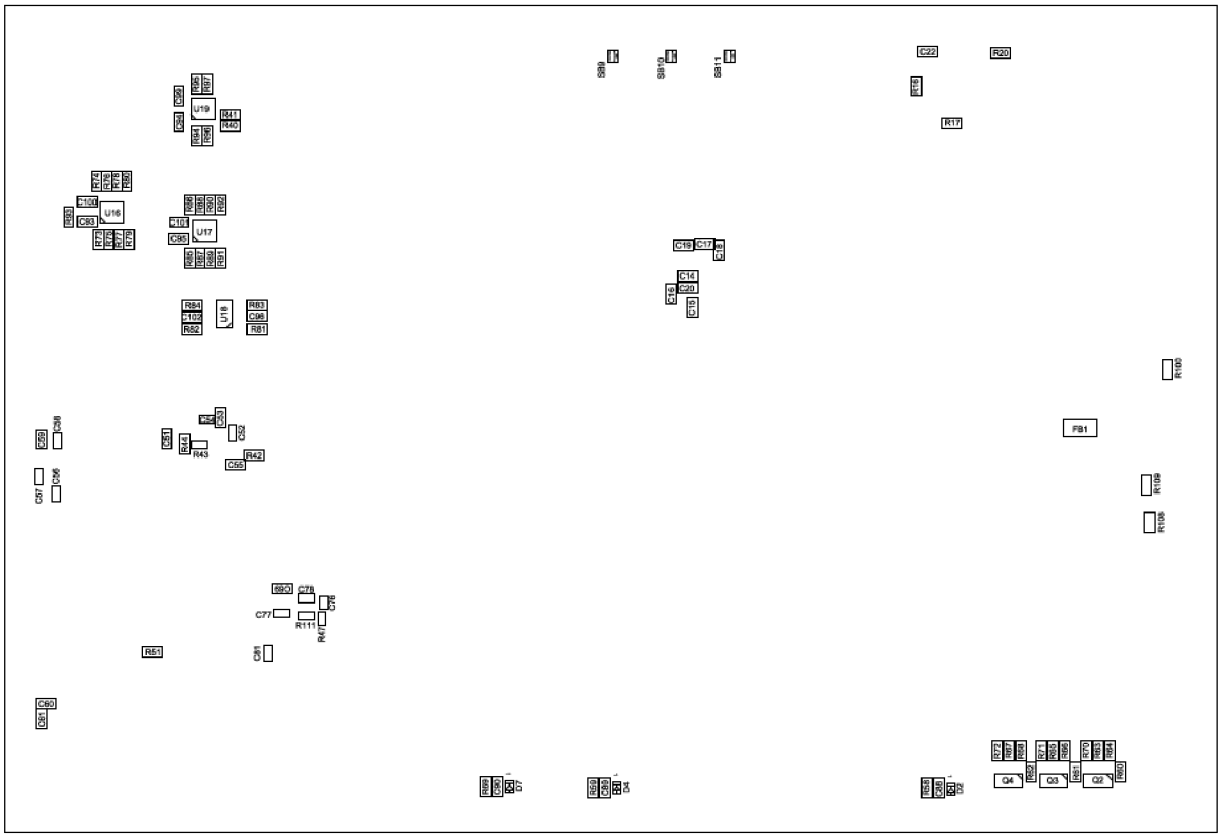


Figure 5. EVB Bottom Side Components

6. Secure Boot on the Apollo510B SoC

The on-board Apollo510B SoC is preprogrammed with a Secure Bootloader and an uninitialized Customer Info Space, referred to as INFO0. Initial provisioning of the part would include programming a valid INFO0 and programming the main firmware image in the flash.

The Apollo510B EVB is shipped with the INFO0 configuration pre-programmed with optimal settings for the EVB layout which would include the following features/settings:

1. Default boot to non-secure mode
2. Enable Boot Override to Push Button on GPIO46 (OTP setting) - BTN0 (SW2).
3. Enable wired updates over UART1
    A. UART1 is mapped to J-Link (OTP Setting).
    B. Baud rate is 115200 bps, no-parity, 8-bit data length, no flow control.
    C. Timeout is 5 seconds.

For reference, the following settings are programmed into INFO0 on the Apollo510B SoC resident on the EVB:

- Secure Bootloader (SBL) interface is configured to UART1 using GPIO12 and GPIO14, which allows secure boot to be performed over the J-Link COM interface of the EVB.
- SBL override pin is configured to GPIO46 which is Button 0 (SW2) on the EVB.

For information on changing the INFO0 settings as well as using the Secure Bootloader, please refer to the README.txt file found in the tools\apollo510_scripts folder of the latest SDK release supporting the Apollo5 family. This folder contains a number of python scripts to demonstrate generation of INFO0 settings, customer main images, and the creation of images for the Wired Update protocol over UART.

Please consult your Ambiq sales team for any additional documentation on INFO0 settings or Secure Bootloader, and visit the Content Portal for security documentation for the Apollo5 family.

7. Header Pin Assignments

This section provides an overview of the Apollo510B EVB connectivity and pin function options.

7.1 MikroBUS Headers

The Apollo510B EVB provides a MikroBUS header to enable rapid prototyping. The interface is accessed through headers J14 and J15 as shown in Figure 6. Function options for the GPIO on the header pins are as shown.

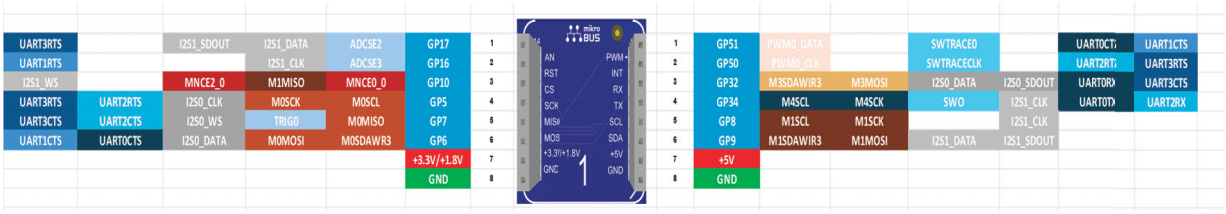


Figure 6. J14/J15 MikroBUS Headers - Function Options

7.2 General Purpose Headers

Function options for pins of general purpose header J8 are as shown in Figure 7.

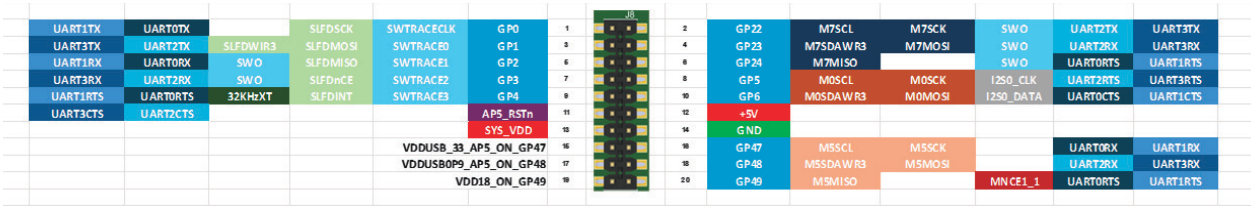


Figure 7. J8 General Purpose Headers - Function Options

There are 3 solder bridges (SB9-SB11) which will connect the 3 enable pins for load switching (2 for USB and 1 for MIPI DPHY) to the proper GPIOs on the Apollo510B. These 3 solder bridge connections are shown in Table 2. If the on-board load switching is not used (USB and MIPI are not used), each of these solder bridges can be cut and pins 16, 18, and 19 on J8 can be used as GPIO interface. In cases that after cutting SB9-SB11 the user would like to use the load switching again, jumpers can be installed between the J8 pins shown in Table 2 for a simpler method of connection.

Source	From Header Pin	To Header Pin	Destination
M5SCL_M5SCK_RX01_GP47	J8-16	J8-15	VDDUSB33_AP5_ON_GP47
M5SDA_M5MOSI_RX23_GP48	J8-18	J8-17	VDDUSB0P9_AP5_ON_GP48
M5MISO_TRIG0_RTS01_GP49	J8-20	J8-19	VDD18_ON_GP49

Table 2: J8 Default Solder Bridge Configuration Table

7.3 High-speed Header

Function options for pins of the high-speed header J7 are as shown in Figure .

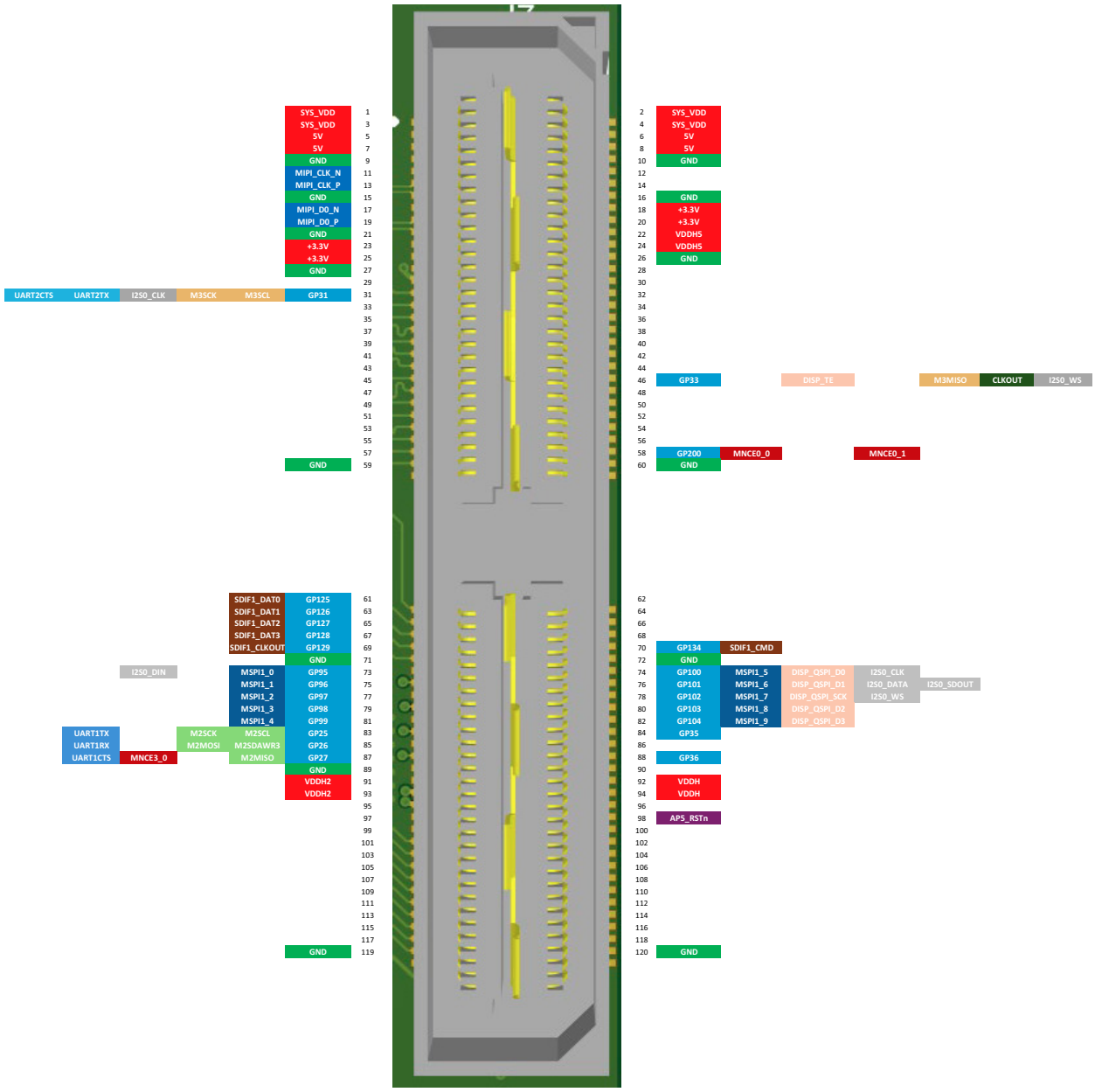


Figure 8. J7 High-speed Header - Function Options

Figure 9 shows board view of the J7 high-speed header which is located on the right edge of the EVB.

Figure 9. Board View of J7 High-speed Header

8. Debug Interface

Figure 10 shows the Apollo510B EVB set up for standard debug using the on-board J-Link debugger, selected by the PWR_SRC header (J17) set to VBUS_JLINK, connected through the MAIN USB connector (J16).

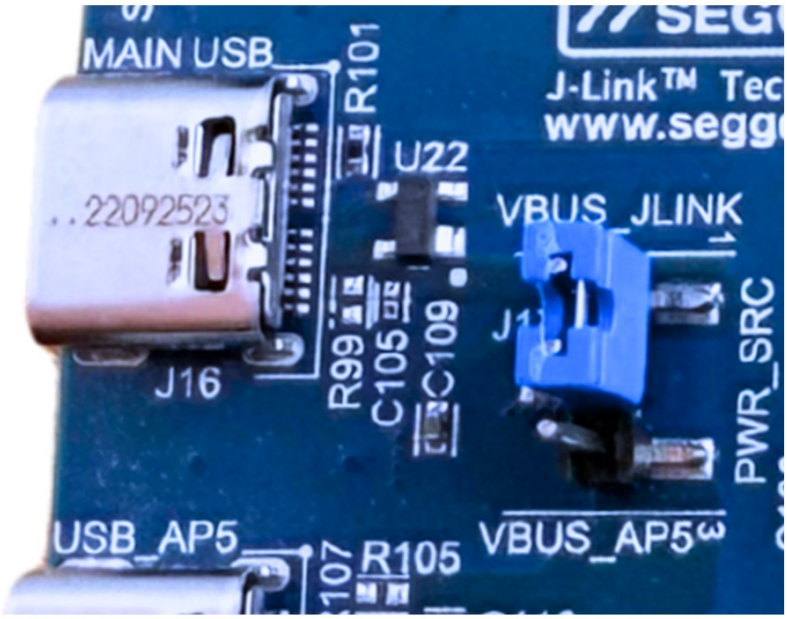


Figure 10. On-board J-Link Debug Connector (MAIN USB)

The debug interface is supported by standard J-Link drivers from Segger. Please refer to “Software Development Tools” on page 19 for more details on J-Link debug support.

8.1 Use of External Debugger

This EVB also supports the use of an external SWD debug interface through a 20-pin debug-in header (DEBUG HDR – J2) as shown in Figure 11. See the EVB schematic for connector pinout.

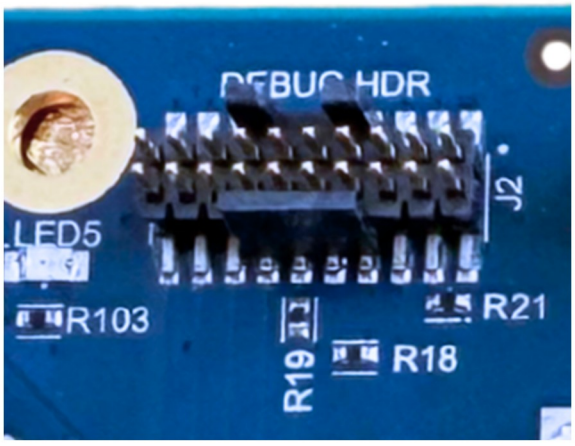


Figure 11. J2 Debug-In Header

No jumper changes are required to use an external debug adapter. Simply connect the external debug adapter with a ribbon cable connector to the “DEBUG HDR” header.

NOTE: Remove protective guard before attempting to connect to the debug header.

9. Software Development Tools

The standard Segger J-Link debug interface is used on the Apollo510B EVB. Regardless of IDE used, please install the Segger J-Link software - see https://www.segger.com/downloads/jlink. Refer to the AmbiqSuite SDK for version numbers of the IDEs used for that release, and see the \Ambiq-Suite\debugger_updates\ folder in the AmbiqSuite SDK for interim updates for Keil, IAR, and JLINK.

IMPORTANT NOTE
When installing the Segger J-Link software described above, it may be necessary to select the “Install Legacy USB Driver” option in order to properly enable the USB connection. This option is not selected by default in the Segger installation setup dialog box, so the checkbox has to be checked to install the legacy USB driver. (This is the only default installation option that needs to be changed when installing the software.)

10. Power Supply Options and Measuring Current

The Apollo510B EVB is intended to operate off a 5 V supply, which is used to generate down-stream voltages.

There are three options for the main power supply (VDD_MCU) for the EVB SoC:

- Operate at a nominal 1.8 V regulated down from the VDD_5V supply to source the on-board power rail SYS_VDD (default). Note that this voltage can be adjusted to 1.9 V by cutting SB3 shown on the Power Supplies page of the EVB schematic.
- Operate at 1.8 V via the low-noise VDD1V8_LN output of the regulated-down VDD_3V3 supply.
- Provide externally-supplied power via J6 (shown but not labeled) in Figure 12.

NOTE: If externally supplying VDD_MCU and/or VDDAUDA, which powers the analog audio and XTALHS crystal of Apollo510B, from VDD_EXT, the supplied voltage range must be in the specified range for the rail(s) being supplied:

- If externally supplying VDD_MCU and VDDAUDA, the allowable range is 1.71 V to 1.98 V.
- If supplying VDDAUDA from the VDD1V8_LN regulated output and not by externally supplied VDD_MCU, the allowable VDD_EXT range is 1.71 V to 2.2 V.
- If externally supplying VDDAUDA but not VDD_MCU, the allowable VDD_EXT range is 1.62 V to 1.98 V.

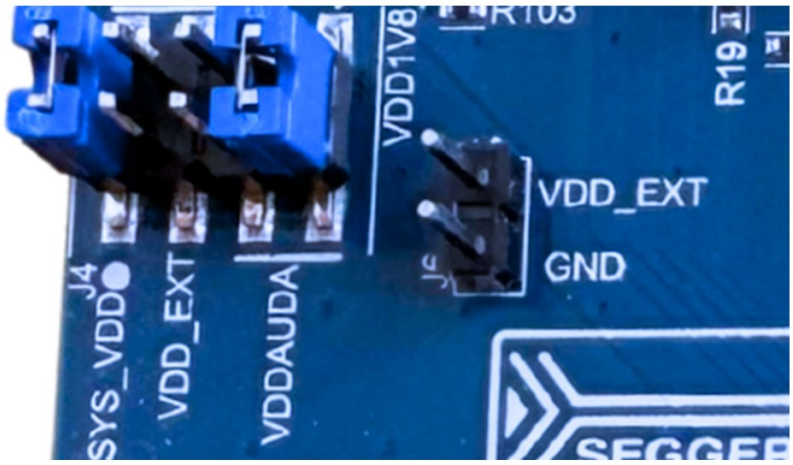


Figure 12. J6 External Supply Header

The EVB utilizes jumpers for connecting and disconnecting rails from power supplies, whether generated on-board or off-board. The following figures show the jumper connection strategy among various on-board power supplies and the SoC's power rails.

Figure 13 shows the power sourcing options for VDD_MCU.

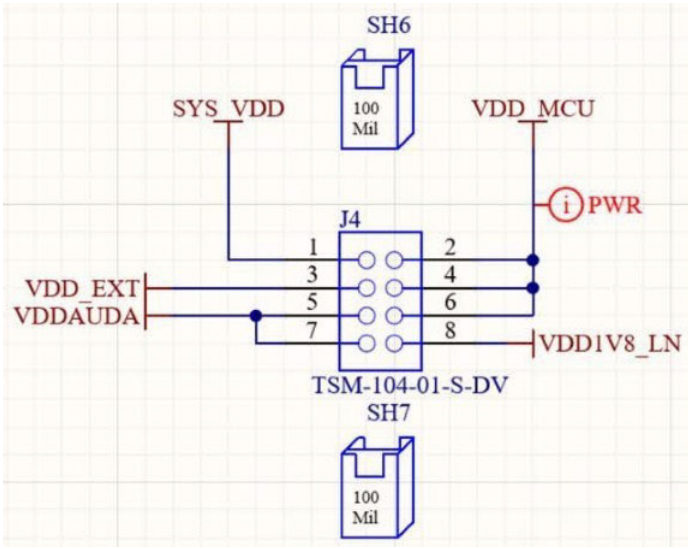


Figure 13. J4 Power Supply Jumper Connections

The J4 default jumper configuration is as shown in Figure 14 and in Table 3.

Figure 14. J4 Default Jumper Configuration

Power Supply Source	From Header Pin	To Header Pin	Power Supply Destination
SYS_VDD	J4-1	J4-2	VDD_MCU
VDD1V8_LN	J4-8	J4-7	VDDAUDA

Table 3: J4 Default Jumper Configuration Table

Figure 15 shows the power sourcing for VDDH1, VDDH2, VDDH3, and BLE_VBAT2. VDDH1, VDDH2 and BLE_VBAT2 are always sourced from VDD_MCU, and VDDH3 is always sourced from VDD_1V2. This header and jumpers are here solely for current measurements.

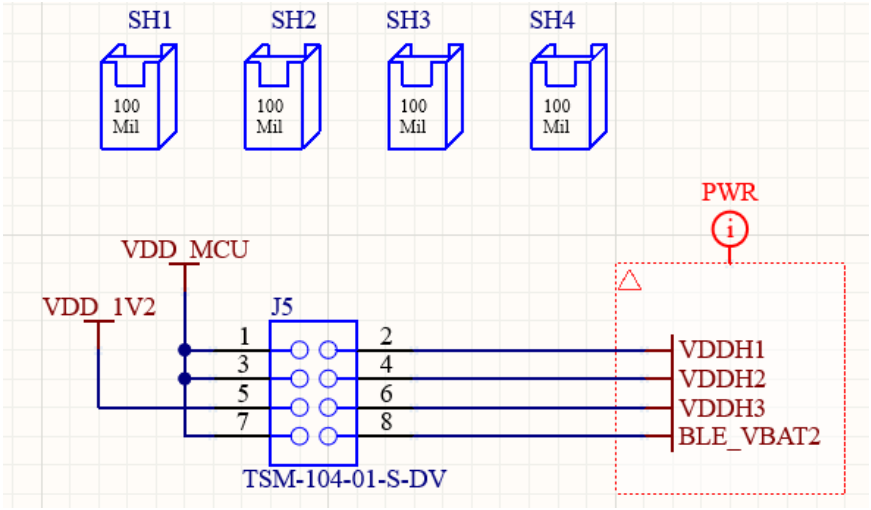


Figure 15. J5 Power Supply Jumper Connections

The J5 default jumper configuration is as shown in Figure 16.

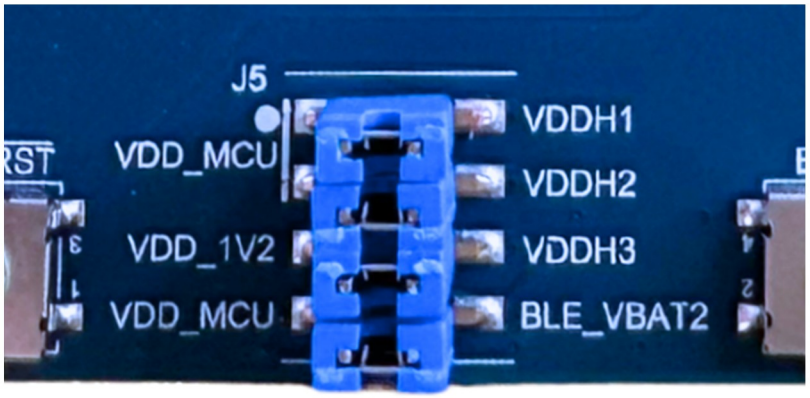


Figure 16. J5 Default Jumper Configuration

Power Supply Source	From Header Pin	To Header Pin	Power Supply Destination
VDD_MCU	J5-1	J5-2	VDDH1
VDD_MCU	J5-3	J5-4	VDDH2
VDD_1V2	J5-5	J5-6	VDDH3
VDD_MCU	J5-7	J5-8	BLE_VBAT2

Table 4: J5 Default Jumper Configuration Table

10.1 USB and VDD18/MIPI Load Switch Circuits

Figure 17 shows the USB load switch circuit producing the voltage supplied to VDDUSB33_AP5 and VDDUSB0P9_AP5.

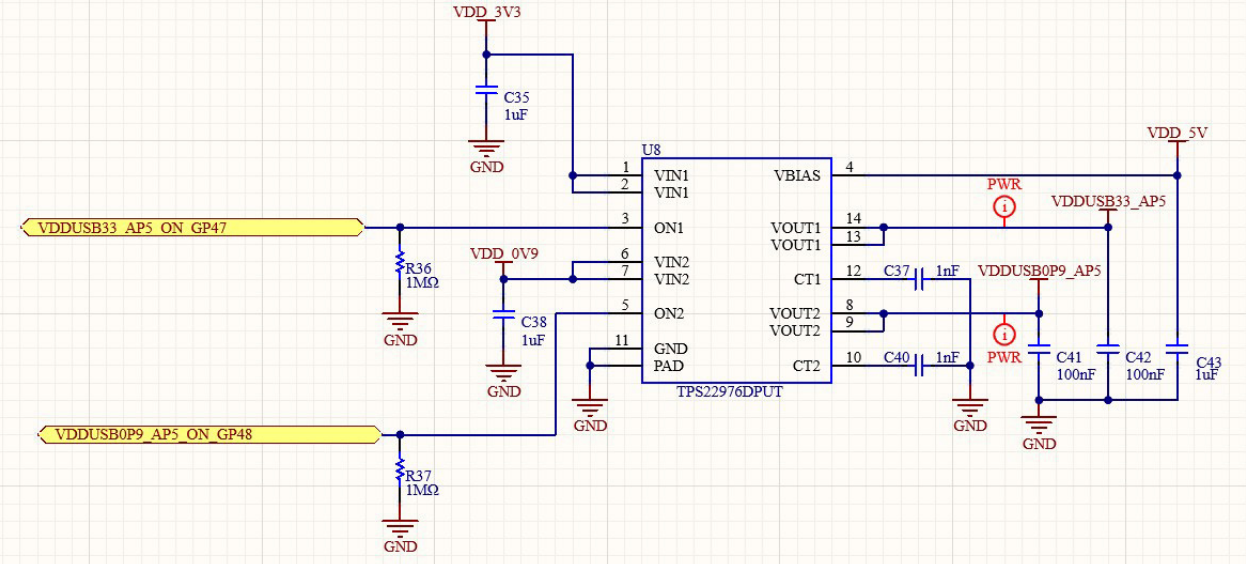


Figure 17. USB Load Switch Circuit

Similarly, Figure 18 shows the load switch circuit that produces the voltage supplied to the MIPI DPHY VDD18.

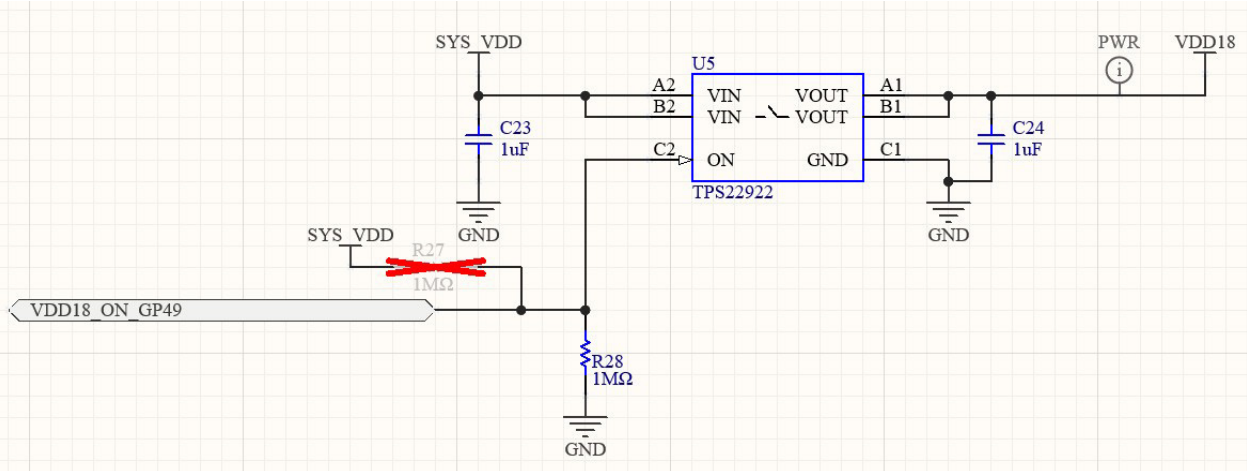


Figure 18. VDD18/MIPI Load Switch Circuit

10.2 Monitoring or Externally Supplying Supply Voltages

As shown in Figure 19 and Figure 20, header J3 provides easy access to the various system and chip-level power supplies present on the EVB. These can be used to monitor voltage or provide externally generated power to each specific rail after assuring that the on-board supply has been disconnected.

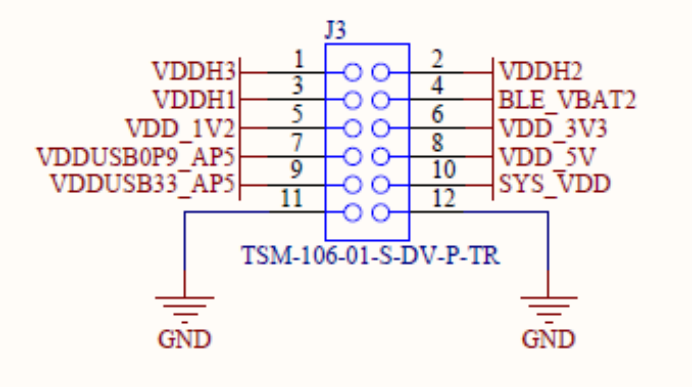


Figure 19. J3 Voltage Test Points Header

The J3 header is as shown in Figure 20. The header guard may need to be removed before connecting to or probing the header pins.

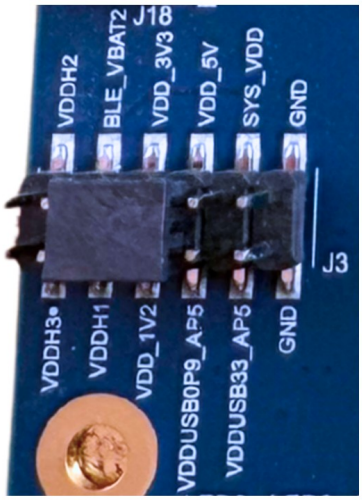


Figure 20. Board View of J3 Voltage Test Points Header

10.3 Measuring Current

Current consumption of the Apollo510B EVB can be measured by connecting an ammeter between the corresponding DUT supplies. Refer to Figure 12 or Figure 15 to measure the current draw from the power supply of interest. Before using an ammeter, turn the power off, remove the corresponding jumper and install the ammeter properly prior to powering the board back on. When the current measurements have been completed, reposition the jumper at its former location.

11. Ordering Information

Device Name	Orderable Part Number	EVB Revision	SoC
Apollo510B EVB	AP510BEVB	2.0	Apollo510B BGA

Table 5: EVB Ordering Information

Device Name[a]	Commercial Temp Range (-20°C to 70°C)	Package Type	GPIOs	NVM (MRAM)	SRAM	Package[b] Size (mm)
Apollo510B SoC	AP510BFA-CBR	BGA	96	4 MB	3.75 MB	5.6 x 5.6 x 0.8 153-pin BGA

Table 6: Apollo510B SoC Ordering Information

a. The silicon revision is identified by the first letter in the bottom row of the package's top marking.
b. Packing: Tape and Reel

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