DATASHEET

Apollo510B SoC

Ultra-low Power Apollo5 SoC Family

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Features

Arm® Cortex®-M55 Processor with Helium™ technology:

- Up to 250 MHz clock frequency
- Helium (MVE) AI accelerator, up to 8 MACs per cycle
- Scalar floating-point: double-/single-/half-precision arithmetic
- Supports Arm® TrustZone® security extensions
- Integrated 64 kB Instruction Cache and 64 kB Data Cache
- Integrated 768 kB Instr./Data Tightly Coupled Memory (TCM)
- Memory Protection Unit (MPU)

Bluetooth® Low Energy 5.4[1]

- Direction finding (single antenna)
- Long range support
- Tx power: up to +6 dBm output power
- Rx sensitivity: -94/-97/-103 dBm for 2Mbps/1Mbps/125 kbps

secureSPOT 3.0 Security Features

- Arm TrustZone technology
- Secure boot
- OTP key storage
- PUF-based identity/sign/verify
- Secure over-the-air (OTA) updates
- Key revocation

Ultra-Low-Power Memory

- Up to 4 MB of non-volatile memory (NVM) for code/data
- 3.75 MB of TCM and system RAM for code/data

Ultra-Low-Power Interface for On- and Off-Chip Sensors

- 12-bit ADC with 11 selectable ADC input channels
- Up to 2.8 MS/s effective continuous, multi-slot sampling rate
- Integrated temperature sensor

Rich Set of Clock Sources

- PLL for precise clocking applications
- 48 MHz and 32.768 kHz crystal (XTAL) oscillators
- Low Frequency RC (LFRC) oscillator
- High Frequency RC (HFRC) oscillator

Power management

- Operating Voltage: 1.71 V - 2.2 V
- Single inductor multiple outputs (SIMO) buck converter
- Multiple I/O voltages supported

Ultra-Low-Power Flexible Serial Peripherals

- 1x 2/4/8-bit SPI manager interfaces
- 1x 2/4/8/16-bit SPI manager interface supporting 1.2 V
- 7x I^2C/SPI managers for peripheral communication
- Full/Half Duplex SPI subordinate for host communication
- 4x UART modules with FIFOs and flow control
- 1x USB 2.0 FS/HS device controller
- 2x SDIO (SD3.0) / eMMC (v4.51)

Display

- MIPI DSI 1.2 up to 768 Mbps
- QSPI display interface (up to 125 MHz DDR)
- Up to 640 x 480 resolution at 60 FPS
- 4 layers with alpha blending
- Frame buffer decompression

graphiqSPOT 2.0 Graphics Features

- 2D/2.5D GPU with vector graphics (VG) acceleration
- 96 MHz / 250 MHz operating modes
- Anti-aliasing hardware acceleration
- Rasterizer / full alpha blending / texture mapping
- Texture / frame buffer compression (TSC4, 6, 6A and 12)
- Dithering and radial/conical fill support

Audio Processing

- 1x Low-power Audio ADC with PGA
- 1x PDM stereo DMIC interface
- 2x full-duplex multichannel I^2S port (1x with ASRC)

Applications

- Smart watches/bands
- Smart home devices
- Body-worn and ambient AI
- Wireless sensors and industrial edge
- Smart remotes
- Patient health monitoring

Ordering Information

AP510BFA-CBR: 5.6 x 5.6 x 0.8 (max) mm BGA (13 x 13 ball array), 153 pins, 96 GPIO, -20°C to +70°C

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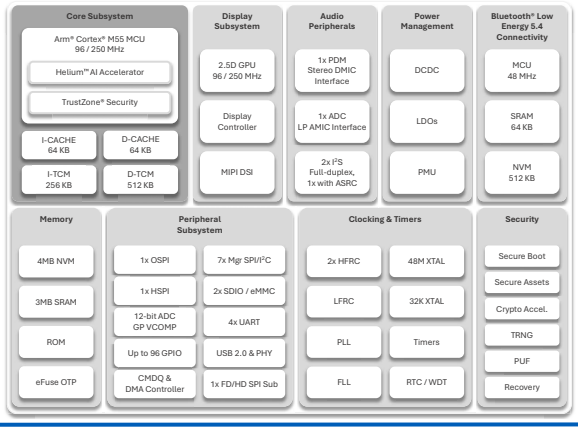

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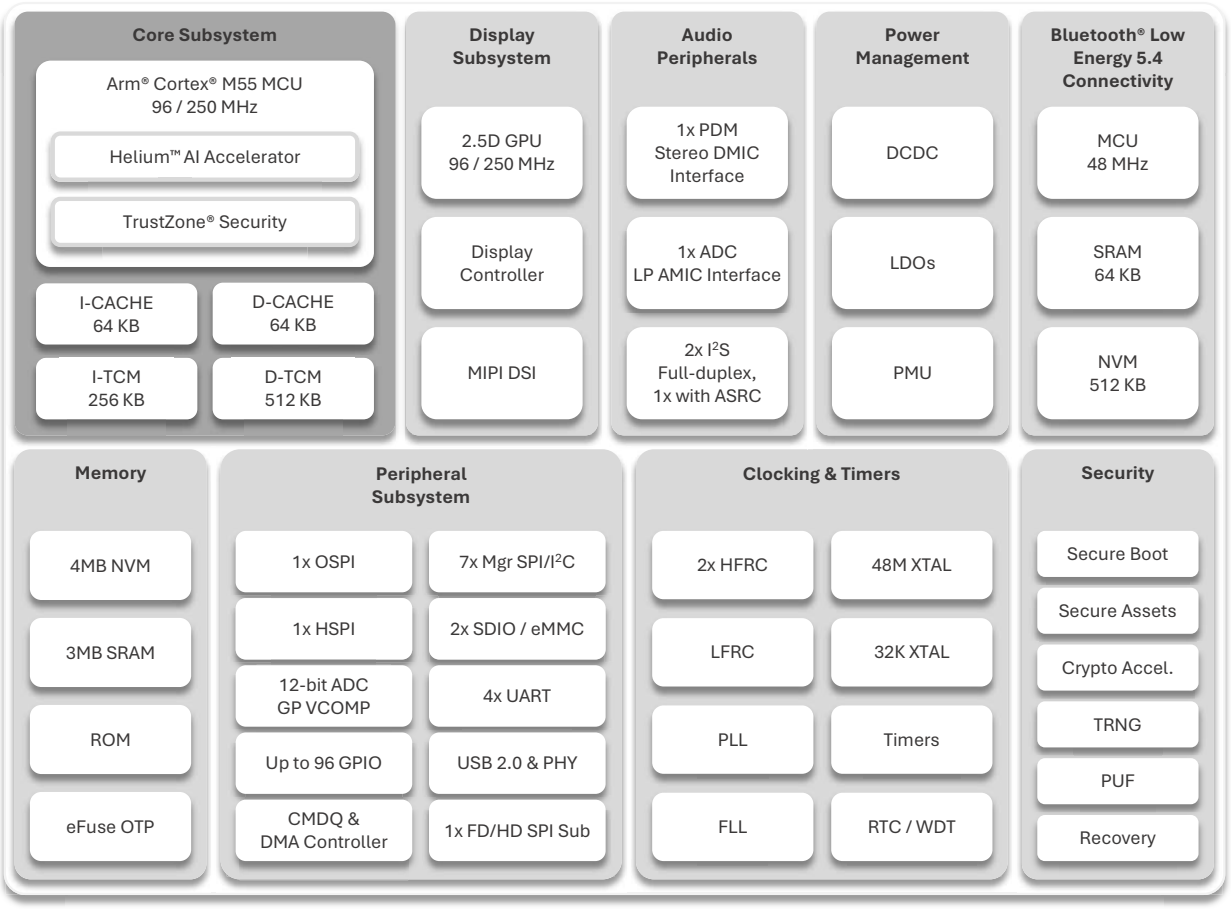

Figure 1. Apollo510B SoC High-Level Block Diagram

1.1 Features

The Apollo510B SoC is an ultra-low power, highly integrated, mixed-signal wireless SoC designed for battery-powered devices. It provides a significant enhancement in processing capability and highly integrated power management and audio capabilities to the Apollo SoC product family. The Apollo510B SoC brings the powerful Arm® Cortex-M55 processor with the Extension Processing Unit which supports M-Profile Vector Extension (MVE) processing and floating point operations, coupled with the world's lowest power audio and communications processing. The SoC takes the Ambiq Micro's patented Subthreshold Power Optimized Technology (SPOT) platform to a whole new level of compute power efficiency, setting new industry benchmarks in low power design and high efficiency portable computing.

The Apollo510B SoC features a state-of-the-art 2.4 GHz transceiver which is Bluetooth® Low Energy 5.4 compliant. Included are a low-power receiver with excellent sensitivity and selectivity, and a programmable transmitter supporting up to +6 dBm for optimized output power and current consumption.

NOTE

Any references to the Apollo5 Family herein apply to all existing derivatives of the Apollo5 SoC family. If a feature or function described herein applies to a specific derivative and/or does not apply to all derivatives, the exception(s) will be noted in the applicable context.

The Apollo510B SoC includes features shown in Figure 1 and listed below.

Arm® Cortex®-M55 Application Processor with Helium™ technology:

- Up to 250 MHz operating modes
- Helium (MVE) AI accelerator, up to 8 MACs per cycle
- Scalar floating-point: double-/single-/half-precision arithmetic
- Integrated 64 kB Instruction Cache and 64 kB Data Cache
- Integrated 256 kB Instruction Tightly Coupled Memory (ITCM) and 512 kB Data TCM (DTCM)
- Memory Protection Unit (MPU)
- Wake-up Interrupt Controller (WIC) with 135 interrupts

Bluetooth Low Energy 5.4[1]:

- Full Bluetooth 5.4 Implementation
- Direction finding (single antenna)
- High Data Rate (HDR) and Long Range (LR) support
- Angle of Arrival (AoA) and Angle of Departure (AoD)
- -94 / -97 / -103 dBm RX sensitivity for 2 Mbps / 1 Mbps / 125 kbps and 37 byte payload
- -20 to +6 dBm transmitter output power range

secureSPOT 3.0 Security Features:

- Arm TrustZone® technology
- Secure boot
- OTP key storage
- PUF-based identity/sign/verify
- Secure over-the-air (OTA) updates
- Key revocation

Ultra-Low-Power Memory:

- Up to 4 MB of non-volatile memory for code/data
- Up to 3.75 MB of low-leakage system RAM for code/data

Ultra-Low-Power Interface for On- and Off-Chip Sensors:

- 12-bit ADC with 11 selectable input channels
  - 10-bit ENOB
  - Up to 2.0 MS/s (12-bit Mode) / 2.8 MS/s (8-bit Mode) effective continuous, multi-slot sampling rate
  - Integrated temperature sensor

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- Voltage comparator

Ultra-Low-Power Flexible Serial Peripherals:

- 7x I^2C/SPI managers for peripheral communication
- 1x 2/4/8-bit SPI manager interface up to 96 MT/s
- 1x 2/4/8/16-bit SPI manager interface up to 250 MT/s
- 1x Full Duplex or Half Duplex SPI subordinate with DMA support for host communication
- 4x UART modules with 32-location Tx and Rx FIFOs with flow control and DMA support
- 2x SDIO controllers allowing concurrent SDIO (v3.0) / eMMC (v4.51) interface with DMA
- USB 2.0 HS/FS device controller with DMA

Display Controller:

- QuadSPI display interface supporting up to 125 MT/s
- Up to 1920 x 1080 resolution[1]
- 4 layer with alpha blending
- Frame buffer decompression
- LCD controller interface

graphiqSPOT 2.0 Graphics Features:

- 2D/2.5D GPU with enhanced Vector Graphics (VG) acceleration
- 96 MHz / 250 MHz operating modes
- Anti-aliasing hardware acceleration
- Rasterizer
- Full alpha blending
- Texture mapping
- Texture and frame buffer compression:
  - 4-bit
  - 6-bit (with/without Alpha)
  - 12-bit (with/without Alpha)
- Dithering support
- Radial/conical fill

Audio / Communication Processing:

- Support for one LP analog microphone using two PGA channels (low gain and high gain)
- 2x full-duplex multichannel I^2S ports - 1x with Asynchronous Sample Rate Converter (ASRC)
- Ultra low power voice and keyword detect
- PDM interface with support for 1 set of stereo high precision/low power digital microphones

Rich set of clock sources:

- High precision / low jitter PLL for high-fidelity audio and high-speed USB
- High frequency 48 MHz crystal (XTAL) oscillator
- 32.768 kHz XTAL oscillator

1. Ignoring frame rate, the Display Controller can support up to 1920 x 1080 resolution. The resulting frame rate at any particular resolution depends upon display interface speed, bus-fabric bandwidth and complexity of the graphics assets and related operations. Typically a resolution of 640 x 480 at 60 frames/second can be supported for most applications.

- 2x high frequency RC oscillators – 192/250 MHz
- Nominal 900 Hz Low Frequency RC (LFRC) oscillator
- RTC based on Ambiq's AM08X5/18X5 families

Power Management:

- Operating ranges:
  - Voltage: 1.71 V - 2.2 V
  - Temp Range[1]: -20°C to 70°C
- Single Inductor Multiple Outputs (SIMO) Buck Converter
- Multiple I/O voltage domains supported (independent voltage rails)

Package(s):

- 5.6 mm x 5.6 mm, 13 x 13 BGA (153 pins / 96 GPIO)

1. See Ordering Information section for other available temp/package options.

1.2 Functional Overview

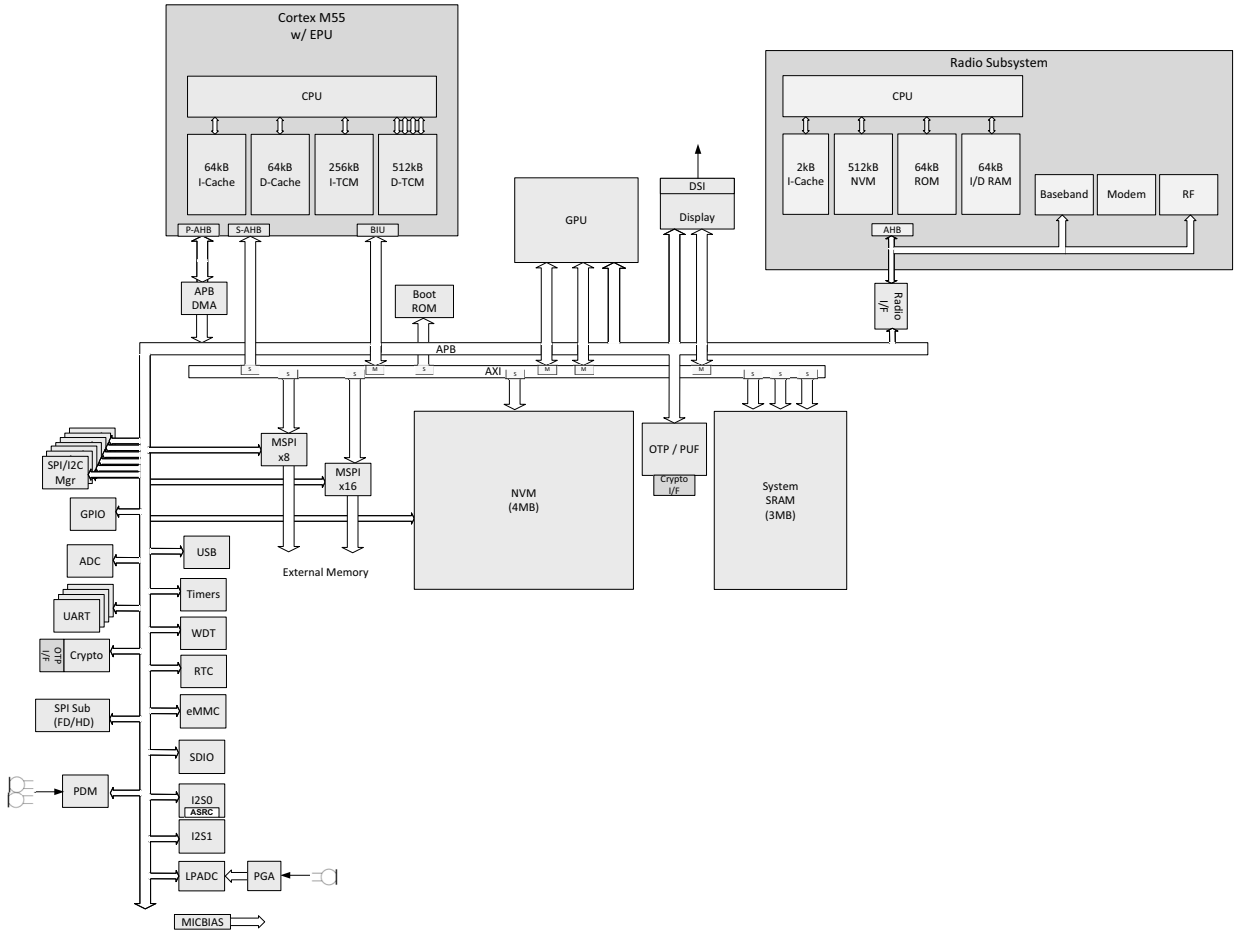

Figure 2. Apollo510B SoC Detailed Block Diagram

The ultra-low power Apollo510B SoC, shown in Figure 2, provides an ideal solution for battery-powered applications supporting near- to far-field audio processing. In a typical system, the SoC serves as an applications processor with fully integrated audio subsystem and BLE 5.4 radio communications. The Apollo510B SoC includes an extensive set of digital and analog peripheral interfaces with integrated ADCs and digital sensor processing using the integrated serial manager ports. The Cortex-M55 core with Helium™ technology, also known as the M-Profile Vector Extension (MVE), integrated in the Apollo510B SoC is capable of running complex data analysis and sensor fusion algorithms to process the sensor data and orchestrate complex audio processing signal flows. The Cortex-M55 core leverages a broad development and support ecosystem to accelerate time-to-market for application and product deployment.

The Apollo510B SoC adds wireless connectivity through an integrated low power Bluetooth Low Energy 5.4 controller and transceiver. A dedicated processor runs the controller stack with independent NVM/ SRAM memory to fully offload the main CPU. The radio supports long range, high data rate, and LE audio with a high sensitivity receiver and programmable transmitter up to +6dBm.

In other configurations, a host processor can communicate or share data with the Apollo510B SoC over its serial subordinate port using its SPI interface or by using the I^2S audio streaming interface module, both of which support full duplex data transfer. With unprecedented energy efficiency for sensor conversion, audio processing and data analysis, the SoC enables months and years of battery life for products only achieving

days or months of battery life today. Similarly the device enables the use of significantly complex algorithmic processing due to its industry leading low active mode power. By using the Apollo510B SoC, artificial intelligence at the portable edge (Edge AI) is truly brought to life.

The Apollo510B SoC supports various operating modes to maximize energy efficiency depending on the workload demand. For extremely power-sensitive workloads, it supports a low power operating mode leveraging Ambiq Micro's patented SPOT technology to achieve industry leading energy efficiency. For timing critical or higher MIPs workloads, the device supports high performance operating modes through Ambiq Micro's TurboSPOT technology. The TurboSPOT technology enables high performance while still maintaining extremely high energy efficiency operation. The device also supports secure boot using Ambiq's SecureSPOT technology enabling applications to establish and maintain a root of trust from boot to execution.

The Apollo510B SoC brings enhanced display and user interface capabilities with a rich set of display and graphics features. The display controller supports MIPI DSI and other serial/parallel display interfaces. Up to 4 layer composition and blending is supported with full CPU offload. A powerful 2.5D graphics controller enables a rich UI experience without compromising on power. Frame buffer compression is supported to minimize storage and bandwidth requirements.

A rich set of sensor peripherals enable the monitoring of several sensors. An integrated temperature sensor enables the measurement of ambient temperature. A scalable ultra-low power Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) monitors the temperature sensor, several internal voltages, and up to eight external sensor signals. The General Purpose ADC is uniquely tuned for minimum power with a configurable measurement mode that does not require MCU intervention.

In addition to integrated analog sensor peripherals, I^2C/SPI manager ports and/or UART ports enable the MCU to communicate with external sensors that have digital outputs.

The Apollo510B SoC integrates a full audio subsystem supporting one set of stereo PDM microphones, one analog microphone and two full duplex I^2S manager/subordinate ports, one with ASRC support. Additionally, ultra low power wake on voice and wake on keyword is supported.

For higher bandwidth peripherals, the Apollo510B SoC supports one Multi-bit SPI (MSPI) controller for 1-bit, 2-bit, 4-bit and 8-bit data, and one MSPI controller capable of up to 16-bit data (two MSPI controllers total).

The Apollo510B SoC also includes a set of timing peripherals and an RTC. The general purpose Timer/Counter Module (TIMER), 32-bit System Timer (STIMER), and the RTC may be driven independently by one of four different clock sources:

- Low frequency RC oscillator
- High frequency RC oscillator
- 32.768 kHz crystal oscillator
- High frequency crystal oscillator

The Apollo510B SoC supports highly optimized PWM pattern generation for complex, efficient control operation.

To facilitate development and debug, the Apollo510B SoC is supported by a complete suite of standard software development tools. Ambiq Micro provides drivers for all peripherals along with basic application code to shorten development times. Software debug on the Cortex-M55 is facilitated by the addition of an Instrumentation Trace Macrocell (ITM), Embedded Trace Macrocell (ETM) and a Trace Port Interface Unit (TPIU). The debug functions are accessible via Serial Wire Debugger (SWD).

In addition, the Performance Monitoring Unit (PMU), a powerful tool used for code profiling and optimization, is available to aid developers' debugging and application optimization.

1.3 Differences between Apollo510 and Apollo510B SoCs

The primary feature and functional differences between the Apollo510 SoC and the Apollo510B SoC are summarized in Table 1.

Table 1: Feature and Functional Differences between the Apollo510 and the Apollo510B

Feature/Functionality	Apollo510 SoC	Apollo510B SoC
BGA Package Size	6.6 mm x 6.6 mm, 16 x 16 (225 pins / 183 GPIO)	5.6 mm x 5.6 mm, 13 x 13 (153 pins / 97 GPIO)
Bluetooth Low Energy 5.4 Controller	-	✓
2/4/8-bit SPI manager interface (MSPI) up to 96 MT/s	2x	1x
2/4/8/16-bit SPI manager interface (MSPI) up to 250 MT/s	2x	1x
I2C/SPI managers	8x	7x
Half-duplex only I2C/SPI subordinate (IOS)	1x	-
Display: DPI-2 and DBI-Type B/C	✓	-
Display: 8080 display support	✓	-
Display: 6-bit parallel interface for color Memory-in-Pixel	✓	-
SDIO: SDIO1 transfer rate and data width	SDIO1 transfers data in 8-bit eMMC mode for 96 MB/s maximum transfer rate	SDIO1 transfers data in 4-bit eMMC mode for 48 MB/s maximum transfer rate
Clocks: High frequency XTAL oscillator	Multiple frequencies supported	48 MHz only. A div-by-4 of this clock (12 MHz) is internally available and used to clock other modules.

2. CPU Subsystem

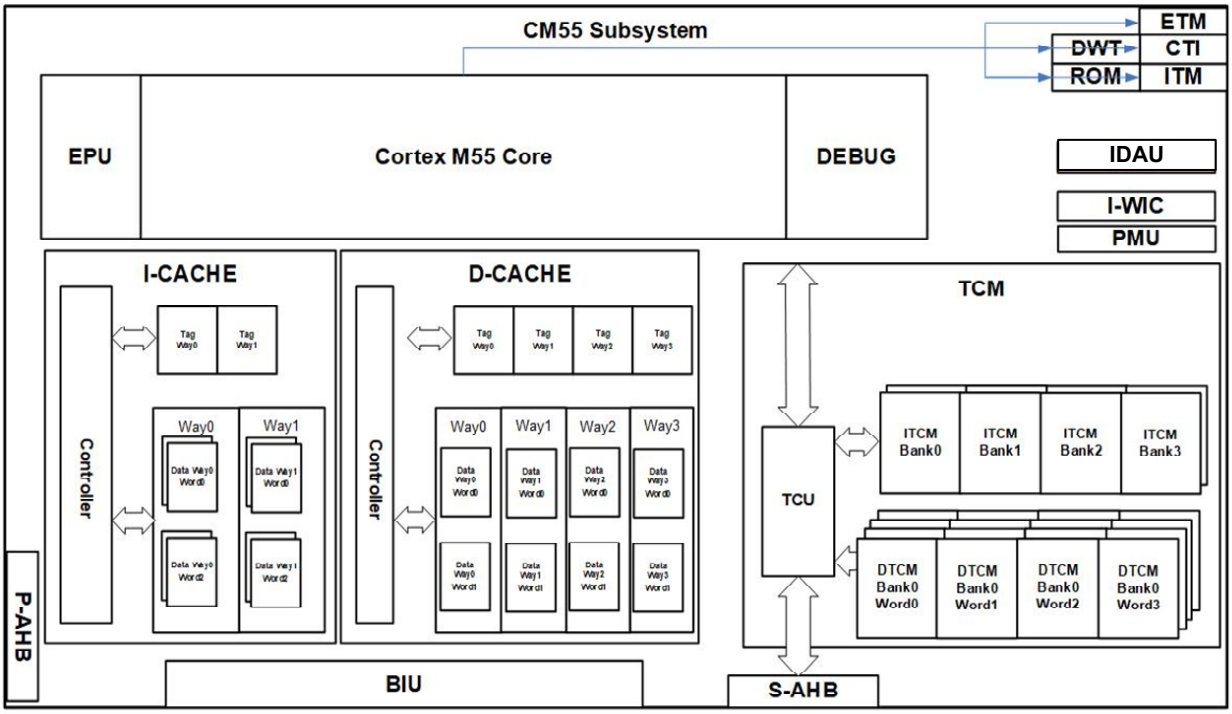

Figure 3. Apollo5 SoC Family CPU Subsystem Block Diagram

2.1 Features

The CPU subsystem (or CPU complex) includes features as shown in Figure 3 and is composed of an Arm Cortex-M55 CPU with Helium technology, instruction and data caching, instruction and data tightly coupled memory, interrupt and debug logic as well as the associated power management control for the subsystem. The subsystem has the following features:

- Cortex-M55 with Helium technology
  - Half-Precision, Single-Precision and Double Precision Floating Point
  - Vector Processing supporting integer, half-precision and single-precision vector arithmetic
- Arm®v8.1-M ISA with DSP and Security Extensions
- TrustZone® technology support
- Operating Modes
  - 96 MHz Low Power Mode
  - 250 MHz High Performance Mode
- Internal WIC (iWIC) supported
- Memory Protection Unit: 16 non-secure and 16 secure memory regions
- Security attribution Unit: 8 regions
- Debug
  - Embedded Trace Macrocell (ETM)
  - 8x data watchpoint comparators and 8x breakpoint comparators
  - ITM/DWT supported
- CPU Power Management block
- 64 kB Instruction Cache / 64 kB Data Cache
- 256 kB Instruction TCM / 512 kB Data TCM

NOTE

Limitations of DMA operations include the following:

- Transferring between memory/NVM (DTCM, SSRAM, NVM) source and destination is not supported as the APBDMA does not have the capability to transfer from memory to memory. When DTCM is the source of the DMA transfer, the transfer should target a peripheral.
- A DMA operation cannot be performed to or from DTCM when the CPU is in deep sleep or the DTCM location is powered down.
- A DMA transfer must not cross a DTCM 4 kB boundary.
- A DMA transfer must not cross the MRAM0-MRAM1 boundary at address 0x600000 on devices with two MRAM partitions. See Cortex-M55 CPU Memory Map in “Memory Maps” on page 33.

2.2 Functional Overview

At the center of the Apollo510B SoC is a 32-bit Arm Cortex-M55 core with floating point and vector processing (Helium technology) option. This implementation of the ArmV8.1-M architecture offers highly efficient processing in a very low power design. The Arm M DAP enables debugging access via a Serial Wire Interface from outside of the MCU which allows access to all of the memory, processors and peripheral devices of the SoC. The Apollo510B SoC supports the Cortex-M55 with Helium technology enabling high efficiency compute non-secure processing support. TrustZone ISA extensions are supported to enable secure computing.

The CPU complex has 64 kB of instruction caching and 64 kB of data caching, as well as 256 kB instruction and 512 kB of TCM. In addition, the CPU has access to 3 MB of total shared system SRAM, 4 MB of non-volatile memory and up to 2x 64 MB, 1x 128 MB and 1x 256 MB external memory interfaces. All of the memory is memory mapped and accessible by the CPU. All of the memory accesses are qualified based on the memory protection attributes (enforced within the Cortex-M55) and the system memory protection attributes (enforced within the system memory controllers).

The Cortex-M55 processor supports the Arm®v8.1-M Protected Memory System Architecture (PMSA) that provides programmable support for memory protection using a number of software controllable regions. Memory regions can be programmed to generate faults when accessed inappropriately by unprivileged software reducing the scope of incorrectly written application code. The architecture includes fault status registers to allow an exception handler to determine the source of the fault and to apply corrective action or notify the system.

Reference the “Arm Cortex-M55 Processor Technical Reference Manual” for more details.

2.3 Memory Protection Unit (MPU)

The Apollo510B SoC includes an MPU which is a core component for memory protection. The Cortex-M55 processor supports the Arm®v8.1-M Protected Memory System Architecture (PMSA). With the Security Extension, the Cortex-M55 supports both an MPU for the non-secure domain and an S-MPU for the secure domain.

The MPU is an optional component and, when implemented, provides full support for:

- Protection regions
- Access permissions
- Exporting memory attributes to the system

MPU mismatches and permission violations invoke the MemManage handler. See the “ArmV8.1-M Architecture Reference Manual” for more information.

The MPU can be used to enforce privilege rules, separate processes and manage memory attributes. The Apollo510B SoC supports up to 16 memory regions and the S-MCU supports up to 16 *secure* memory regions.

2.4 Power Management Overview

Power management is partitioned into several components across the Apollo510B SoC. For the CPU complex, a dedicated finite-state machine controls the transitions of the CPU between power modes. When moving from Active Mode to Deep Sleep Mode, the CPU-PMU manages the state-retention capability of the registers within the Cortex-M55 core and also handshakes with the central power management controller to appropriately handle the voltage rails to the CPU complex. Once in Deep Sleep Mode, the CPU-PMU, in conjunction with the Wake-Up Interrupt Controller, waits for a wakeup event. When the event is observed, the CPU-PMU begins the power restoration process by handshaking with the central power management controller to adjust the voltage rails to the CPU complex and initiate the restoration of the CPU register state. The Cortex-M55 is then returned to active mode once all state is ready.

2.4.1 Cortex-M55 Power Modes

The Arm Cortex-M55 supports power modes as listed in Table 2.

Table 2: Arm Cortex-M55 Power Modes

Ambiq M55 Power Mode	Arm M55 Power Mode
HP Active	Active
Active	
Sleep	ON, clock off
Deep Sleep	Retention
Off	Off

In addition to the above Arm-defined modes, the Apollo510B SoC supports system level power modes which are defined in the Power Management chapter. See section “Program Control of Power Management” on page 47 which describes programmatic control of power mode transitioning via the MCUPERFREQ register and other module/processor-specific registers in the PWRCTRL register set.

2.4.1.1 High Performance Mode

The Apollo510B SoC supports the Ambiq TurboSPOT™ which enables a higher frequency operating mode (HP Mode). In this mode, the Cortex-M55 and all closely coupled memory run at an elevated frequency. All of the non-debug Arm clocks (FCLK, HCLK) also operate at the elevated frequency level. All peripherals are maintained at the nominal frequency level during burst. This mode is entered and exited under software direction but transitions are completely handled in hardware.

This is not a standard Arm-defined power mode. From the Arm core, this mode is treated similarly to “Active Mode”.

2.4.1.2 Active Mode

In the Active Mode, the Cortex-M55 core is powered up, clocks are active, and instructions are being executed. In this mode, the Cortex-M55 expects all (enabled) devices attached to the interfaces to be powered and clocked for normal access. All of the non-debug Arm clocks (FCLK, HCLK) are active in this state.

To transition from the Active Mode to any of the lower-power modes, a specific sequence of instructions is executed on the Cortex-M55 core. First, specific bits in the Armv8-M System Control Register must be set to determine the mode to enter. See the Armv8-M Architecture Reference Manual for more details.

After the SCR is setup, code can enter the low-power states using one of the three following methods:

- Execute a Wait-For-Interrupt (WFI) instruction.
- Execute a Wait-For-Event (WFE) instruction.
- Set the SLEEPONEXIT bit of the SCR such that the exit from an ISR will automatically return to a sleep state.

The Cortex-M55 will enter a low-power mode after one of these are performed (assuming all conditions are met) and remain there until some event causes the core to return to Active Mode. The possible reasons to return to Active Mode are:

- A reset
- An enabled Interrupt is received by the NVIC
- An event is received by the NVIC
- A debug event is received from the DAP

2.4.1.3 Sleep Mode

In Sleep Mode, the Cortex-M55 is powered up, but the clocks (HCLK, FCLK) are gated. The power supply is still applied to the Cortex-M55 logic such that it can immediately become active on a wakeup event and begin executing instructions.

2.4.1.4 Deep Sleep Mode

In Deep Sleep Mode, the Cortex-M55 enters SRPG mode where the main power is removed, but the flops retain their state. The clocks are not active, and the MCU clock sources for HCLK and FCLK can be deactivated. To facilitate the removal of the source supply and entry into SRPG mode, the Cortex-M55 will handshake with the Wake-up Interrupt Controller and Power Management Unit and set up the possible wakeup conditions.

2.5 Debug

The Apollo510B SoC supports several debug features to facilitate software development, profiling and analysis. Standard Serial Wire Debug (SWD) interface is supported along with 1-bit and 4-bit trace data port and optional Serial Wire Output (SWO).

The CPU debug components in the Apollo510B SoC support the following features:

- Secure and Non-Secure Debugging
- Embedded Trace Macrocell (ETM)
- Dedicated 32 kB Embedded Trace Buffer (ETB)
- Instrumentation Trace Macrocell (ITM) supporting instrumentation tracing and trace port via Serial Wire Output (SWO)
- Trace Port Interface Unit (TPIU)
- 8x Data Watchpoint and Trace (DWT)
- 8x Breakpoint Unit (BPU)
- Hardware fault reporting

- Serial Wire Debug (SWD)
- Performance Monitoring Unit (PMU)

ERRATUM NOTICE

On the Cortex-M55, self-hosted debug components should be powered on automatically when the Cortex-M55 writes to any of the debug subsystem registers (ITM, WDT, TPIU, etc.). In the Apollo510, writing to the TPIU registers does not automatically power-on the debug subsystem. Therefore software must manually enable the debug power domain, PDDBG, by setting the PWRCTRL_DEVPWREN_PWRENDBG bit, and then can access the debug registers safely. This is required before accessing any self-hosted debug functions, including enabling the SWO for logging or messages. If software writes to a TPIU register when the PDDBG is off, the system hangs. Note that manually enabling PDDBG is not required when an external debugger is attached.

See “ERR003: DEBUG: In self-hosted debug, TPIU register writes when PDDBG is not power up can cause system hang” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

The enabled SWO pin goes low during deep sleep mode which violates the SWO specifications. This signal is expected to stay high during deep sleep. The SWO output is in the PDDBG power domain which does remain powered when the Cortex-M55 core goes to sleep. However, these signals are routed through the MCUH power domain which is powered down in deep sleep resulting in the SWO signal being isolated low.

See “ERR032: DEBUG: SWO pin goes low during deep sleep” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

After SWO printing has concluded, the Apollo510 SDK HAL functions disable the Instrumentation Trace Macrocell (ITM) and Trace Port Interface Unit (TPIU), then power down the DEBUG domain. Before doing so, the HAL functions attempt to detect that all printing has completed via ITM status signals. Based on these signals, in some cases it's possible that the disabling and DEBUG domain power down occur before the ITM/TPIU pipeline has actually become quiescent. When this happens, a debugger (e.g. J-Link Commander) will not be able to connect again to the device as the DEBUG domain will not power up until a power cycle occurs.

See “ERR040: DEBUG: Cannot connect to a debugger after DEBUG domain is powered down” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

The DEBUG power domain can be put into a state where it will not power down after reads from the processor ROM table, which leads to increased power consumption and manifests as the PWRCTRL_DEVPWRSTATUS_PWRSTDBG register field getting stuck at 1. Due to a handshake issue in the power control logic, this can happen when accessing the processor ROM table with back-to-back reads. This issue occurs with the following conditions and effect: 1. 2. 3. The issue occurs whether or not the debug domain already had been powered up before the back-to-back reads occur. Only ROM table reads are at risk of causing this issue. Once in this state, the PWRSTDBG cannot be cleared by software and a chip reset is required.

See “ERR041: DEBUG: DEBUG power domain may not power down under certain conditions” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

2.5.1 Embedded Trace Macrocell (ETM)

The Apollo510B SoC supports hardware instruction tracing via an Embedded Trace Macrocell (ETM). The ETM stream is accessible via APB or TPIU. An Embedded Trace Buffer provides 32 kB of trace buffering. Note that while ETM 4.5 is capable of supporting data tracing as well as instruction tracing, data tracing was not implemented in the ETM-M55. However, data-tracing facilities are available through the DWT.

2.5.2 Instrumentation Trace Macrocell (ITM)

For system trace the processor integrates an Instrumentation Trace Macrocell (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system events these generate, a Serial Wire Viewer (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

2.5.3 Trace Port Interface Unit (TPIU)

The Apollo510B SoC includes a Cortex-M55 Trace Port Interface Units (TPIU) which can take input from the CPU ITM or ETM. It is an Arm IP component that supports a 1-bit or 4-bit trace data port and Serial Wire Output (SWO). It can act as a bridge between the on-chip trace data from the ITM and the single pin supporting the Serial Wire Viewer Protocol, as well as support the ETM trace output. The TPIU includes a Trace Output Serializer that can format and send the SWV protocol in either a Manchester encoded form or as a standard UART stream.

NOTE

For ETM instruction tracing, Arm recommends the 4-bit trace data port with the TPIU input frequency matching the maximum CPU frequency (250 MHz) for TPIU TRACECLKIN. Note that only GPIO142 to GPIO147 can be used as the TRACE port for clock frequencies above 96 MHz.

2.5.4 Serial Wire Debug (SWD)

An external debugger can be connected to the MCU using the Arm Serial Wire Debug (SWD) interface. The SWD interface is a 2-wire interface that is supported by a variety of off-the-shelf commercial debuggers, enabling customers to utilize their development environment of choice.

2.5.5 Performance Monitoring Unit (PMU)

The Performance Monitoring Unit (PMU) is a powerful tool used for code profiling and optimization and provides the following capabilities:

- Collect real-time data to fine-tune applications, maximizing efficiency and performance on the Cortex-M55 core.
- Track memory usage and identify system inefficiencies, enhancing responsiveness and minimizing slow memory accesses.
- Optimize AI and digital signal processing by monitoring vector unit utilization and enhancing throughput on complex tasks.
- Gather detailed data on execution patterns, helping identify and resolve bottlenecks faster.

2.5.6 Data Watchpoint and Trace (DWT)

The Data Watchpoint and Trace (DWT) of the Cortex-M55 (ArmV8-M) includes watchpoints, data value watchpoints, and trace control signaling which can be used to control the ETM and CTI, performance profiling and more. It does not perform tracing of all data addresses issued by the processor.

See the Arm Cortex-M55 Technical Reference Manual, section 17.1 and ArmV8-M Architecture Reference Manual, section D1.2.63 for more details.

2.5.7 Breakpoint Unit (BPU)

The BPU is configured with four instruction address comparators. Each comparator supports breakpoint functionality on all instructions that are fetched across the entire address range in which code is located. If invasive debug is not enabled for a security mode, then debug events associated with breakpoints in that mode are blocked.

2.5.8 Faulting Address Trapping Hardware

The Apollo510B SoC offers an optional facility for trapping the address associated with bus faults occurring on any of the three AMBA AHB buses on the chip. This facility must be specifically enabled so that energy is not wasted when one is not actively debugging. The Cortex-M55 core provides bus fault information using the Configurable Fault Status Register that can be configured for usage fault, bus fault and memory management fault reporting. The Auxiliary Fault Status Register provides additional information on the types and causes of faults. The Bus Fault Address Register and the MemManage Fault Address Register capture the memory address that caused one of these faults.

2.5.9 PPB/EPPB Interfaces

The ITM, DWT, BPU, CTI and ETM programming interfaces are provided through the Cortex-M55 private peripheral bus (PPB). The system TPIU and the ETB programming interfaces are provided on the external private peripheral bus (EPPB).

2.6 Additional Information

Please refer to the MCUCTRL registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

3. Memory Subsystem

3.1 Features

The memory for the CPU subsystem consists of the following features.

- 2-way set associative instruction cache
- 4-way set associative data cache
- Tightly-coupled instruction memory
- Tightly-coupled memory
- NVM interface
- System SRAM interface

3.2 Functional Overview

The instruction cache for the CPU subsystem caches all instruction accesses to the code region of the memory map. On the Apollo510B SoC, this memory includes internal and external non-volatile memory as well as on-chip and off-chip RAM.

The instruction cache has the following features:

- 64 kB capacity
- 2-way set-associative
- 32-byte line size
- Instruction prefetching

The data cache has the following features:

- 64 kB capacity
- 4-way set-associative
- 32-byte line size
- Write-back and write-through cacheable
- Read-allocate and no read-allocate
- Write-allocate and no write-allocate
- Transient and non-transient. Clean cache lines that are associated with transient memory are prioritized for eviction over lines that are associated with non-transient memory
- Data prefetching with programmable look ahead distance

The store buffer has five 64-bit entries and has merging capabilities. If a previous write access has updated an entry, other write accesses on the same double-word can merge into this entry.

The Instruction Tightly Coupled Memory (ITCM) is up to 256 kB in size and provides zero wait-state instruction memory access to the CPU. The ITCM is a low-power/low-latency memory with multiple size configurations.

The TCM is up to 512 kB in size and provides zero wait-state data memory access to the CPU.The DTCM is a low-power/low-latency memory with configurable power settings for multiple size configurations.

ERRATUM NOTICE

There are three known restrictions on DMAing to TCM.

1. A DMA transfer cannot cross a DTCM 4 kB boundary.
2. Access to TCM when it is powered down returns an incorrect error condition (Success).
3. Access to TCM while the CPU is in deep sleep with memory retained returns an error. A DMA operation cannot be performed to or from DTCM when the CPU is in deep sleep or the DTCM location is powered down.

See “ERR014: Memory: Restrictions on use of DMA to TCM” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

The Shared SRAM (SSRAM) is accessible via the SRAM region. The SSRAM is 3072 kB of shared system memory. Access to this memory region incurs 8 or more cycle wait-states, depending on the CPU operating mode.

The CPU sub-system includes a boot ROM which is the initial boot memory for the system. The boot ROM initiates the secure boot flow, if enabled, as well as other primitive/critical helper functions to facilitate accesses such as NVM programming.

ERRATUM NOTICE

A write to INFO0, INFO1 or MRAM main_mem coincident with an AXI burst read results in read data corruption.

See “ERR043: MRAM: Concurrent AXI burst read to MRAM and an MRAM write cause read data to be corrupted” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

A bug exists where, if NVM1 is powered down while NVM0 is powered on, the MRAM Controller state machine hangs upon a POR or POI level reset.

See “ERR044: MRAM: Powered down NVM1 causes state machine to hang” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

3.3 Interrupts

Within the SoC, multiple peripherals can generate interrupts. In some cases, a single peripheral may be able to generate multiple different interrupts. Each interrupt signal generated by a peripheral is connected to one of the processing cores. For interrupts that route back to the Cortex-M55 core, these can be routed to two places. First, the interrupts are connected to the Nested Vectored Interrupt Controller, NVIC, in the core. This connection provides the standard changes to program flow associated with interrupt processing. Additionally, they are connected to the WIC outside of the core, allowing the interrupt sources to wake the Cortex-M55 core when it is in a deep sleep (SRPG) mode.

For details on the interrupt model of the Cortex-M55, please see the “Cortex-M55 Devices Generic User Guide.” The VTOR register in the System Control Block (SCB) determines the starting address of the vector table.

In the Apollo510B SoC implementation with the Security Extension, the VTOR is banked so there is a VTOR_S and a VTOR_NS. The initial values of VTOR_S and VTOR_NS are system design specific. The vector table used depends on the target state of the exception. For exceptions targeting the Secure state, VTOR_S is used. For exceptions targeting the Non-secure state, VTOR_NS is used.

Note that for non-secure interrupts, the value in the secure vector table will be an invalid address to generate an exception as this is an error condition (which could be the non-secure address as jumping to it would be a security error). Conversely, for secure-interrupts, the value in the non-secure table will be an invalid address for non-secure code (could be the secure address as this would generate a security error). Banked interrupts means there are secure and non-secure versions of this interrupt. Therefore the vector values in each of the secure and non-secure versions are valid, and should be different (one secure and one non-secure).

3.3.1 Vector Table for Apollo510B SoC

In the Apollo510B SoC implementation with the Security Extension, the VTOR is banked so there is a VTOR_S and a VTOR_NS. The initial values of VTOR_S and VTOR_NS are system design specific. The vector table used depends on the target state of the exception. For exceptions targeting the secure state, VTOR_S is used. For exceptions targeting the non-secure state, VTOR_NS is used.

Note that for non-secure interrupts, the value in the secure vector table will be an invalid address to generate an exception as this is an error condition. Conversely, for secure-interrupts, the value in the non-secure table will be an invalid address for non-secure code. Banked interrupts mean there are secure and non-secure versions of this interrupt. Therefore the vector values in each of the secure and non-secure versions are valid, and should be different (one secure and one non-secure).

Table 3 represents the Cortex-M55 Vector Table for the Apollo510B SoC.

Table 3: Apollo510B SoC Cortex-M55 Vector Table

Exception Number	IRQ	Offset	Vector	Description
150	134	0x258	IRQ134	OTP
149	133	0x254	IRQ133	FP Exception[1]
148	132	0x250	IRQ132	Reserved
141 - 147	125 - 131	0x234 - 0x24C	IRQ 125 - 131	GPIO8 - 14: MCUN1INTn (n = 0 to 6)
125 - 140	109 - 124	0x1F4 - 0x230	IRQ109 - 124	Reserved
124	108	0x1F0	IRQ108	Reserved
116 - 123	100 - 107	0x1D0 - 0x1EC	IRQ100 - 107	Reserved
115	99	0x1CC	IRQ99	IOSFD1 SPI Subordinate Register Access
114	98	0x1C8	IRQ98	IOSFD1 SPI Subordinate
113	97	0x1C4	IRQ97	IOSFD0 SPI Subordinate Register Access
112	96	0x1C0	IRQ96	IOSFD0 SPI Subordinate
108 - 111	92 - 95	0x1B0 - 0x1BC	IRQ92 - IRQ95	SW INT[3:0]
107	91	0x1AC	IRQ91	Reserved

Table 3: Apollo510B SoC Cortex-M55 Vector Table

Exception Number	IRQ	Offset	Vector	Description
106	90	0x1A8	IRQ90	Reserved
105	89	0x1A4	IRQ89	Reserved
104	88	0x1A0	IRQ88	Reserved
103	87	0x19C	IRQ87	Reserved
102	86	0x198	IRQ86	Reserved
101	85	0x194	IRQ85	Reserved
100	84	0x190	IRQ84	SDIO1
99	83	0x18C	IRQ83	Reserved
98	82	0x188	IRQ82	Timer 15
97	81	0x184	IRQ81	Timer 14
96	80	0x180	IRQ80	Timer 13
95	79	0x17C	IRQ79	Timer 12
94	78	0x178	IRQ78	Timer 11
93	77	0x174	IRQ77	Timer 10
92	76	0x170	IRQ76	Timer 9
91	75	0x16C	IRQ75	Timer 8
90	74	0x168	IRQ74	Timer 7
89	73	0x164	IRQ73	Timer 6
88	72	0x160	IRQ72	Timer 5
87	71	0x15C	IRQ71	Timer 4
86	70	0x158	IRQ70	Timer 3
85	69	0x154	IRQ69	Timer 2
84	68	0x150	IRQ68	Timer 1
83	67	0x14C	IRQ67	Timer 0
82	66	0x148	IRQ66	Reserved
81	65	0x144	IRQ65	Reserved
80	64	0x140	IRQ64	Reserved
79	63	0x13C	IRQ63	Reserved
72 - 78	56 - 62	0x120 - 0x138	IRQ56 - IRQ62	GPIO Group 0 - 6: MCUN0INTn (n = 0 to 6)
71	55	0x11C	IRQ55	Reserved
70	54	0x118	IRQ54	Reserved
69	53	0x114	IRQ53	Reserved
68	52	0x110	IRQ52	Reserved
67	51	0x10C	IRQ51	Reserved
66	50	0x108	IRQ50	Reserved
65	49	0x104	IRQ49	Reserved

Table 3: Apollo510B SoC Cortex-M55 Vector Table

Exception Number	IRQ	Offset	Vector	Description
64	48	0x100	IRQ48	PDM0
63	47	0xFC	IRQ47	Reserved
62	46	0xF8	IRQ46	Reserved
61	45	0xF4	IRQ45	I2S1
60	44	0xF0	IRQ44	I2S0
59	43	0xEC	IRQ43	Reserved
58	42	0xE8	IRQ42	AUDADC
57	41	0xE4	IRQ41	Reserved
56	40	0xE0	IRQ40	Stimer Capture/Overflow
48 - 55	32 - 39	0xC0 - 0xDC	IRQ32 - IRQ39	Stimer Compare[0:7]
47	31	0xBC	IRQ31	Reserved
46	30	0xB8	IRQ30	DSI
45	29	0xB4	IRQ29	Display
44	28	0xB0	IRQ28	Graphics
43	27	0xAC	IRQ27	USB
42	26	0xA8	IRQ26	SDIO0
41	25	0xA4	IRQ25	CRYPTO Non-Secure
40	24	0xA0	IRQ24	CRYPTO Secure
39	23	0x9C	IRQ23	Clock Control
38	22	0x98	IRQ22	Reserved
37	21	0x94	IRQ21	MSPI1
36	20	0x90	IRQ20	MSPI0
35	19	0x8C	IRQ19	GPADC
34	18	0x88	IRQ18	UART3
33	17	0x84	IRQ17	UART2
32	16	0x80	IRQ16	UART1
31	15	0x7C	IRQ15	UART0
30	14	0x78	IRQ14	Counter/Timers (combined - also see IRQ 65 - 81)
29	13	0x74	IRQ13	I^2C/SPI Manager7
28	12	0x70	IRQ12	Reserved
27	11	0x6C	IRQ11	I^2C/SPI Manager5
26	10	0x68	IRQ10	I^2C/SPI Manager4
25	9	0x64	IRQ9	I^2C/SPI Manager3
24	8	0x60	IRQ8	I^2C/SPI Manager2
23	7	0x5C	IRQ7	I^2C/SPI Manager1
22	6	0x58	IRQ6	I^2C/SPI Manager0

Table 3: Apollo510B SoC Cortex-M55 Vector Table

Exception Number	IRQ	Offset	Vector	Description
21	5	0x54	IRQ5	Reserved
20	4	0x50	IRQ4	Reserved
19	3	0x4C	IRQ3	Voltage Comparator
18	2	0x48	IRQ2	RTC
17	1	0x44	IRQ1	Watchdog Timer
16	0	0x40	IRQ0	Brownout Detection
15	-1	0x3C	Systick(_S)	
14	-2	0x38	PendSV(_S)	
13	-	0x34	Reserved	
12	-4	0x30	DebugMonitor	
11	-5	0x2C	SVCall(_S)	
10	-	0x28	Reserved	
9	-	0x24		
8	-	0x20		
7	-9	0x1C	SecureFault_S	Secure Fault
6	-10	0x18	UsageFault_S	Usage Fault
5	-11	0x14	BusFault_S	Bus Fault
4	-12	0x10	MemoryManage_S	Memory Management Fault
3	-13	0xC	HardFault_S	Hard Fault
2	-14	0x8	NMI_S	
1	-	0x4	Reset	
		0x0	Initial SP	

1. Floating point exception interrupt is raised when one of six possible FP errors is detected. The FPSCR register must be interrogated to determine the source(s) of the interrupt. Note that the interrupt is not banked (nor is FPSCR), so the interrupt must be reassigned secure if a FP secure context is created. (The FPDSCR is banked).

3.3.2 GPIO Extension

The Apollo5 family supports up to 190 GPIOs depending on device and package, so the mapping is extended such that 0-6 are groups of 32 GPIO interrupts, and 8-14 form the second group (GPIO interrupts 7 and 15 are reserved). See “GPIO Interrupts” on page 90 for more information about GPIO interrupt grouping and operation.

3.4 Memory Maps

Table 4 shows the memory map for the Arm Cortex-M55 CPU used by the Apollo510B SoC.

Table 4: Cortex-M55 CPU Memory Map

Type	Address Range	Name	Executable	Description
Code	0x00000000 - 0x0003FFFF	ITCM	Y	Instruction TCM (256 kB)
	0x00040000 - 0x003FFFFF	Reserved	X	Reserved
	0x00400000 - 0x0040FFFF	NVM-SBL	Y	NVM reserved for Secure Boot Loader (64 kB)
	0x00410000 - 0x005FFFFF	NVM0-APPL	Y	NVM0 for application (1.94 MB)
	0x00600000 - 0x007FFFFF	NVM1-APPL	Y	NVM1 for application (2 MB)
	0x00800000 - 0x01FFFFFF	Reserved	X	Reserved
	0x02000000 - 0x0201FFFF	Boot Loader ROM	Y	Boot Loader ROM (128 kB)
	0x02020000 - 0x0FFFFFFF	Reserved	X	Reserved
	0x10000000 - 0x1003FFFF	ITCM	Y	Instruction TCM (256 kB) [Aliased to 0x00000000 - accessible only from Secure SW when TrustZone is enabled]
	0x10040000 - 0x1FFFFFFF	Reserved	X	Reserved
SRAM	0x20000000 - 0x2007FFFF	DTCM	Y	Data TCM (512 kB)
	0x20080000 - 0x2037FFFF	System SRAM	Y	System SRAM (3 MB)
	0x20380000 - 0x2FFFFFFF	Reserved	X	Reserved
	0x30000000 - 0x3007FFFF	DTCM	Y	Data TCM (512 kB) [Aliased to 0x20000000 - accessible only from Secure SW when TrustZone is enabled]
	0x30080000 - 0x3FFFFFFF	Reserved	X	Reserved
Peripheral	0x40000000 - 0x4FFFFFFF	Peripheral	N	See Peripheral Memory Map
	0x50000000 - 0x5FFFFFFF	Reserved	X	Reserved
External RAM	0x60000000 - 0x6FFFFFFF	MSPI0	Y	External Memory (256 MB)
	0x70000000 - 0x7FFFFFFF	Reserved	X	Reserved
	0x80000000 - 0x83FFFFFF	MSPI1	Y	External Memory (64 MB)
	0x84000000 - 0x87FFFFFF	Reserved	Y	Reserved
	0x88000000 - 0x8FFFFFFF	Reserved	Y	Reserved
	0x90000000 - 0x9FFFFFFF	Reserved	X	Reserved
External Device	0xA0000000 - 0xDFFFFFFF	Reserved	X	Reserved
Private Peripheral Device	0xE0000000 - 0xE00FDFFF	PPB	N	NVIC, System timers, System Control Block, MPU, TPIU, EWIC
	0xE00FE000 - 0xE00FEFFF	Debug ROM	X	Debug ROM
	0xE00F1000 - 0xE00FFFFF	PPB	X	Reserved
Vendor_ SYS	0xE0100000 - 0xFFFFFFFF	Reserved	X	Reserved

Peripheral devices within the memory map are allocated on 4 kB boundaries (mostly), allowing each device up to 1024 32-bit control and status registers. Peripherals will return undefined read data when an attempt to access a register which does not exist occurs. Peripherals will always accept any write data sent to their registers without attempting to return an error response. Specifically, a write to a read-only register would just become a don't-care write.

Table 5 shows the memory map for the peripheral devices. The CPU has access to all peripheral devices. This table illustrates how SAU partitions are used to make certain peripheral regions secure when running with a TrustZone-secure partition enabled. OTP registers are separated from MRAM control to allow OTP registers to be secure via the SAU while the MRAM registers remain non-secure.

Table 5: Apollo510B SoC Peripheral Memory Map

Address Range	Device Name
0x40000000 - 0x400003FF	Reset/BoD Control (1 kB)
0x40000400 - 0x40003FFF	Reserved
0x40004000 - 0x400041FF	Clock Generator (0.5 kB)
0x40004200 - 0x400047FF	Reserved
0x40004800 - 0x40004BFF	RTC (1 kB)
0x40004C00 - 0x40007FFF	Reserved
0x40008000 - 0x400083FF	Timers (1 kB)
0x40008400 - 0x400087FF	Reserved
0x40008800 - 0x400089FF	STImer (0.5 kB)
0x40008A00 - 0x4000BFFF	Reserved
0x4000C000 - 0x4000C3FF	Voltage Comparator (1 kB)
0x4000C400 - 0x4000FFFF	Reserved
0x40010000 - 0x400107FF	GPIO Control (2 kB)
0x40010800 - 0x40013FFF	Reserved
0x40014000 - 0x40014FFF	MRAM/OTP Control (4 kB)
0x40015000 - 0x4001FFFF	Reserved
0x40020000 - 0x400207FF	Miscellaneous Control (MCUCTRL) (2 kB)
0x40020800 - 0x40020FFF	Reserved
0x40021000 - 0x400213FF	Power Control(1 kB)
0x40021400 - 0x40023FFF	Reserved
0x40024000 - 0x400243FF	Watchdog Timer (1 kB)
0x40024400 - 0x40024FFF	Reserved
0x40025000 - 0x40025FFF	SSC (4 kB)
0x40025400 - 0x4002FFFF	Reserved
0x40030000 - 0x400303FF	Security (1 kB)
0x40030400 - 0x40034FFF	Reserved

Table 5: Apollo510B SoC Peripheral Memory Map

Address Range	Device Name
0x40035000 - 0x400353FF	IOSFD0 SPI Subordinate (1 kB)
0x40035400 - 0x40035FFF	Reserved
0x40036000 - 0x400363FF	IOSFD1 SPI Subordinate (1 kB)
0x40036400 - 0x40037FFF	Reserved
0x40038000 - 0x400383FF	GPADC (1 kB)
0x40038400 - 0x40038FFF	Reserved
0x40039000 - 0x400393FF	UART0 (1 kB)
0x40039400 - 0x40039FFF	Reserved
0x4003A000 - 0x4003A3FF	UART1 (1 kB)
0x4003A400 - 0x4003AFFF	Reserved
0x4003B000 - 0x4003B3FF	UART2 (1 kB)
0x4003B400 - 0x4003BFFF	Reserved
0x4003C000 - 0x4003C3FF	UART3 (1 kB)
0x4003C400 - 0x4004FFFF	Reserved
0x40050000 - 0x40050FFF	I^2C/SPI Manager0 (4 kB)
0x40051000 - 0x40051FFF	I^2C/SPI Manager1 (4 kB)
0x40052000 - 0x40052FFF	I^2C/SPI Manager2 (4 kB)
0x40053000 - 0x40053FFF	I^2C/SPI Manager3 (4 kB)
0x40054000 - 0x40054FFF	I^2C/SPI Manager4 (4 kB)
0x40055000 - 0x40055FFF	I^2C/SPI Manager5 (4 kB)
0x40056000 - 0x40056FFF	Reserved
0x40057000 - 0x40057FFF	I^2C/SPI Manager7 (4 kB)
0x40058000 - 0x4005FFFF	Reserved
0x40060000 - 0x400603FF	MSPI Manager0 (1 kB)
0x40060400 - 0x40060FFF	Reserved
0x40061000 - 0x400613FF	MSPI Manager1 (1 kB)
0x40061400 - 0x4006FFFF	Reserved
0x40070000 - 0x400703FF	SDIO0 (1 kB)
0x40070400 - 0x40070FFF	Reserved
0x40071000 - 0x400713FF	SDIO1 (1 kB)
0x40071400 - 0x4008FFFF	Reserved
0x40090000 - 0x4009FFFF	Graphics Subsystem (64 kB)
0x400A0000 - 0x400A7FFF	Display Controller (32 kB)
0x400A8000 - 0x400AFFFF	Display PHY (32 kB)
0x400B0000 - 0x400B3FFF	USB (16 kB)
0x400B4000 - 0x400B7FFF	USB PHY (16 kB)

Table 5: Apollo510B SoC Peripheral Memory Map

Address Range	Device Name
0x400B8000 - 0x400BFFFF	Reserved
0x400C0000 - 0x400C7FFF	Crypto (32 kB)
0x400C8000 - 0x40200FFF	Reserved
0x40201000 - 0x402013FF	PDM0 (1 kB)
0x40201400 - 0x40207FFF	Reserved
0x40208000 - 0x402083FF	I2S0 (1 kB)
0x40208400 - 0x40208FFF	Reserved
0x40209000 - 0x402093FF	I2S1 (4 kB)
0x40209400 - 0x4020FFFF	Reserved
0x40210000 - 0x402103FF	AUDADC (LPADC) (1 kB)
0x40210400 - 0x41FFFFFF	Reserved
0x42000000 - 0x420007FF	NVM_INFO0 (2 kB)
0x42000800 - 0x42001FFF	Reserved
0x42002000 - 0x420037FF	NVM_INFO1 (6 kB)
0x42003800 - 0x42003FFF	Reserved
0x42004000 - 0x420040FF	OTP2_INFO0 (256 Bytes)
0x42004100 - 0x42005FFF	Reserved
0x42006000 - 0x42006AFF	OTP2_INFO1 (1.375 kB)
0x42006B00 - 0x4FFFFFFF	Reserved

3.5 Static Random Access Memory (SRAM)

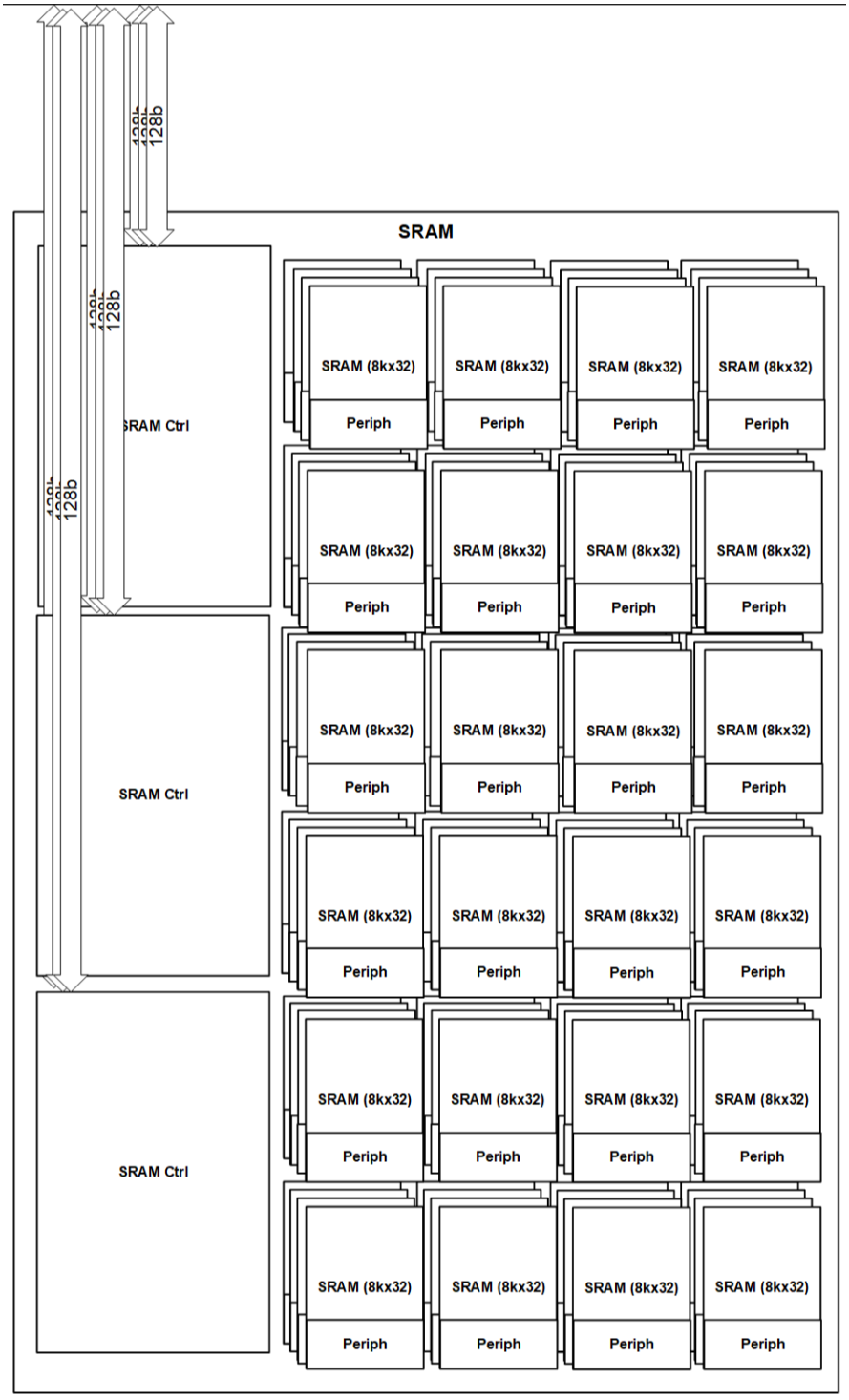

Figure 4. SRAM Block Diagram

3.5.1 Features

The Static Random Access Memory (SRAM) Controller supports features shown in Figure 4 and listed below.

- Fully synchronous design at 96 MHz (nominal)
- Three (3) 128-bit wide main AXI interfaces
- Internal arrays have 128 kB granularity. Each array can be concurrently accessed unless a physical conflict exists for the same 128 kB region.
- Supports concurrent operation to 3 independent 128 kB banks
- Partitioned into 2 power domains

Please refer to the MCUCTRL registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

3.5.2 Functional Overview

The Apollo510B SoC SRAM module provides up to 3 MB of shared internal SRAM for the system. It has three primary 128-bit AXI system interfaces and accommodates up to three simultaneous SRAM operations per cycle as long as the RAM bank doesn't overlap. Below are the port mappings:

- Port 0: DMA
- Port 1: GPU, Display Controller
- Port 2: CPU

3.6 OTP

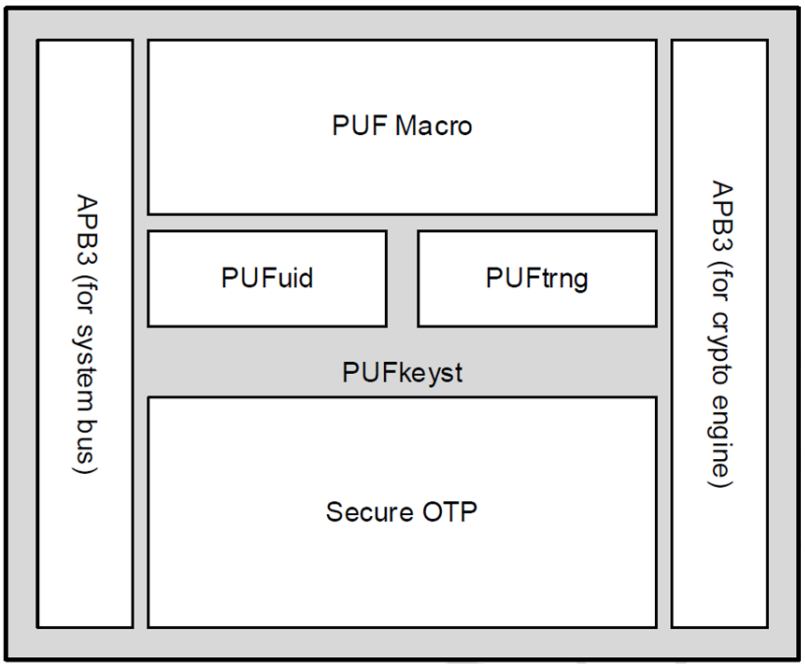

Figure 5. OTP Block Diagram

3.6.1 Features

The One-Time Programmable (OTP) and Physically Unclonable Function (PUF) include features[1] shown in Figure 5 and listed below.

- OTP anti-fuses
- PUFuid on NeoPUF: 2 kbits on-chip Identification
- PUFtrng: PUF-based True Random Number Generator
  - Conditioning & Entropy Health Test

ERRATUM NOTICE
An access to the OTP info space or OTP registers when the OTP is powered down will result in an APB bus hang. The OTP power domain is powered up by setting the PWRCTRL_DEVPWREN_PWRENOTP field to Enable. This field is enabled by default. See “ERR022: PWRCTRL: APB bus hang when accessing unpowered OTP registers or INFO space” in the *Apollo510 SoC*.

1. Some of the features are reserved for Ambiq use.

ERRATUM NOTICE
The SoC design requires that the CPU be powered on when either OTP or ROM is powered on. See “ERR023: PWRCTRL: CPU cannot go into deep sleep when either OTP or ROM is powered on” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

3.6.2 Functional Overview

The OTP block on the Apollo510B SoC includes multiple regions of OTP anti-fuse bits, anti-tampering support, read/write locking and dedicated interfaces for system and crypto access. The OTP anti-fuses are divided into the following three regions:

- INFO0: 256 bytes (2048 bits)
- INFO1: 1.375 kB (11 kbits)
- INFOC: 1024 bytes (8 kbits)

3.6.2.1 PUF Features/Functionality

PUF features[1] on the Apollo510B SoC are described below.

- **NeoPUF®** - A weak PUF defined as a PUF with limited CRPs (challenge-response-pairs).
  - Able to be used for generating true random bits which can act as a silicon fingerprint.
  - Has the near ideal PUF characteristics of 50% HW (Hamming-Weight), 50% Inter-HD (Hamming-Distance), 0% Intra-ID HD and 0ppm BER (Bit-Error-Rate).
  - Passes the NIST SP800-22 and NIST SP80090B IID statistical analysis test suites.
- **PUFuid®**
  - Offers 1 kilobit unique keys, which are derived from NeoPUF and programmed into PUF array in OTP by Ambiq. These keys can be used as a source for a unique ID, root key or entropy source, which is different for each chip.
- **PUFtrng®**
  - True random number generator with a PUF-based refinement engine.
  - Leverages 1 kilobits of PUF data for initial seeding.

3.6.2.1.1 PUF System Side Function Descriptions

System side function descriptions are as follows. PUF register addresses listed are offsets from a base address of 0x40014800.

- **Get Random Number Output (0x12A0)**
  - Provides high-quality random number bits (32 bits each time) for security usage.
  - Open to all security levels unless memory range is mapped Secure.
- **Read UID (0x1300 - 0x137C)**
  - Reads from a 1 kilobit PUF Array which contains all the random data that is used for UIDs and the entropy source for the TRNG.
  - 32 UID locations ranging from 0x1300 to 0x137C.
  - Read the UID from PUF cell.
  - These registers are labeled puf_000 - puf_031.

1. Certain functions have been protected and are only accessible to secure software if a secure execution environment (SEE) is instantiated.

- Each PUF location provides 32 bits static entropy which can act as a silicon fingerprint for the various security applications of identification, authentication, and local data protection.
- Only accessible to the Secure domain, if SEE is instantiated.

3.7 Additional Information

Please refer to the MCUCTRL and OTP registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

4. System Power Management

System Power Management on the Apollo510B SoC is handled through a combination of hardware and software. The hardware handles the interface and control sequencing between the regulators and the individual power domains within the SoC. The software initiates transitions through power states by processor instructions and system level power control commands.

4.1 Functional Overview

The Power Management system is composed of a central power management controller and various power management units (PMUs) for each primary subsystem. The primary PMUs are as follows:

- CPU PMU: responsible for power sequencing for the CPU subsystem
- GPU PMU: responsible for power sequencing for the graphics subsystem
- IO/Peripheral PMU: responsible for power sequencing at each I/O subsystem
- Memory PMU: responsible for power sequencing each memory subsystem/power bank

4.1.1 CPU Power Management Unit

When moving from Active Mode to Deep Sleep Mode, the CPU PMU manages the state-retention capability of the registers within the Cortex-M55 core and controls the interface to the voltage regulators as needed to support the various operating modes of the CPU. Once in the Deep Sleep Mode, the CPU PMU, in conjunction with the Wake-Up Interrupt Controller, waits for a wakeup event. When the event is observed, the CPU PMU begins the power restoration process by re-enabling the on-chip voltage regulators and restoring the CPU register state. The Cortex-M55 is then returned to active mode.

The CPU-PMU enables support for the following Arm Cortex-M55 defined power modes:

- OFF
- Deep Sleep
- Sleep
- Active
  - Low Power / High Efficiency: 96 MHz (LP)
  - High Performance: 250 MHz

4.1.2 GPU Power Management Unit

When transitioning power states (such as Active LP to Active HP), the system software manages the voltage power mux and clock selection as well as the appropriate isolation and reset controls as needed.

The system software enables support for the following defined power modes:

- OFF
- Sleep/Idle (device is enabled but no active transactions)
- Active
  - Low Power / High Efficiency: 96 MHz
  - High Performance: 250 MHz

4.1.3 IO/Peripheral Power Management Unit

The IO/Peripheral PMU's manage power state for I/O subsystems. Each I/O subsystem will support the following power modes. Note that each I/O subsystem may have differences in power state implementation (i.e., what “Active” means). This is implementation specific to each I/O controller. Also, not all power modes may be supported by each IO/Peripheral PMU (typical configuration may support only OFF and Active power modes).

- OFF
- Sleep/Idle: device is enabled but no active transactions

- Active

4.1.4 Memory Power Management Unit

The Memory PMUs manage power state for the various memory subsystems. Each memory subsystem will support the following power modes.

- OFF (no memory retained for volatile RAM, power down mode for non-volatile memory)
- Retention (corresponding memory is held at retention level, all memory contents are maintained)
- Sleep/Idle (device is enabled but no active transactions)
- Active

Note that the primary power state for all memory in the SoC is dependent on the CPU power state. Once CPU goes into Deep Sleep mode, all memories can enter into retention or OFF mode (depending on the software configuration). When in this mode, DMA transactions or accesses from other peripherals (such as Graphics) are on-demand. On access, the PMU ensures the target memory is powered up into Active mode before servicing the transaction.

4.2 Power Management Controller

The power management controller provides control functions for each supply regulator as well as the primary power gates under digital logic control. The power management controller receives input from all PMUs indicating requested power levels and also controls from software (via power management control registers). A power management mapping configuration is also provided (sourced from trims shadowed to the power management controller) which dictates the functional operation at the regulator interface based on the input power requests. This mapping configuration allows the power management functionality to be programmatic enabling characterization, tuning and/or bug fixes.

Following are the supply regulator interfaces:

- SIMO Buck
- Core LDO
- Mem LDO
- MEM LP LDO

The central power controller is also responsible for controlling power gate enables for all digital power domains. The power gate enables are controlled based on the power level requests. When an “OFF” level is requested from the respective requester PMU or a software override is asserted to force a requester “OFF” or, for I/O requesters, when the corresponding I/O device enable is deasserted, the respective power gate enable is asserted to power off the domain. For all other power level requests, the power gate is disabled powering up the respective domain. It also controls the power muxes that source the various voltages to each of the corresponding power domains.

SSRAM and MRAM power domains are controlled based on the dependent requester domains. For MRAM, if CPU PMU requester is “OFF” *and* DMA requesters are “OFF” or “Sleep”, the MRAM power domain is powered OFF. For SSRAM, each SSRAM bank is powered OFF either based on the SKU memory configuration or if CPU requester is “OFF” *and* DMA requesters are “OFF” or “Sleep” and the SRAM is enabled to power off based on the power control MEMPWDINSLEEP configuration.

4.2.1 System Power States

At the SoC level, various power states are supported to enable key workloads and ensure maximum power efficiency. The system power states are defined in the following sub-sections. Mentioned in each of these system power state sections is the powering up and sleep mode retention of SRAM. SRAM consists of Shared SRAM (SSRAM) and Tightly Coupled Memory (TCM). The power-up and sleep mode retention settings for each of these memories is done via separate register settings whereby individual banks of SSRAM are selected to be powered on and their retention selected with the PWRCTRL_

SSRAMPWREN_PWRENSSRAM field and the PWRCTRL_SSRAMRETCFG_SSRAMPWDSLP field, respectively. The power-up and sleep mode retention settings for TCM is done via the PWRCTRL_MEMPWREN_PWRENTCM field and the PWRCTRL_MEMRETCFG_TCMPWDSLP field, respectively. Note that in deep sleep mode, a portion, all or none of the enabled SSRAM/TCM can be selected for retention while in normal sleep mode whatever SSRAM/TCM is enabled is retained.

4.2.1.1 SYS Active (SACT)

The CPU is in one of the Active Modes and executing instructions. All respective memory and I/O devices are powered on and available as needed.

4.2.1.2 SYS Sleep Mode 0 (SS0)

SYS Sleep Mode 0 is a low power state for the SoC and can be entered if all processor cores are in sleep mode or deeper sleep state.

In this mode, the following conditions apply:

- All *enabled* SRAM memory (SSRAM and TCM) is retained (up to 3.75 MB).
- NVM memory is in standby.
- HFRC is on.
- Main core clock domain(s) is gated but peripheral clock domains can be on.

This state can be entered if a peripheral device (SPI/UART/I2C/MSPI, etc) is actively (or intermittently) transferring data but the window of acquisition is long enough to allow the processor(s) to go into a deeper low power state.

4.2.1.3 SYS Sleep Mode 1 (SS1)

SYS Sleep Mode 1 can be entered if all processor cores are in sleep mode or deeper sleep state, and all peripheral devices are idle and no peripheral device (SPI/UART/I^2C/MSPI, etc) is actively transferring data. However, communication may occur within a short time window which prevents the processor(s) from entering Deep Sleep Mode (and subsequently the system from entering a lower power state).

This state is also referred to as “Active Idle” whereby all power domains can be powered on but all clocks are gated. This state is a good power baseline for the system as it represents the active mode DC power level. Typically, the power in this state is dominated by leakage and always-on functional blocks.

In this mode, the following conditions apply:

- All *enabled* SRAM memory (SSRAM and TCM) is retained (up to 3.75 MB).
- NVM memory is in standby.
- HFRC is on.
- All functional clocks are gated.

4.2.1.4 SYS Deep Sleep Modes

There are 4 levels of SYS Deep Sleep Mode as described in the sub-sections below. Each of the four modes represents a deeper level of sleep and a proportionate reduction in power draw.

In Deep Sleep Mode 0-2, SRAM (SSRAM and TCM) can have a configurable amount of memory in retention depending on the software/system functional and latency requirements. SSRAM retention options, which do not include available selections for size of TCM retention, are the following:

- 3072 kB (All)
- 2048 kB
- 1024 kB
- 0 kB

The ITCM/DTCM retention options in these modes are (1) all *enabled* TCM is retained and (2) no TCM is retained, where the enabled TCM options are:

- 256 kB of ITCM and 512 kB of DTCM
- 128 kB of ITCM and 256 kB of DTCM
- 32 kB of ITCM and 128 kB of DTCM
- 0 kB of ITCM and 0 kB of DTCM

4.2.1.4.1 SYS Deep Sleep Mode 0 (SDS0)

SYS Deep Sleep Mode 0 is a deep low power state for the SoC. This state can be entered if a peripheral device (SPI, UART, I^2C, MSPI, etc.) is actively or intermittently transferring data but the window of acquisition is long enough to allow the processor(s) to go into a deeper low power state.

In this mode, the following conditions apply:

- All processors are in Deep Sleep mode and/or are powered OFF.
- Configurable amount of SRAM (SSRAM and TCM) is in retention (capacity controlled by software).
- Cache memory is in retention.
- NVM memory is in power down.
- HFRC can be on depending on the state of the peripherals needing the HFRC clock.
- Main processor power domains are off but peripheral power domains can be on.

4.2.1.4.2 SYS Deep Sleep Mode 1 (SDS1)

SYS Deep Sleep Mode 1 is another deep low power state for the SoC. This state can be entered if the latency to warm up the cache can be tolerated. This could be an extended wait for a peripheral communication event.

In this mode, the following conditions apply:

- All processors are in Deep Sleep mode or are powered OFF.
- Configurable amount of SRAM (SSRAM and TCM) is in retention (capacity controlled by software).
- Cache memory is powered off (no retention).
- NVM memory is in power down.
- HFRC can be on depending on the state of the peripherals needing the HFRC clock.
- Main processor power domains are off but peripheral power domains can be on.

4.2.1.4.3 SYS Deep Sleep Mode 2 (SDS2)

SYS Deep Sleep Mode 2 is the minimum power state that the processor(s) can resume normal operation. This state can be entered when all activity has suspended for a duration of time sufficient to sustain the longer exit latencies to resume. This could be a state where periodic data samples are taken and the data is locally processed/accumulated/transferred at long time intervals. This state can only be entered (vs SDS1) if the peripheral devices are either not enabled/active or if the application can afford to save/restore the state of the controller(s) on entry/exit of this mode.

In this mode, the following conditions apply:

- All processors are in Deep Sleep or are powered OFF.
- Minimal SRAM (SSRAM and TCM) memory is retained as needed for software to resume.
- Cache memory is powered off (no retention).
- NVM memory is in power down.
- HFRC is off.
- XTAL can be on depending on the configuration of timers.
- All internal switched power domains are off/gated.
- Processor logic state is retained.

4.2.1.4.4 SYS Deep Sleep Mode 3 (SDS3)

SYS Deep Sleep Mode 4 is a deep sleep power state that can be entered on long periods of inactivity.

In this mode, the following conditions apply:

- All processors are in Deep Sleep or are powered OFF.
- No memory is in retention, all memory is powered down.
- LFRC is on (HFRC and XTAL are off)
- All internal switched power domains are off/gated.
- Processor logic state is retained.

4.2.1.5 SYS OFF Mode (SOFF)

In SYS OFF Mode, SoC is completely powered down with no power supplied. This mode is controlled external to the SoC by removing power to the device.

- Processors are in shutdown mode with no state retention.
- Only NVM memory is retained.

4.3 Program Control of Power Management

The transition between power modes is largely directed by software and the workload/task requirements.

4.3.1 CPU

Transitioning to different power modes is initiated through a couple methods depending on the software intent and performance/power/latency requirements. The different mode transitions are described in the following table.

Table 6: Transitioning among Power Modes

	Deep Sleep	Sleep	Active - LP	Active - HP
Sleep/ Deep Sleep	X	X	WAKE+LP	WAKE+HP
Active - LP	WFI (DS)	WFI (S)	X	HP
Active - HP	WFI (DS)	WFI (S)	LP	X

- WFI (DS): Issue WFI instruction Deep Sleep
- WFI (S): Issue WFI instruction Sleep
- LP: Write to CLKGEN_PERFREQ register indicating “LP”. Check CLKGEN_PERFSTAT to check if mode switch completed and if performance mode is available. Continue execution.
- HP: Write to CLKGEN_PERFREQ register indicating “HP”. Check CLKGEN_PERFSTAT to check if mode switch completed and if performance mode is available. Continue execution.

CPU active state transitions are controlled via the PWRCTRL_MCUPERFREQ register. Software requests the appropriate performance mode (LP or HP mode) by writing to the MCUPERFREQ field as appropriate. Software must check that it received an acknowledge of the performance mode request (by checking the MCUPERFACK and MCUPERFSTATUS fields. It is possible that the PMU will not honor a performance mode change request (i.e. in the case where max power condition might be exceeded). Once acknowledged, the CPU should be operating in the corresponding performance mode until software switches to a different mode.

ERRATUM NOTICE

After transitioning from low power (LP) mode to high performance (HP) mode, the MCU still uses the clock for LP (HFRC) after the switch if the clock for HP (HFRC2) is not enabled before switching. For the HP HFRC2 clock to immediately go into effect upon transition from LP mode to HP mode, the HFRC2 clock must be enabled and allowed a settling time for the HFRC2 clock to stabilize before the transition.

See “ERR024: PWRCTRL: MCU continues to use the clock for LP mode (HFRC) after switching from LP to HP mode” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

4.3.2 GPU

GPU active state transitions are controlled via the PWRCTRL_GFXPERFREQ and PWRCTRL_GFXPWRSWSEL registers. Software must sequence the GFXPWRSWSEL and GFXPERFREQ settings properly to ensure proper transition to/from HP and LP mode. Also note that switching of operating mode for GFX must only be done when the GFX device is powered OFF.

For any HP mode transition, software must perform the following sequence:

1. Set GFXPWRSWSEL_GFXVDDSEL bit to “VDDF” (0x1) level.
2. Set the desired GFXPERFREQ field setting.

4.3.3 I/O

The I/O power modes are determined by how the I/O controller is configured. For example:

- OFF: Controller power domain is OFF, “device enable” bit not set in power controller. This transition can also be made by the I/O PMU if auto-power-off is supported.
- Sleep: Controller is “device enabled” but the controller interface has not been enabled/activated (AKA IDLE). This transition can also be made by the I/O PMU if auto-power-on is supported.
- LP: This needs to be determined based on the operating mode of the controller. This typically will be for high performance interfaces (such as MSPI).

4.3.4 Memory

The memory power modes are determined by PWRCTRL register configuration and the relative state of the various mains in the SoC. The primary state of all memories is dictated by the CPU. Once the CPU goes into Deep Sleep mode, all memories can go into retention or power down mode. If any outstanding transaction exists for a given memory target, the power controller will keep that respective memory device powered in Active mode or will wake the memory from retention or power down mode. Once Active, the outstanding transaction can be completed. There are hysteresis counters to keep memories powered up for longer periods of time to avoid thrashing.

The memory is configured by PWRCTRL_MEMPWREN and PWRCTRL_MEMRETCFG (for MRAM, CPU TCM and cache memories) as well as PWRCTRL_SSRAMPWREN and PWRCTRL_SSRAMRETCFG (for Shared SRAM memories) registers. If a memory is not enabled, the retention configuration is a don't care. Only if enabled, the retention configuration applies and will be enforced whenever the respective memories can enter lower power states.

4.4 Additional Information

Please refer to the PWRCTRL registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

5. Security

5.1 Features

The Apollo510B SoC provides secure boot and security functions leveraging Ambiq's SecureSPOT™ technology, and additionally supports the Arm Platform Security Architecture (PSA) and is TrustZone® compliant.

Key security features include:

- TrustZone® technology (ArmV8.1-M)
- Physically Unclonable Function (PUF)
- Tamper resistive fuses and key storage bank
- Secure Boot
- Secure Over-the-Air (OTA) Updates
- Secure Wired Updates
- Secure Key Storage
- Key revocation
- Secure debug
- Secure lifecycle management
- Crypto Subsystem (See "Crypto Subsystem" on page 55 for features and details.)

Please refer to the Security and Crypto registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

5.2 Functional Overview

The Apollo510B SoC enables the security extension on the Cortex-M55 (TrustZone-M) and protection of a subset of memories and peripherals. This enables the device to incorporate Trusted Execution Environment (TEE) into its software architecture. TrustZone technology creates a new processor execution domain, the secure domain.

5.3 TrustZone-M Basics

Arm TrustZone technology enables the system and the software to be partitioned into Secure and Normal worlds whereby secure software can access both secure and nonsecure memories and peripherals, while normal software can only access nonsecure memories and peripherals. These security states are orthogonal to the existing Thread and Handler modes, enabling both a Thread and a Handler mode in both secure and nonsecure states.TrustZone-M is memory map-based where the instruction address determines the security state of the processor. Memory and other critical resources designated as secure can only be accessed when the core is executing in secure state. There are two separate MPUs for the secure and nonsecure world.

Memory can have the following security attributes:

- Nonsecure (NS)
- Secure (S)
- Nonsecure Callable (NSC)

The security attributes of memory are configured using the following constructs:

- Implementation Defined Attribution Unit (IDAU) – Fixed in implementation
- Security Attribution Unit (SAU) – Classifies memory regions as S/NS/NSC

Interrupt handling is performed by classifying interrupts as Secure or Nonsecure in the NVIC.

5.3.1 TrustZone-M in the Apollo5 Family SoCs

TrustZone technology is supported in the Apollo5 family's Cortex-M55 core whereby security attributes of the instruction address determine the security state of the processor. Outside of the core TrustZone support is limited in that all other mains (DMA, GPU, DC) during run-time are treated as nonsecure. Because of this, secure memory cannot be accessed by other mains and must be configured separately. As mentioned above, secure memory is configurable using SAU.

The BootROM helper function region should be classified as secure, while portions of ITCM, DTCM and SSRAM can be classified as secure. Protecting secure memory from external nonsecure access is accomplished by two means:

- TCM Gate Units (TGU) for ITCM and DTCM
- SSRAM Protection (SSRAMPROT) for SSRAM

Secure Peripherals on the APB are configurable using SAU & NVIC. Recommended modules to configure as Secure Peripherals are the following:

- Watchdog
- PWRCTRL
- MCUCTRL
- RESETGEN
- STIMER
- RTC
- CLOCKGEN

System Security Control (SSC) registers are used for global control/locking of peripheral and memory registers.

In the boot flow, Secure Boot (SBR+SBL) always runs in Secure Execution Mode. The SBR/SBL transitions to the Secure Firmware Image, which contains the Customer Firmware Entry. It too is always in Secure Execution Mode. This portion of firmware is responsible for system partitioning into secure/ nonsecure domains by using SAU, TGU, SSRAMPROT and NVIC configurations. The flow eventually transitions to the nonsecure Firmware Image.

5.4 Physically Unclonable Function (PUF)

The Apollo510B SoC incorporates a PUF that can be utilized by software and is used internally to secure the OTP memory, providing enhanced protection of assets. See “OTP” on page 40 for more information about PUF features.

5.5 Secure Boot

The Secure Boot feature on the Apollo510B SoC provides a secure foundation for customer firmware/ services. The secure boot loader provides authentication, decryption and integrity validation for all firmware upon installation and boot/reset. Secure boot loader provides firmware recovery and OTA update support.

Secure Boot policy can be used to direct the secure boot loader based on the customer security requirements.

A high level flow diagram of the Secure Boot process is illustrated below in Figure 6. See the “Apollo5 Security Guide” [To Be Supplied] for more details.

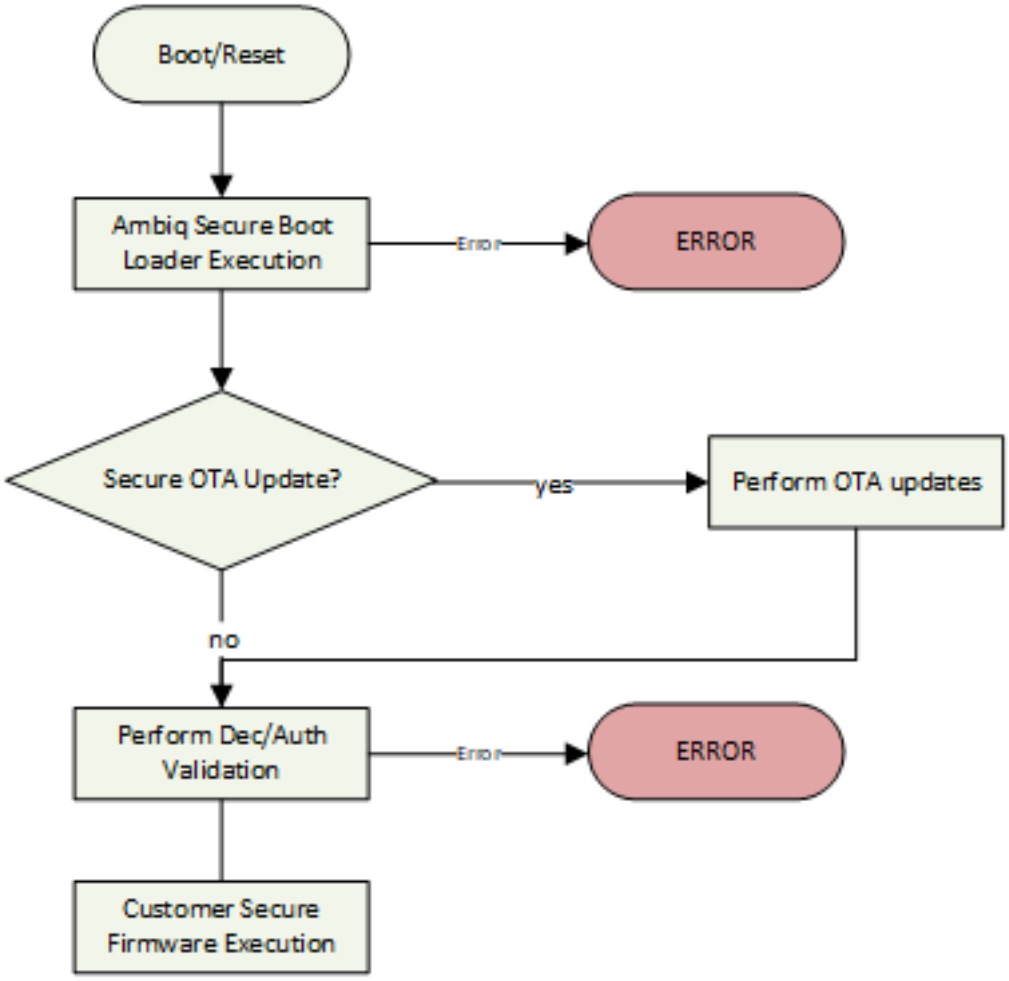

Figure 6. Secure Boot Process Flow Diagram

5.6 Secure OTA

The Apollo510B SoC supports secure OTA leveraging the Ambiq secure boot loader. Customers can update any firmware component securely as directed via the security policy configuration. The basic Secure OTA flow is shown in Figure 7.

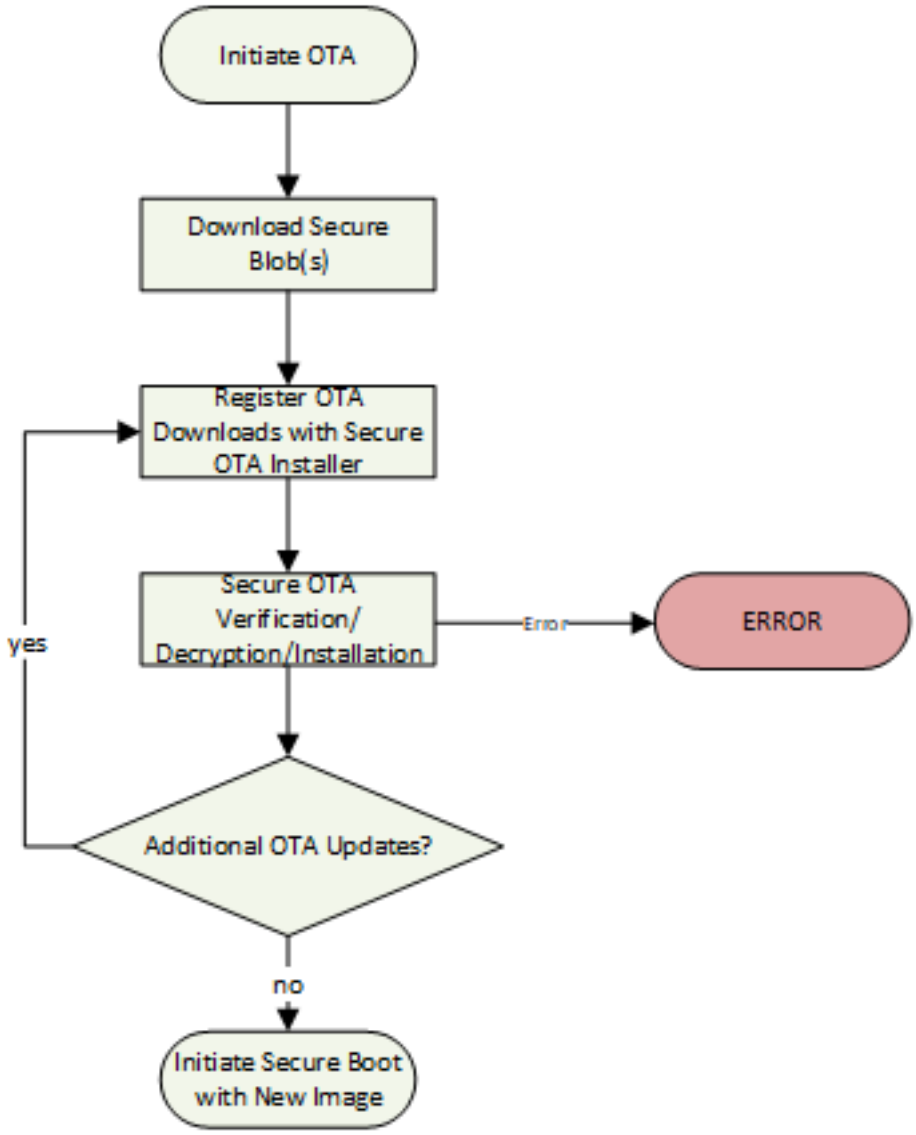

Figure 7. Secure OTA Flow Diagram

5.7 Secure Key Storage

Key material is managed by hardware and exposed to software via security APIs. The keys are stored securely in OTP memory and are never directly accessible to software. Certain key material is used/ accessible only during certain lifecycle state of the device. These are mainly used for provisioning of the device.

5.7.1 Software Keys

Additionally, there are “Software Keys” available to use in OTP (INFOC) that can be provisioned by OEM. These keys can be configured to be accessible only to privileged software (e.g., bootloader).

ERRATUM NOTICE

Keybank1, Keybank2 and Keybank3 keys cannot be used as AES keys for use with secure OTAs or wired updates. Keybank0 keys (4 total at kek index 0x80-0x83) can be used.

See “ERR033: Boot Loader: Keybank restrictions when used for OTA encryption” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

5.8 Secure Lifecycle States

The Apollo510B SoC supports the following lifecycle states:

- Chip Manufacturer (CM)
- Device Manufacturer (DM)
- Secure
- RMA

The lifecycles are managed by hardware and OTP.

5.9 Secure Debug

The debug sub-system has been enhanced in the Apollo510B SoC to provide separate capabilities for secure and nonsecure debug. If only nonsecure debug is enabled, then no secure resources may be accessed, and no secure code may be stepped into, debugged, or traced.

5.10 Crypto Subsystem

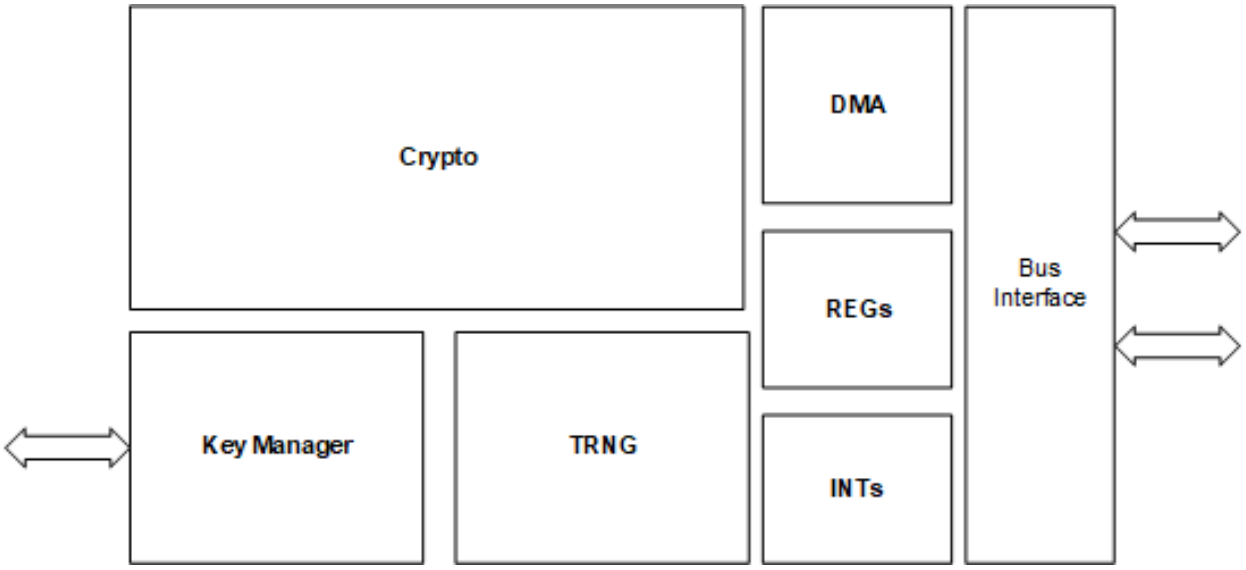

Figure 8. Crypto Subsystem Block Diagram

The Apollo510B SoC's Crypto Subsystem provides the cryptographic acceleration and isolation required to support the Apollo5 family security model. These services are managed by software to support private and public-side cryptographic functions, and includes features shown in Figure 8 and listed below.

- Cryptographic acceleration for the protection of data-in-transit and data-at-rest.
- Protection of various assets belonging to the chip manufacturer (ICV) or device manufacturer (OEM), service operators providing services over the target device and the device. These asset protection features include:
  - Image verification at boot/during runtime
  - Authenticated debug
  - Random number generation
  - Security lifecycle state management
  - Asset Provisioning

The following standard specifications are supported:

- FIPS Publication 186-4: Digital Signature Standard (DSS), July 2013, compliant with sections 5.1, 6.2, 6.3, 6.4, B.1.2, B.2.2, B.3.6, B.4.2, C.3.1, C.3.3, C.3.5, C.9, and D.1.2.
- FIPS Publication 197: Advanced Encryption Standard, support only 128-bit and 256-bit keys.
- NIST SP 800-38A: Recommendation for Block Cipher Modes of Operation: Methods and Techniques, compliant with sections 6.1, 6.2, 6.4, and 6.5.
- NIST SP 800-38B: Recommendation for Block Cipher Modes of Operation: the CMAC Mode for Authentication
- NIST SP 800-108: Recommendation for Key Derivation Using Pseudorandom Functions, compliant with section 5.1.
- Standards for Efficient Cryptography Group (SECG): SEC1 Elliptic Curve Cryptography, 2000, compliant with sections 2.1.1, 2.2.1, 3.1.1, 3.2, 3.3.1, 3.6.1, 4, and 6.1.

5.10.1 Crypto Acceleration

The CryptoCell-312 crypto accelerator is available to both the secure and the nonsecure domains. The following cryptographic features are supported:

- AES (128, 192, 256 bit)
  - ECB, CBC, CTR, OFB
  - CMAC, CBC-MAC, AES-CCM, AES_GCM
- AES Key Wrapping
- CRC32 with crypto acceleration
- External storage inline encryption/decryption with crypto acceleration
- Diffie-Hellman (1024, 2048, 3072 bit)
  - ANSI X9.42-2003: Public Key Cryptography for the Financial Services Industry: Agreement of Symmetric Keys Using Discrete Logarithm Cryptography.
  - Public-Key Cryptography Standards (PKCS) #3: Diffie-Hellman Key Agreement Standard.
- ECC Key Generation (NIST and 25519 curves)
- ECIES
- ECDSA
- ECDH
- SHA1/SHA224/SHA256
- HKDF
- KDF
  - NIST SP 800-108: Recommendation for Key Derivation Using Pseudorandom Functions
- RSA PKCS#1 (2048, 3072, 4096b)
  - Public-Key Cryptography Standards (PKCS) #1 v2.1: RSA Cryptography Specifications
  - Public-Key Cryptography Standards (PKCS) #1 v1.5: RSA Encryption
- RSA Key Generation
- True Random Number Generator (TRNG)
  - BSI AIS-31: Functionality Classes and Evaluation Methodology for True Random Number Generators.
  - NIST SP 800-90B: Recommendation for the Entropy Sources Used for Random Bit Generation.

See more detailed information at the CryptoCell-312 page of the Arm Developer site.

5.11 Additional Information

Please refer to the Security and Crypto registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

6. Reset Generator (RSTGEN)

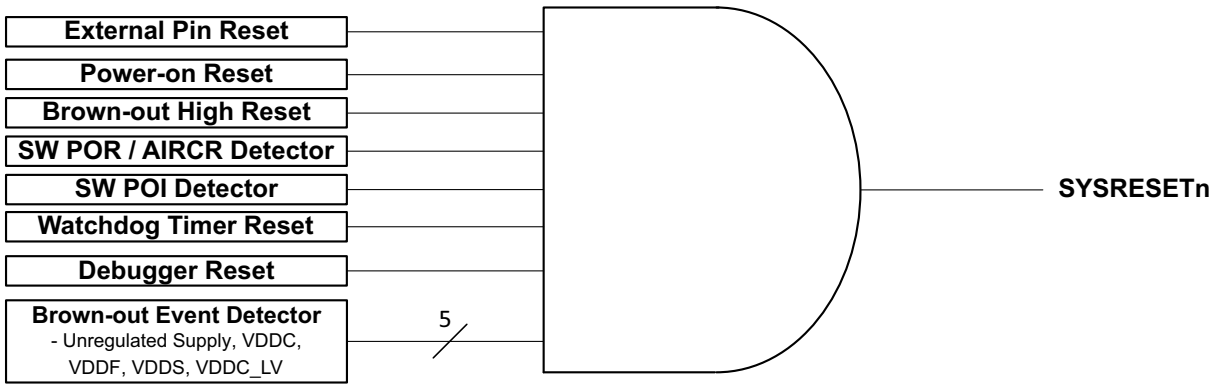

Figure 9. Reset Generator Module Block Diagram

6.1 Features

There are various resets that can be initiated in the Apollo510B SoC. Depending on the level of reset, certain functions may get cleared or may persist values or executing across specific reset assertions. In all cases, the source of a reset is captured in RSTSTAT register.

The Reset Generator Module (RSTGEN) supports reset sources shown in Figure 9 and listed below.

- External reset pin (RSTn)
- Power-on event (POA)
- Brown-out event (BODL)
- Software requests
- Debugger request
- System request (AIRCR SYSRESETREQ from the Cortex-M55)
- Watchdog expiration

6.2 Functional Overview

The Reset Generator Module (RSTGEN) monitors a variety of reset signals and asserts the active low system reset (SYSRESETn) accordingly. A reset causes the entire system to be re-initialized, and the cause of the most recent reset is indicated by the STAT register.

There are four levels of reset on the Apollo510B SoC:

- SYSRESETn System Software Reset
- Software POR Reset
- Software POI Reset
- Power-on Analog (POA) Reset

SYSRESETn is triggered by AIRCR.SYSRESETREQ, a Cortex-M55 warm reset.

Most resets trigger a POR reset, which is a shallow reset. This includes a Watchdog reset, a pin (RSTn) reset and a Cortex-M55 cold reset.

A POI reset is the deepest digital reset affecting hardware subsystems.

POA is the very deepest reset, digital and analog, and is only triggered by voltage going below POA voltage.

The effect of each of these reset levels on SoC modules and functionality is summarized in the following table and described in more detail in the following sections.

Table 7: Reset Levels and Affected Components

Reset Level	CPU, GPIO and Peripherals (Except XT, LFRC, RTC and STIMER)	Debug Subsystem	CLKGEN (XT, LFRC, etc.), Reloads INFO Settings (Trims, Options and Security)	RTC and STIMER
SYSRESETn	x			
POR[1]	x	x		
POI[2]	x	x	x	
POA (Power-on Reset)	x	x	x	x

1. Doesn't affect CLKGEN except for setting the CPU clock to 96 MHz.
2. Reloads CLKGEN_OCTRL_OSEL bit from trim and resets CLKGEN features such as registers, CPU clock, HFADJ and HF2ADJ - everything else is reset only by POA.

NOTE

There is a delay of 500 µs after a POR reset trigger before the reset actually occurs. During this delay the CPU continues to execute instructions.

ERRATUM NOTICE

All the power domains can be trimmed to be powered on after a SWPOI reset. In the failure case, some of the power domains might not power up as expected after a SWPOI reset. This is a hardware startup issue, which could result in non-functional peripherals/memories. A workaround for this issue is implemented in the pre-installed SBL and hence is not visible to, or need be a part of, a user application.

See “ERR026: PWRCTRL: Some power domains might not power up as expected after a SWPOI reset” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

6.3 External Reset Pin

The active-low RSTn pin can be used to generate a reset using an off-chip component (e.g., a push-button). An internal pull-up resistor in the RSTn pad enables optional floating of the RSTn pin, and a debounce circuit ensures that bounce glitches on RSTn does not cause unintentional resets. The RSTn pin

is not maskable. An internal pull-down device will be active during a brownout event pulling the RSTn pin low. See Figure 10.

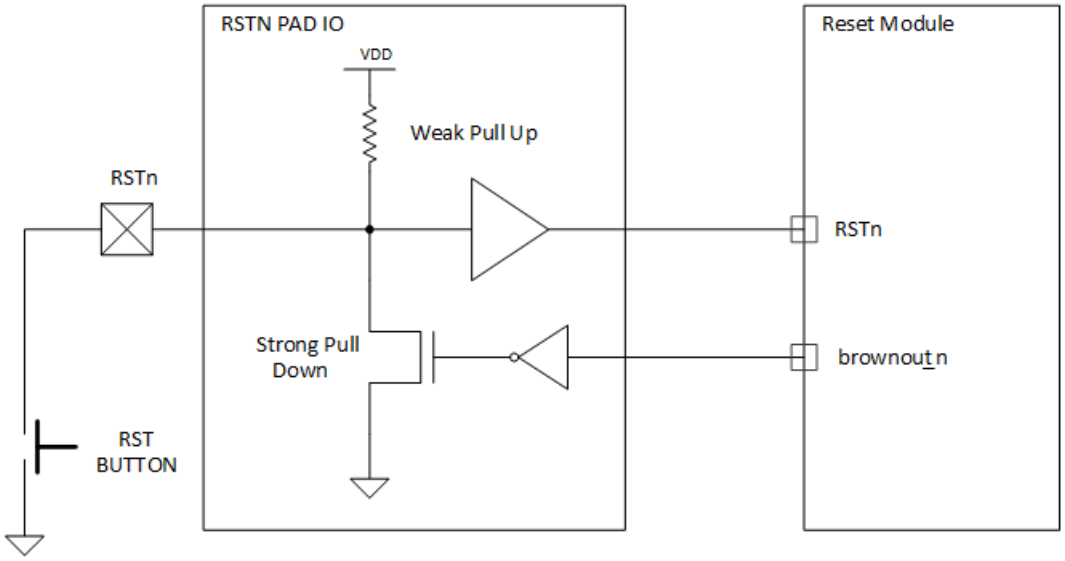

Figure 10. Block Diagram of Reset Pin Circuitry

6.4 Power-on Event

An integrated power-on detector monitors the supply voltage and keeps SYSRESETn asserted while VDD is below the rising power-on voltage, V_{POR+}. When VDD rises above V_{POR} at initial power on, the reset module will initialize the low power analog circuitry followed by deassertion of SYSRESETn, and normal operation proceeds. SYSRESETn is re-asserted as soon as VDD falls below the falling power-on voltage, V_{POR-}. The power-on reset signal, PORn, is not maskable.

6.5 Brown-out Events

An integrated brown-out detector monitors the primary supply voltage and causes an automatic and non-configurable reset when the voltage has fallen below the low brownout threshold (BODL).

In addition, there are individual brownout detector monitors integrated within the core/memory and Bluetooth Low Energy supply regulators which cause separate/maskable reset assertions when the voltage falls below a critical level for the respective voltage rails - VDDC, VDDC_LV, VDDS or VDDF. In the event any of the supply voltages fall below its corresponding core/memory/Bluetooth Low Energy threshold if enabled, the reset module will initiate a system reset, enabling the RSTn pull-down and driving the reset pin low. The occurrence of a brownout reset will be reflected by the setting of the associated bit in the RSTGEN's INTSTAT Register after reset

In the event of a brownout detection, the following functionality is maintained until a power down detection occurs.

- All RTC registers retain state.
- RTC and STIMER counters continue operation from 32 kHz XTAL or from LFRC (if below BODL). If clock sources stop oscillating at very low voltage, the RTC and STIMER will continue to maintain state.
- Clock configuration registers retain state.

ERRATUM NOTICE

The brown-out reset status bit, RSTGEN_STAT_BORSTAT, may inadvertently get set due to the brown-out signals powering up inconsistently during system power-up. Whether the status bit gets set is influenced by the voltage levels of the power supplies (VDDH/VDDP/VDDA) and the ramp rate of these supplies.

See “ERR027: RSTGEN: Brown-out reset status bit may get set inadvertently during power-up” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

6.6 Software Reset

The SYSRESETn reset may be generated via software using the Application Interrupt and Reset Control Register (AIRCR) defined in the Cortex-M55. For additional information on the AIRCR, see the Arm document titled “Cortex-M55 Devices Generic User Guide.” The software reset request is non-maskable.

A second source for the identical software reset functionality is made available through the SWPOR register in the RSTGEN peripheral module. This reset causes a reset to all blocks except for registers in CLKGEN, RTC, STIMER and the power management unit. Most resets trigger a POR reset, which is a shallow reset. POR doesn't affect CLKGEN except that it sets the CPU clock to 96 MHz.

A third source of reset, which is the deepest digital reset affecting hardware subsystems, is made available through the SWPOI register. Writing the key value (0x1B) to this register triggers a Software POI reset, which causes:

- INFO space settings to be reloaded from Flash.
- a reset of all blocks except for registers in the RTC and the STIMER.
- the reloading from trim of the OSEL bit to the CLKGEN_OCTRL register, which selects either the LFRC or the XTAL to be used as the RTC clock source.
- reset of the CLKGEN features such as registers, CPU clock, HFADJ and HF2ADJ - everything else is reset only by POA.

6.7 Watchdog Reset

The Watchdog Timer sub-module generates an interrupt if it has not been properly managed by software within a pre-defined time. The watchdog reset is maskable.

6.8 Additional Information

Please refer to the RSTGEN registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

7. Clock Generator (CLKGEN)

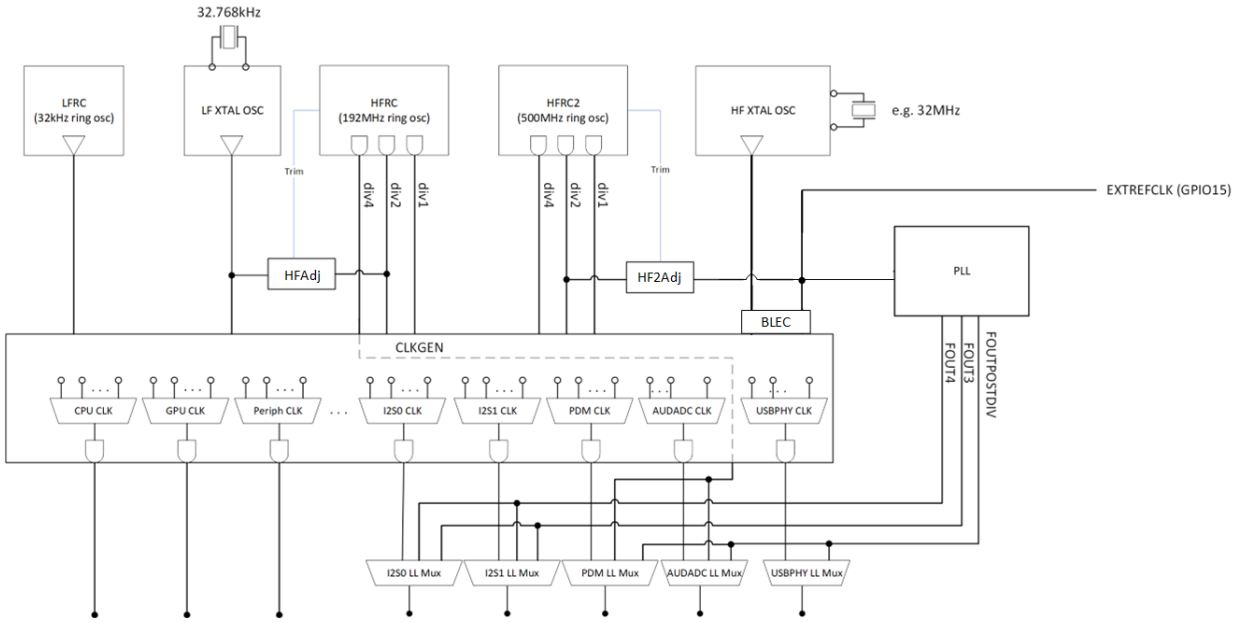

Figure 11. Block Diagram for Clock Generator Module

NOTE
For the Apollo510B SoC the HF XTAL OSC in the above block diagram, referred to as BLE XTAL in 7.2.1.2 and elsewhere in the document, is not a direct clocking option for the M55, as those external pins are connected internally to the BLEC. A div-by-4 of this clock (12 MHz) is internally available on EXTREFCLK (GPIO15) and can be used to clock other modules.

7.1 Features

The Apollo510B SoCs clock generation subsystem is responsible for generating all of the primary and derived clocks in the SoC.

- Independent frequency scaling for various SoC subsystems
- Ultra low power, low frequency clock generation with XTAL calibration
- Programmable I/O clock dividers
- High precision audio clock generation
- High precision / low jitter PLL for high-fidelity audio and high-speed USB

NOTE
When enabling a module which automatically starts clocking with a default clock source, or when changing the clock source for any enabled module, there is a required 30 µs settling time for the selected clock.

7.2 Functional Overview

A high-level view of the Clock Generator Module, which supplies all clocks required by the Apollo510B SoC, is shown in Figure 11. Note that the output clock frequencies from the clock sources are nominal values. Consult the Electrical Characteristics section for specified values.

7.2.1 Clock Generation Subsystem

The clock generation subsystem consists of the following sub-modules:

- Low-frequency crystal oscillator circuit (XTAL)
- 48 MHz BLEC crystal oscillator circuit (BLE XTAL)
- 2x High-frequency RC oscillators (HFRC and HFRC2)
- Low-frequency RC oscillator (LFRC)
- High-frequency PLL circuits
- SoC clock generation logic
- Audio subsystem clock generation logic

7.2.1.1 Low-Frequency Crystal Oscillator (XTAL)

The high accuracy XTAL Oscillator is tuned to an external 32.768 kHz crystal, and has a nominal frequency of 32.768 kHz. It is used when frequency accuracy is critically important. To minimize power consumption, the XTAL is only enabled when an internal module is using it.

It should be noted that the XTAL oscillator is also optional if the requirements of the design can tolerate the internal LFRC/HFRC oscillator specifications.

External load capacitors are required to tune the XTAL oscillator circuit. Refer to “Clocks/Oscillators” on page 228 for more guidance and specifications.

NOTE

The XTAL is highly sensitive to external leakage on the XI pin. Therefore it is recommended to minimize the components on XI and to use extremely low leakage load capacitors.

The RTC clock source, either the LFRC Oscillator or the XTAL Oscillator, is selected via the CLKGEN_OCTRL_OSEL bit. If the XTAL Oscillator experiences a temporary failure and subsequently restarts, the Apollo510B SoC will switch back to the XTAL Oscillator.

A 32 kHz reference clock is output from the XTAL circuit to several GPIO pins on all packages.

7.2.1.2 High-Frequency Crystal Oscillator (BLE XTAL)

A 48 MHz crystal provides the clock for the BLEC and other module. This crystal, connected to pins BLE_XIN and BLE_XOUT, sets the primary clock input for the radio subsystems. The output of this crystal clock provides an alternate internal high-frequency clock source to synchronize various clock generators within the SoC (such as the system PLL, DSI and/or USB PLL) to avoid interference with or spur injection to the BLEC subsystem. This internal clock utilizes GPIO15’s EXTREFCLK function and should not be used for any other purpose. Despite the function’s name, it is not available for external use and the pin must be left unterminated.

7.2.1.3 Low-Frequency RC Oscillator (LFRC)

The low-power low-frequency RC block, LFRC, with a nominal frequency of 900 Hz, provides the low-frequency clocks for timers and other logic within the SoC. It is used when short-term frequency accuracy is not important. It also supplies clocks for the SIMO buck regulator in low power mode as well as some basic state machines and is always enabled.

7.2.1.4 High Frequency RC Oscillator (HFRC)

The high-frequency RC oscillator (HFRC) provides all the primary clocks for the high-frequency digital processing blocks in the SoC except for audio, radio and HP mode clocks. These clocks are gated/ selected based on performance requirements. The digital clocks are isolated to avoid noise injection into the critical clocks for audio and radio communications. Additionally, the high-frequency digital clock is programmatically divided to generate the various I/O clocks in the system. All high-frequency clocks can be gated if not needed. The HFRC also supports a frequency-locked loop (FLL) circuit to ensure the HFRC oscillator locks to a specific frequency range to ensure high quality/low ppm output reference as needed to meet audio clock quality requirements. The HFRC uses the 32 kHz XTAL as the reference clock for calibration.

The high-frequency HFRC Oscillator, with a nominal frequency of 96 MHz, is used to supply all high-frequency clocks in the Apollo510B SoC such as the processor clock for the Arm core, memories and many peripheral modules. Digital calibration is not supported for the HFRC, but its frequency may be automatically adjusted by the auto-adjustment function which is a combination of analog and digital operations.

The HFRC is enabled only when it is required by an internal module. When the Arm core goes into a sleep mode, the HFRC will be disabled unless another module is using it. If the Arm core goes into deep sleep mode, the HFRC will be powered down when it is not needed. When the HFRC is powered up, it will take a few microseconds for it to begin oscillating, and a few more microseconds before the output is completely stable. In order to prevent erroneous internal clocks from occurring, the internal clocks are gated until the HFRC is stable.

7.2.2 Secondary High-Frequency RC Oscillator (HFRC2)

A secondary high-frequency RC block, HFRC2, provides the optional high-frequency clocks needed for the CPU and GPU in HP mode and optionally for MSPI high-frequency mode. The HFRC2 also supports an FLL circuit (via HFAdj2) to ensure the HFRC2 oscillator locks to a specific frequency range to ensure high quality/low ppm output reference as required for audio features. The HFRC2 generally uses the high frequency XTAL as the reference clock for calibration, but can also use an external reference clock.

7.2.2.1 System PLL

The system PLL is used to generate the high-precision clocks needed for high-fidelity audio and for the USB PHY reference clock. The System PLL has the following features:

- Wide output frequency range
- 24-bit fractional accuracy
- 2 post-dividers each with a selectable setting of 1 to 7
- 1 additional divide-by-6 or divide-by-8 post-divider option for audio clocks

ERRATUM NOTICE

The SYSPLL can be clocked only by a divide-by-4 of the 48 MHz high-speed crystal oscillator (BLE XTAL), which is the 12 MHz internally-accessed EXTREFCLK on GPIO15. If BLE XTAL had been enabled at any time after reset and then disabled, then the selection of the EXTREFCLK as the SYSPLL clock source cannot be made. If the BLE XTAL had been enabled and then disabled, it must be re-enabled to be able to transition the SYSPLL clock source from BLE XTAL (default setting) to the EXTREFCLK.

If BLE XTAL had not been enabled prior to selecting the clock source for the SYSPLL or is not present in the system, then EXTREFCLK can be selected as the SYSPLL clock source directly (by setting the MCUCTRL_PLLCTL0_FREFSEL bit to EXTREFCLK).

See “ERR030: SYSPLL: Special case where the SYSPLL cannot select the EXTREFCLK as its clock source” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

7.3 Clock Sources for Apollo510B SoC

Clock sources used within the SoC are as shown in Table 8. All clock sources except for the external reference clock (EXTREFCLK) can be gated.

Table 8: Requirements for Clock Sources

Clock Name	Frequency	Tolerance	Duty Cycle (% High/ Low)	Additional Requirements / Comments
HFRC_96MHz	96 MHz	±5%	50/50	
HFRC_192MHz	192 MHz	±5%	30/70	
HFRC48	48 MHz			HFRC48 is a dedicated clock from the HFRC block (HFRC192_DIV4); selected by MCUCTRL_PLLMUXCTRL field for the PDM or AUDADC modules only.
LFRC	Nominal 900 Hz		50/50	
HFRC2_125MHz	125 MHz	±5%	50/50	
HFRC2_250MHz	250 MHz	±5%	45/55	
BLE XTAL[1]	48 MHz	±50 ppm[2]	50/50	This 48 MHz clock is used exclusively by the BLEC module. A div-by-4 of this clock (12 MHz) is internally available on EXTREFCLK and can be used to clock other modules.
XT_32KHz[3]	32.768 kHz	±50 ppm[4]	50/50	
EXTREFCLK	Divide-by-4 of the 48 MHz BLE XTAL			The internal clock EXTREFCLK is used to provide an alternate reference clock source as needed to synchronize various clock generators within the SoC.
PLLCLK	1.22 MHz to 960 MHz		50/50	PLLCLK output offered as clock for I^2S and other audio modules in HP mode, and for the USBPHY.

1. See Clocks/Oscillator section of Electrical Characteristics for the specifications and range of frequencies supported by the high frequency XTAL.
2. Required tolerance of the BLE XTAL
3. See Clocks/Oscillator section of Electrical Characteristics for the specifications of the 32 kHz XTAL.
4. Depends on the accuracy of the external 32 kHz crystal. See Clocks/Oscillator section of Electrical Characteristics for crystal requirements.

Clocks used by the CPU, SRAM and MRAM are as listed in Table 9.

Table 9: CPU, Memory and Storage Clocks

Block	Clock	LP		HP		Additional Requirements / Comments
		Frequency	Source	Frequency	Source	
CPU	CLKIN	96 MHz	HFRC	250 MHz	HFRC2	
	IWICCLK	96 MHz	HFRC	250 MHz	HFRC2	Synchronous with CLKIN, same frequency when in use. Gated during sleep.
	PMUCLK	96 MHz	HFRC	250 MHz	HFRC2	Synchronous with CLKIN, same frequency when in use. Gated when not in use.
	STCLK	EXT: 3 MHz	HFRC_DIV32	EXT: 3 MHz	HFRC_DIV32	Asynchronous clock. STCLK has 2 clock sources - EXT and INT.
		INT: 96 MHz	HFRC	INT: 250 MHz	HFRC2	
	DBGCLK	See Debug section in Table 10				Synchronous with CLKIN, Gated when not in use.
	TRACECLKIN	See Debug section in Table 10				Asynchronous clock. Gated. Arm recommends that this match the maximum frequency of the CPU clock.
	SWCLKTCK	See Debug section in Table 10				Input clock on SWJ DAP interface.
Shared SRAM/ Fabric	AXICLK	96 MHz	HFRC			
MRAM	Bus Clock	96 MHz	HFRC			

Clock sources and divider options used by the modules and sub-systems on the SoC are as listed in Table 10.

Table 10: Module Clocks and Dividers

Module / Subsystem	Clock Node	Source / Frequency Selections	Additional Requirements / Comments
USBPHY	Ref Clock 24 MHz	• HFRC_48MHz with HFAdj • HFRC_24MHz with HFAdj • EXTREFCLK • EXTREFCLK_DIV2 • PLLCLK	PLLCLK (FOUTPOSTDIV only) selected by MCUCTRL_PLLMUXCTRL register. All others selected by USB_CLKCTRL_PHYREFCLKSEL field. Quiesce clock option available.
	Bus Clock	• HFRC_96MHz	
USB Controller	Bus Clock	• HFRC_96MHz	
DSIPHY	Ref Clock	• HFRC_24MHz • HFRC_12MHz • EXTREFCLK • EXTREFCLK_DIV2	
	Bus Clock	• HFRC_96MHz	
MSPI	MSPI0: HFRC, HFRC2 MSPI1: HFRC	MSPI0 Sources: • HFRC_96MHz • HFRC_192MHz • HFRC2_125MHz • HFRC2_250MHz MSPI1 Sources: • HFRC_96MHz • HFRC_192MHz	Clock source selected by CLKGEN_MSPIIOCLKCTRL register. Each MSPI further divided by 1, 2, 3, 4, 6, 8, 12, 16, 24 or 32 by MSPI_DEV0CFG_CLKDIV0.
	Bus Clock	• HFRC_96MHz	
SDIO0/1	Ref Clock	• HFRC (up to 96MHz)	Source synchronous. xin_clk is fixed to HFRC_96MHz in the SDK software. HFRC_48MHz and HFRC_24MHz are in Apollo510 MCUCTRL register as options.
	Bus Clock	• HFRC_96MHz	
Crypto	Core Clock	• HFRC_96MHz	
GFX	Core Clock	CLKCTRL_GFXCORECLKSEL: • HFRC_96MHz (LP) • HFRC2_250MHz (HP)	250 MHz HP mode is primary/default frequency and recommended as GPU HP clock.
	Bus Clock	• HFRC_96MHz (LP) • HFRC2_250MHz (HP)	
Display Controller	Bus Clock	• HFRC_96MHz	
	Pixel Clock	• HFRC (12, 24, 48, 96, 192 MHz) • DPHY (TxByteClkHS, 96 MHz max)	In DC+DSI 1-lane mode, DPHYPLL is primary DC clock source. In DC+DSI 2-lane mode, HFRC_96MHz is primary DC clock source. In DC only mode, HFRC_96MHz and HFRC_48MHz are primary DC clock sources.

Table 10: Module Clocks and Dividers

Module / Subsystem	Clock Node	Source / Frequency Selections	Additional Requirements / Comments
Audio Subsystem	PDM I/O CLK 400-3200 kHz	• PDM MCLK	
	PDM MCLK	• HFRC2 31.25MHz (250MHz_DIV8) with HFAdj2 • HFRC_96MHz_DIV4 with HFAdj • EXTREFCLK • PLLCLK • HFRC48	HFRC is the primary clock source. HFRC48 is a dedicated clock from the HFRC (HFRC192_DIV4). PLLCLK (FOUTPOSTDIV only) PLLCLK and HFRC48 selected by MCUCTRL_PLLMUXCTRL register. All others selected by PDM_CTRL_-CLKSEL field. Quiesce clock option available.
	PDM Bus Clock	• HFRC_96MHz	
	I^2S I/O SCLK: 128-3027 kHz	• I^2S SCLK	
	I^2S MCLK	• HFRC DIV1 to DIV128 in octave steps • HFRC2 DIV8 to DIV1024 in octave steps • EXTREFCLK DIV1 to DIV64 in octave steps • PLLCLK: PLLFOUT3 (nominal 8 MHz) or PLL-FOUT4 (nominal 6 MHz)	PLL output frequency is selected by MCUCTRL_PLLMUXCTRL register: • PLLFOUT3 is FOUTPOSTDIV divided by 6, or nominal 8 MHz based on 48 MHz PLL clock ref. • PLLFOUT4 is FOUTPOSTDIV divided by 8, or nominal 6 MHz based on 48 MHz PLL clock ref. All others selected by I2S_CLKCF-G_FSEL field. HFRC is the primary clock source. Quiesce clock option available.
	I^2S NCO Clock	• HFRC2_31.25MHz with HFAdj2 • HFRC_48MHz with HFAdj • EXTREFCLK	
	I^2S Bus Clock	• HFRC_96MHz	
	AUDADC Clock	• HFRC_48MHz with HFAdj • HFRC2_31.25MHz with HFAdj2 • EXTREFCLK • HFRC48 • PLLCLK	HFRC is the primary clock source. HFRC_48MHz is HFRC96_DIV2 and HFRC48 is a dedicated clock from the HFRC (HFRC192_DIV4). PLLCLK option is FOUTPOSTDIV only. PLLCLK and HFRC48 are selected by MCUCTRL_PLLMUXCTRL register. All others selected by AUDADC_CF-G_CLKSEL field. Quiesce clock option available.
	AUDADC Bus Clock	Same as AUDADC.	
WDT	Ref Clock	• LFRC/8, LFRC/64, LFRC/1024, LFRC/16384 •	LFRC source clock is nominally 900 Hz.
	Bus Clock	• HFRC_48MHz	

Table 10: Module Clocks and Dividers

Module / Subsystem	Clock Node	Source / Frequency Selections	Additional Requirements / Comments
Timers	Various Source Clocks	• HFRC_DIV4, HFRC_DIV16, HFRC_DIV64, HFRC_DIV256, HFRC_DIV1024, HFRC_DIV4K • LFRC, LFRC_DIV2, LFRC_DIV32, LFRC_DIV1K • 32 kHz XT: XT (uncalibrated), XT_DIV2, XT_DIV4, XT_DIV8, XT_DIV16, XT_DIV32, XT_DIV64, XT_DIV128 • RTC_100HZ • TMR00, TMR01 - TMR150, TMR151 • GPIO00 - GPIO127 • HFRC2: 16/8/4/2/1 MHz, 512 kHz	LFRC source clock is nominally 900 Hz.
	Bus Clock	• HFRC_48MHz	
IOS	IOS I/O Clock 0.75 - 48 MHz	• External	Sourced from external manager
	Bus Clock	• HFRC_96MHz	
IOM	IOM I/O Clock	• HFRC_48MHZ • HFRC_24MHZ • HFRC_12MHZ • HFRC_6MHZ • HFRC_3MHZ • HFRC_1p5MHZ • HFRC_750KHz • HFRC_375KHz	Quiesce clock option available.
	Bus Clock	• HFRC_96MHz	
UART	UART HF Clock	With HFAdj: • HFRC_48MHZ • HFRC_24MHZ • HFRC_12MHZ • HFRC_6MHZ • HFRC_3MHZ • PLLCLK	
	Bus Clock	• HFRC_96MHz	
GPIO	Bus Clock	• HFRC_48MHz	
PWRCTRL	Bus Clock	• HFRC_48MHz	
Debug	TPIU Clock	• HFRC2_250MHz • HFRC2_125MHz (DIV2) • HFRC_96MHz	Gated when not in use.
	Debug Subsystem Clock	• HFRC2_250MHz • HFRC_96MHz	Gated when not in use. DBGCLK is synchronous with the CPU clock.
	SWD Clock 100 MHz	• External (Pad Input)	SWJ input clock on the DAP. Tools support up to 100 MHz interface.
ADC	ADC Clock	• HFRC 48 MHz (HFRC_96MHz_DIV2) • HFRC 24 MHz (HFRC_96MHz_DIV4) • HFRC2 31.25 MHz (HFRC2_250MHz_DIV8)	
MCUCTRL	Bus Clock	• HFRC_24MHz	
RSTGEN	Bus Clock	• HFRC_24MHz	

7.4 Additional Information

Please refer to the CLKGEN registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

8. Real Time Clock (RTC)

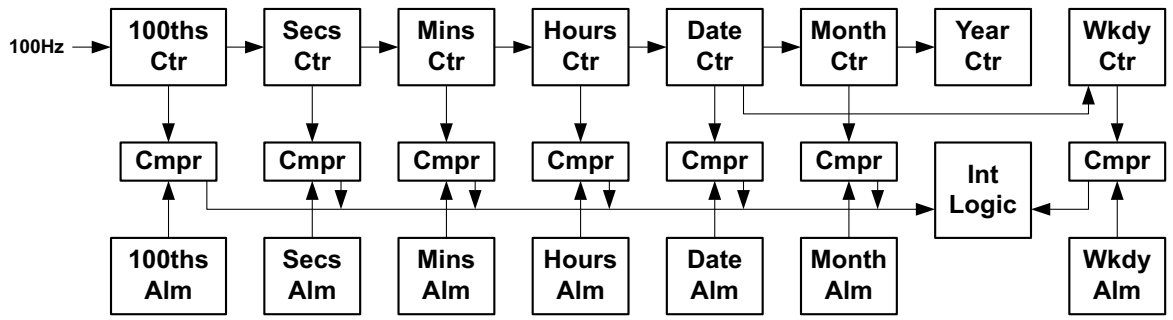

Figure 12. Block diagram for the Real Time Clock Module

8.1 Features

The Real Time Clock (RTC) Module, shown in Figure 12, provides an accurate means of maintaining real time. Key features are:

- 100^{th} of a second resolution
- Time is measured for the years between 1900 and 2199
- Automatic leap year calculation
- Hours are specified in 24 hour mode
- Alarm precise to 1/100 second
- Alarm interval every 100^{th} second, second, minute, hour, date, day of the week or month
- 100 Hz input clock taken from either the high accuracy XT Oscillator or the low power LFRC Oscillator

8.2 Functional Overview

Real time is held in a set of eight Calendar Counters, which hold the following counts of current units in BCD format:

- $1/100^{th}$ of a second (RTC_CTRLOW_CTR100)
- Second (RTC_CTRLOW_CTRSEC)
- Minute (RTC_CTRLOW_CTRMIN)
- Hour (RTC_CTRLOW_CTRHR)
- Date (RTC_CTRUP_CTRDATE)
- Day of the week (RTC_CTRUP_CTRWKDY)
- Month (RTC_CTRUP_CTRMO)
- Year (RTC_CTRUP_CTRYR)

The timer chain which generates the 100 Hz clock is reset to 0 whenever any of the Calendar Counter Registers is written. Since unintentional modification of the calendar counters is a serious problem, the RTC_RTCCTL_WRTC bit must be set in order to write any of the counters. Software may stop the clock to the calendar counters by setting the RTC_RTCCTL_RSTOP bit.

The RTC includes special logic to help ensure that the calendar counters may be read reliably, i.e., that no rollover has occurred. Two 32-bit reads are required to read the complete set of counters.

There are seven alarm register fields in the ALMLOW and ALMUP registers which may be used to generate an alarm interrupt at a specific time. These fields correspond to the above listed time calendar counters except for year which does not have an associated alarm. When all selected counters match their corresponding alarm register, the ALM interrupt flag is set.

By setting the Century Enable Bit (RTC_CTRUP_CEB), the Century Bit (RTC_CTRUP_CB) indicates the current century. A value of 0 indicates the 21st century, and a value of 1 indicates the 20th or 22nd century.

The Weekday Counter is a 3-bit counter which counts up to 6 and then resets to 0. It is the responsibility of software to assign particular days of the week to each counter value.

ERRATUM NOTICE

An intermittent bus hang may result from reading either the RTC's CTRUP or CTRLOW register in Low Power (LP) or High Performance (HP) mode. When the read access occurs close to the rising edge of the 100 Hz RTC clock, the read finite state machine (FSM) could potentially transition to an unknown state and get stuck there causing a bus hang. Only a reset returns the FSM back to normal.

See "ERR007: RTC: Intermittent bus hang by reading either the CTRUP or CTRLOW registers in LP or HP mode" in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

When the RTC_CTRUP_CEB bit is set to enable the Century bit (CB) to change, the CB toggles whenever and as long as the Year field (CTRYR) is 99. This happens not just on rollover from 99 to 00 but toggles randomly, which is (essentially) every RTC clock.

See "ERR028: RTC: CB field value is unpredictable when year = 99 and CEB = 1" in the *Apollo510 SoC / Apollo510B SoC Errata List*.

8.3 Additional Information

Please refer to the RTC registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

9. Counter/Timer (TIMER)

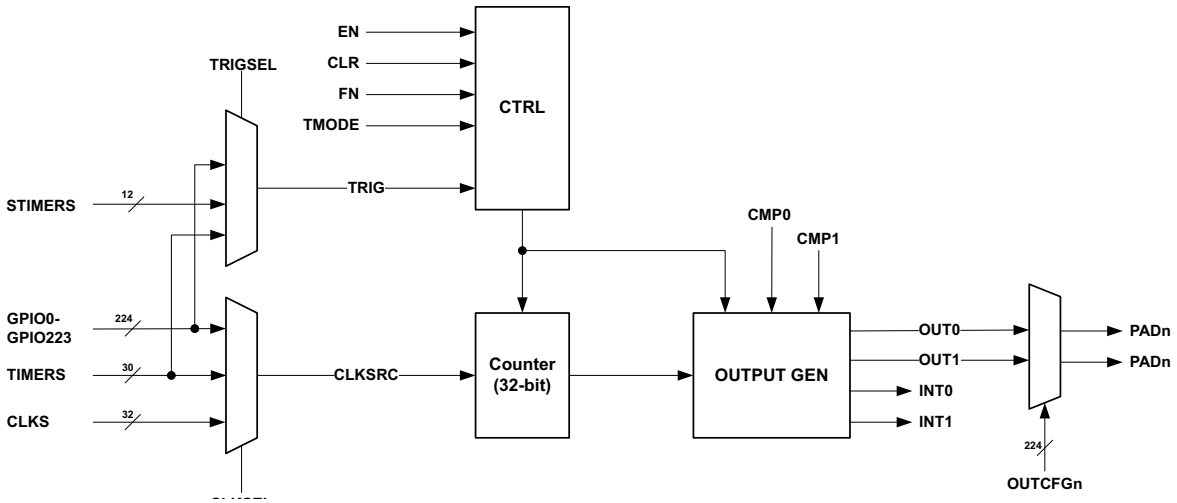

Figure 13. TIMER Block Diagram

NOTE

GPIOs available to be selected as timer triggers and clocks are dependent upon specific device and package pinout. Numbers shown are platform maximums.

9.1 Features

The Counter/Timer Module (TIMER) includes features shown in Figure 13 and listed below.

- Sixteen 32-bit binary up-counters used for simple waveform generation, interrupt sources, and counting applications.
- Each timer core has 2 interrupts, TMRnINT0/TMRnINT1 (Only for EDGE, UPCNT and PWM).
  - TMRnINT0 is generated when the value of the TIMER matches the TMRnCMP0 value.
  - TMRnINT1 is generated when the value of the TIMER matches the TMRnCMP1 value.
- For all modes CMP0 defines the end of a counter cycle and the timer will either stop or repeat. CMP1 is a secondary comparator.
- Each timer has two outputs which are controlled from CMP0 and CMP1 registers based on timer mode.
- Each timer is fully independent but can be linked by clocking one timer from another's output.
- Each timer offers several clock options including CLKGEN clocks, another timer output, or any GPIO input.
- Each timer has an interface to the GPIO module which allows any GPIO to be driven by any timer output and any GPIO to be used as a timer input.
- The start of a timer can optionally be triggered by a rising, falling or either edge of another timer output, an STIMER capture/compare event, or any GPIO input.
- Counter register value may be written directly.
- Either or both OUT0/OUT1 outputs of any timer can be inverted by using the POL0/POL1 bit.
- TMRnLMT register can be used to generate 1-255 repetitions of a waveform (0=unlimited).

9.2 Functional Overview

The Apollo510B SoC's Timer/Counter module includes sixteen Timer/Counters, one of which is shown in the Figure 13. This is in addition to a system timer as described in the System Timer chapter. Each Timer/Counter includes a very low power asynchronous 32-bit counter. Each Timer/Counter has external pin connections using any GPIO pads as outputs for each of the two comparators.

Timer functions include those listed in Table 11.

Table 11: Timer Modes

Mode	Outputs	Description/Uses
EDGE	OUT0 transitions when TIMERn = CMP0. OUT1 transitions when TIMERn = CMP1 (if CMP1 < CMP0).	Edge generation (0x1): TIMERn counts up from 0 to CMP0 and stops. A single edge is generated on OUT0 when TIMERn reaches CMP0. If CMP1 < CMP0, then a single edge is also generated on OUT1 when TIMERn reaches CMP1. If CMP0 < CMP1, then no edge is generated on OUT1 (because TIMERn never reaches CMP1). TMRnLMT: Has no effect in this mode. Trigger: Timer does not start until trigger occurs (if enabled). Subsequent triggers ignored.
UPCOUNT	OUT0 pulses for 1 clock cycle when TIMERn = CMP0; counter resets to 0; repeats per TMRnLMT setting. OUT1 pulses for 1 clock cycle when TIMERn = CMP1 (if CMP1 < CMP0).	Repeatable Up-counter (0x2): Counts up from zero to CMP0 and stops (TMRnLMT = 1), repeats N times (TMRnLMT = 2 - 255), or repeats indefinitely until TMRnEN is cleared (TMRnLMT = 0). Timer outputs will be a pulse of one source clock period on the output when the TIMER reaches the associated CMP value. If CMP1 < CMP0, then a single pulse of one source clock period is also generated on OUT1 when TIMERn reaches CMP1. If CMP0 < CMP1, then no pulse is generated on OUT1 (because TIMERn never reaches CMP1). Trigger: Timer does not start until trigger occurs (if enabled). Subsequent triggers ignored.

Table 11: Timer Modes

Mode	Outputs	Description/Uses
PWM	OUT0 transitions when TIMERn = CMP1, then transitions again when TIMERn = CMP0; repeats per TMRnLMT setting. OUT1 is the complement of OUT0.	Repeatable PWM (0x4): Counts up from zero to CMP0 and stops (TMRnLMT=1), repeats N times (TMRnLMT = 2 - 255), or repeats indefinitely (TMRnLMT = 0). CMP0 specifies the period and CMP1 specifies number of TIMERn counts for the initial phase of the output waveform. Trigger: Timer does not start until trigger occurs (if enabled). Subsequent triggers ignored.
SINGLEPATTERN	For TMRnLMT < 32 and for TIMERn count = 0 to TMRnLMT: OUT0 = CMP0[TIMERn]. OUT1 = CMP1[TIMERn]. For TMRnLMT between 32 and 63 (maximum 64-bit pattern consisting of CMP1:CMP0) and for TIMERn count = 0 to TMRnLMT: OUT0 = OUT1 = CMP1:CMP0[TIMERn]. OUT1 can be configured to be the complement of OUT0.	Single-run Pattern Generation (0xC): CMP0 and CMP1 are bit-shifted to form the output pattern on OUT0 and OUT1, or concatenation of CMP1:CMP0 is bit shifted to form the output pattern on both OUT0 and OUT1. The TIMER count is an up-counter that indexes into the bits of CMP0 (TIMER values from 1-31) and CMP1 (TIMER values 32-63). TMRnLMT value defines the length of the pattern minus 1 (0 = 1-bit pattern, 63 = 64-bit pattern). OUT1 is the same as OUT0, but can be inverted for motor control applications. INT0 is triggered when all TMRnLMT+1 bits have been streamed out. INT1 is triggered only when TMRnLMT is set to 31 and all 32 bits of CMP0 have been streamed out. Trigger: Timer does not start until trigger occurs (if enabled). After clearing and reconfiguring the timer for this mode, a subsequent trigger restarts the pattern replay.
REPEATPATTERN	For TMRnLMT < 32 and for TIMERn count = 0 to TMRnLMT: OUT0 = CMP0[TIMERn]. OUT1 = CMP1[TIMERn]. For TMRnLMT between 32 and 63 (maximum 64-bit pattern consisting of CMP1:CMP0) and for TIMERn count = 0 to TMRnLMT: OUT0 = OUT1 = CMP1:CMP0[TIMERn]. OUT1 can be configured to be the complement of OUT0.	Repeated Pattern Generation (0xD): CMP0 and CMP1 are bit-shifted to form the output pattern on OUT0 and OUT1 as described in SINGLEPATTERN mode with the exception that the timer repeats the pattern after TMRnLMT+1 bits have been streamed out, resetting TMRnLMT back to 0 after each iteration. Since TMRnLMT is used for the repeat pattern length, there is no option to repeat the pattern N times. The iterations repeat indefinitely until TIMERn is disabled.

NOTE

CMP0/CMP1 values should not be changed when the TIMER is running or else it will corrupt the counter.

Software should assert TMRnCLR each time before asserting TMRnEN. if this is not done, stale values will remain.

ERRATUM NOTICE

Since two timer clock cycles are required for the TMREN to be synchronized from the APB clock to the timer clock and another two timer clock cycles are required to synchronize the initial value, a total of four extra timer clock cycles must occur before the timer counter starts to increment, regardless of the clock selected for the timer. Subsequent clocking is not affected.

See “ERR045: TMR: Timer does not start counting until 4th clock tick” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

9.3 Additional Information

Please refer to the TIMER registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

10. System Timer (STIMER)

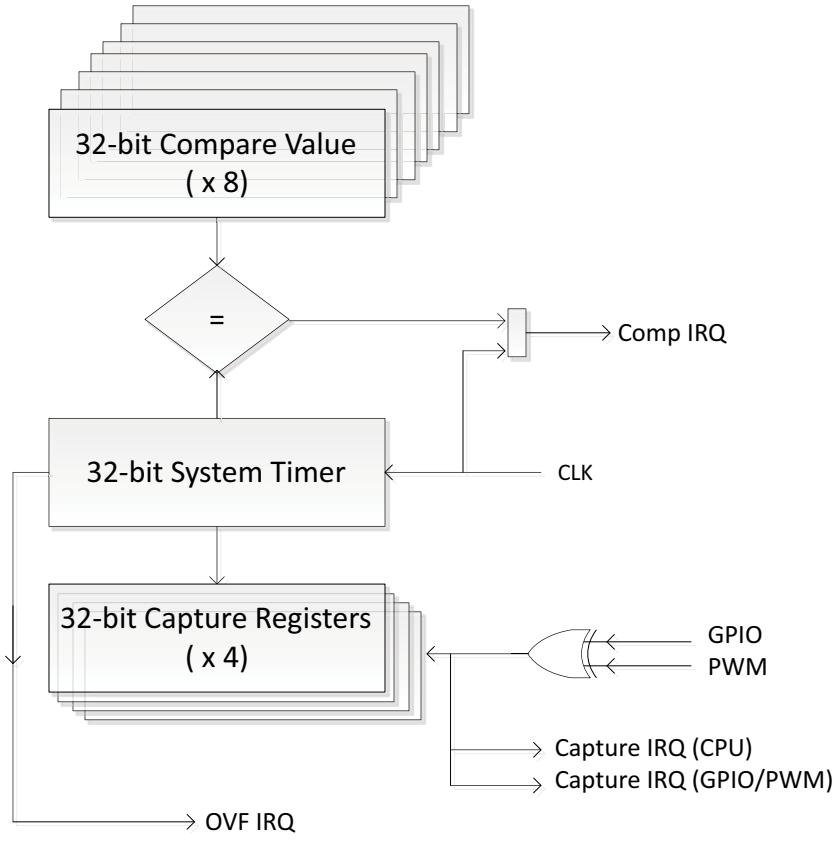

Figure 14. STIMER Block Diagram

10.1 Features

The System Timer (STIMER) includes features shown in Figure 14 and listed below.

- 32-bit binary counter used for RTOS scheduling decisions
- Eight 32-bit compare and interrupt registers to facilitate light weight scheduling (designs without RTOS)
- Accurate scheduling of comparator interrupts
- Only offsets from “NOW” written to comparator registers
- Maintains real time epoch for applications
- Overflow interrupt to allow firmware to keep the extended part (more than 32-bits) of real time epoch
- Time stamping hardware for multiple sensor streams (4 capture registers)
- Firmware handling of odd calculations such as Leap Second and events like surprise/legislated changes to the daylight savings time transition dates
- Firmware handling of 1024 versus 1000 scaling of real time conversions
- Only reset by POA (Power On Analog - system cold reset) so that it retains time across all POI and POR (system warm reset) events except full power cycles
- Contains three 32-bit NVRAM registers that are only reset by POA to maintain real time offset from epoch
- Programmable external GPIO trigger and/or PWM trigger on capture (required for sensor synchronization)

10.2 Functional Overview

The System Timer tracks the global synchronized counter. It can be used for RTOS scheduling and real-time system tracking. This timer is provided in addition to the other timer peripherals to enable software/firmware to have a simple, globally synchronized timer source.

The System Timer Module provides real time measurement for all task scheduling, sensor sample rate calibration, and tracking of real time and calendar maintenance.

ERRATUM NOTICE

Compare interrupts are delayed by one STIMER clock. Additionally, it takes two STIMER clock cycles for the write to an SCMPRn register (where n is 0 to 7 representing one of the STIMER Compare registers) to get operated on. These timing issues put constraints on the minimum value of delta that can be applied to SCMPRn, which is 4 STIMER clock cycles.

In addition, back-to-back writes to SCMPRn may not work reliably (i.e., take the last value) unless the application ensures not to write within two STIMER clock cycles of the previous one. As well, after writing to SCMPRn, the application needs to wait for at least three STIMER clock cycles before reading it back for the new value to be reflected.

It takes two STIMER clock cycles for the write to STCFG to take effect. This caused 2 extra cycles to add to the minimum delta.

It takes two STIMER clock cycles for the write to STCFG to take effect. This causes the need for 2 extra cycles to be added to the minimum delta.

See “ERR029: STIMER: Constraints on writing to SCMPRn registers and handling Compare interrupts” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

10.3 Additional Information

Please refer to the STIMER registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

11. Watchdog Timer (WDT)

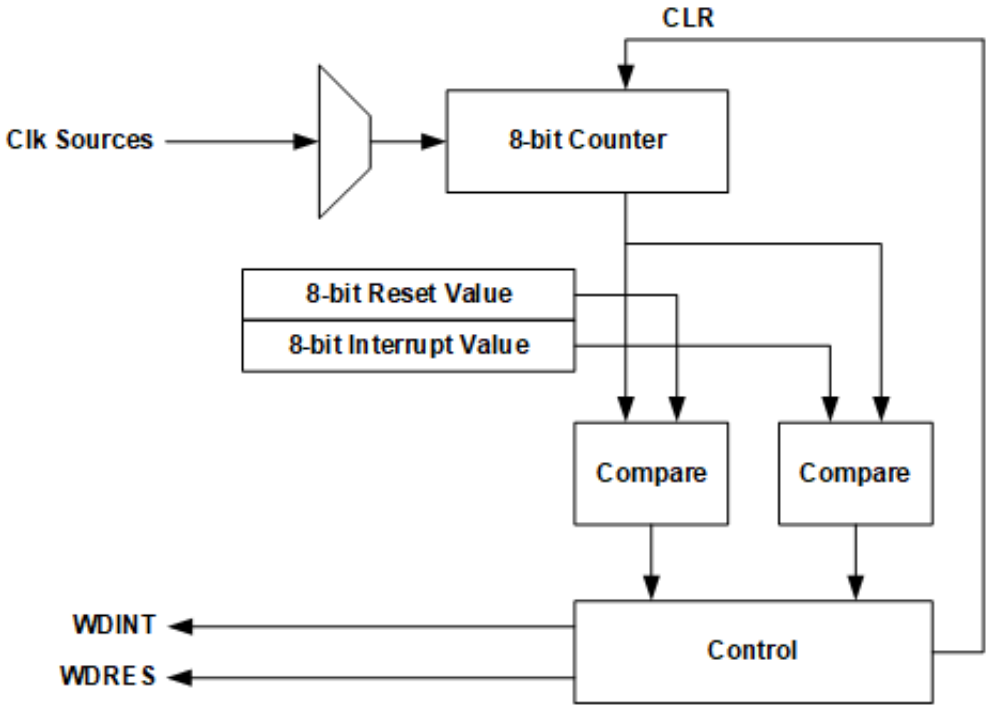

Figure 15. Watchdog Timer Block Diagram

11.1 Features

The Watchdog Timer (WDT) includes features shown in Figure 15 and listed below.

- Ensures software remains operational by initiating a reset if WDT times out
- May be clocked by one of four selectable prescalers of the LFRC clock
- May be locked to ensure software cannot disable its functionality
- Early warning may be implement via an interrupt

11.2 Functional Overview

The Watchdog Timer (WDT) is used to ensure that software is operational, by resetting the Apollo510B SoC if the WDT reaches a configurable value before being cleared by software. The WDT can be clocked by one of four selectable prescalers of the always active low-power LFRC clock, but is nominally clocked at 128 Hz. The WDT may be locked to ensure that software cannot disable its functionality, in which case the WDTCFG register cannot be accidentally reprogrammed. An interrupt can also be generated at a different counter value to implement an early warning function. Note: The RESEN bit in the WDTCFG register must be set and the WDREN bit in the RSTCFG register must be set to enable a watchdog timer reset condition.

11.3 Additional Information

Please refer to the WDT registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

12. Bluetooth Low Energy Controller (BLEC)

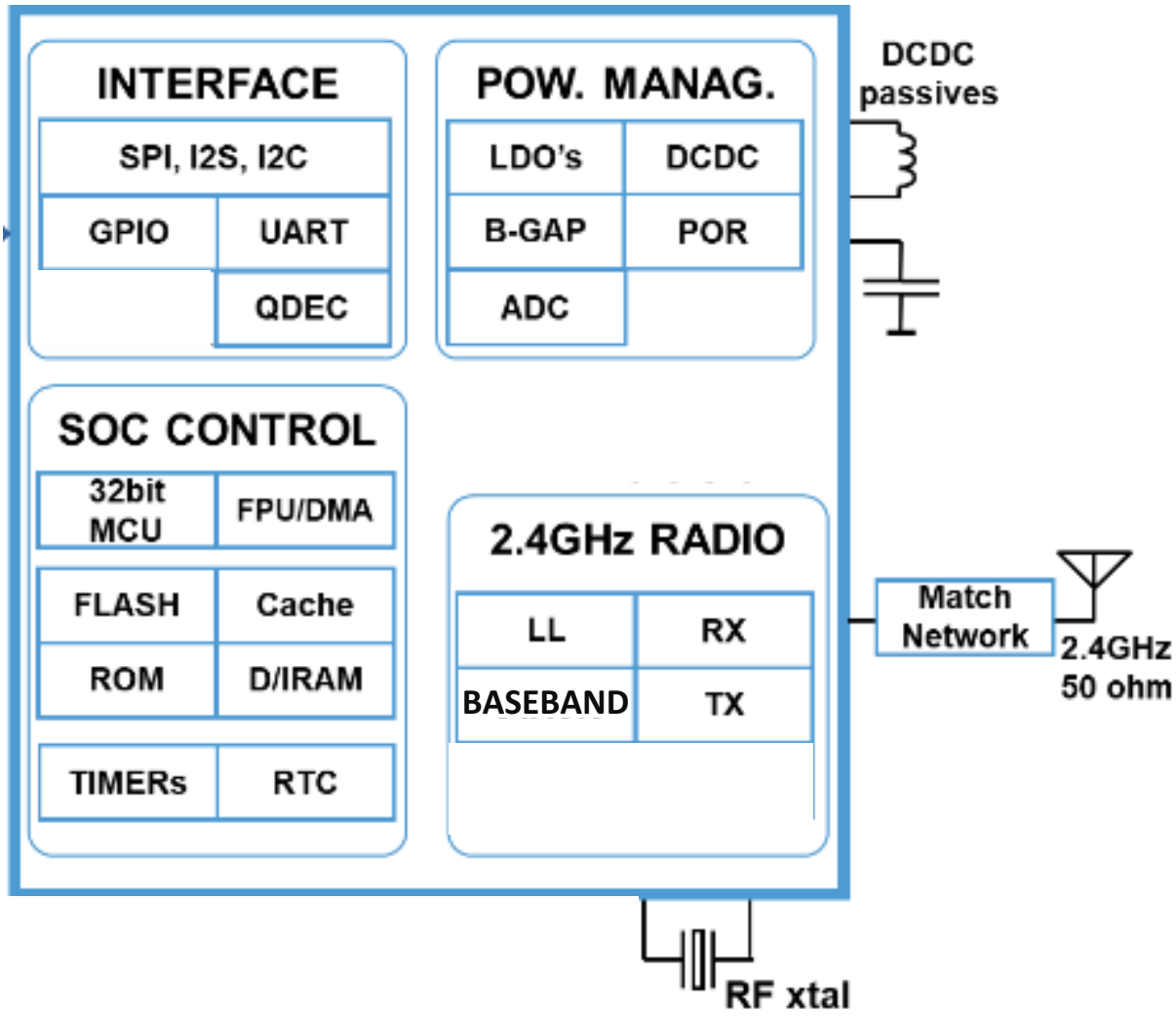

Figure 16. Block Diagram for Bluetooth Low Energy Controller

12.1 Features

The Bluetooth® 5.4 Low Energy Controller (BLEC) is represented by the block diagram shown in Figure 16. Key features of the Bluetooth Low Energy Controller include:

- Energy efficient, industry standard 32-bit MCU (co-processor) with DMA and Cache for minimum power consumption
  - DSP and FPU for signal processing
  - 64 kB ROM for secure boot
  - 512 kB flash memory for multi-protocol and applications
  - 64 kB data/instruction RAM, all retainable starting from 4 kB
  - 48 MHz MCU and memory-read speed
- Full Bluetooth 5.4 Implementation
  - High Data Rate (HDR) and Long Range (LR) support
  - Angle-of-Arrival and Angle-of-Departure (AOA/AOD) support

  - Isochronous channels for audio applications
  - SPI HCI Transport Layer
  - Up to 4 simultaneous connections
  - AES-128 Hardware Encryption/Decryption Engine
- Security Features
  - True Random Number Generator
  - Key Generation (ECC-P256)
  - Secure Key Containers
  - Secure Firmware Over-the-Air Updating (FOTA)
  - Secure lifecycle management
- Sophisticated Power Management System
  - Digital step up DCDC operation or inductor-less voltage multiplier mode
- Low Current Consumption
- High Performance RF
  - -94 / -97 / -103 dBm RX sensitivity for 2 Mbps / 1 Mbps / 125 kbps modes and 37 byte payload
  - -20 dBm to +6 dBm transmitter output power range
- Single ended antenna pin to be used with external matching network
- 48 MHz XTAL

12.2 Functional Overview

The Apollo510B SoC's highly integrated, ultra-low power BLEC offers execution on an efficient 32-bit co-processor from flash using a cache and DMA to optimize power. DSP and floating-point units can be utilized to implement advanced audio and tracking algorithms. A low-power SPI interface is used to communicate with the manager Apollo510 Cortex-M55 CPU.

Included in firmware is a fully featured Bluetooth 5.4 link layer, Host Controller Interface (HCI) and stack. All Bluetooth 5.4 features are available on the BLEC, including High Data Rate (HDR) and Long Range (LR) communication, Angle-of-Arrival (AOA) and Angle-of-Departure (AOD) for localization applications. Isochronous channels are also available for BLE LE audio applications.

The BLEC includes a sophisticated on-chip power management system supporting a wide range of voltage sources. All 64 kB of dedicated RAM memory can be kept in retention during sleep, or in 4 kB increments to optimize leakage. A stable, low-power sleep oscillator (RC or crystal based) minimizes power consumption while in a connected state or RTC operation. Current consumption is minimized for all modes of the application utilizing an efficient scheduler and memory manager.

The BLEC features a state-of-the-art 2.4GHz transceiver including a low-power receiver with excellent sensitivity/selectivity, and a programmable transmitter up to +6 dBm for optimized output power and current consumption.

The BLEC supports the following target applications:

- Bluetooth Controller Mode
  - Host connect to Apollo510 M55 controller via Host Controller Interface (HCI)
  - HCI implemented via SPI transport layer
  - Link layer implemented in flash
  - Up to 4 simultaneous connections supported
  - Long packet lengths (payload up to 255 bytes) supported

12.3 MCU and Digital Architecture

The 32-bit co-processor efficiently controls movement of data between the RF modem, memory, and the digital interfaces. The co-processor includes a digital signal-processing unit (DSP) and a floating-point unit

(FPU) for efficient implementation of signal processing algorithms. A CRC co-processor is also included for efficient verification of program memory. Memories are included for the following functions:

- ROM (64 kB) - used for the secure boot
- RAM (64 kB) - used for application development and for data
  - All 64 kB are retainable starting from a minimum of 4 kB.
  - All 64 kB can be used for data (DRAM).
  - Up to 36 kB can be used for instructions (IRAM) if not used for data.
- Flash (512 kB) - used for data, protocol, stack, profiles, and applications
  - The architecture includes an additional 32 kB of information area and trimming.
- Cache (2 kB) - used to optimize code access in flash

The memory architecture is divided into several different power domains for power consumption optimizations. When a memory is not being used, it can be switched off to reduce current consumption. During Bluetooth connected sleep mode the entire MCU subsystem can be shut off and only the power management system and required state retention memories (if any) need to be powered. The power management system will properly wakeup the MCU subsystem when it is needed. The RF modem is turned on and off as needed in order to minimize energy consumption.

12.4 Firmware Architecture

The firmware is implemented in a power efficient manner using a basic scheduler and memory manager. The BLEC implements a Bluetooth 5.4 compliant link layer at the bottom of the stack and accessed through the standard HCI interface. Bluetooth HCI commands are implemented and additionally some vendor specific commands are implemented. The link layer is designed to optimize power consumption in each role. The CPU is normally halted and is only activated when a task needs to be accomplished. When sleeping, states and connection information are properly stored in the retention memory and all other memories and peripherals are turned off. A low power timer is used to properly wakeup the system. The BLEC is certified by the Bluetooth SIG as Bluetooth Low Energy 5.4 Controller Subsystem.

12.5 RF Transceiver Overview

The RF transceiver exceeds the specifications and requirements of the Bluetooth 5.4 PHY specification. The main features of the RF transceiver are the following:

- Ultra-low-power
- Excellent RF performance: The transceiver offers -97 dBm sensitivity for 1 Mbps operation with 37 byte payload and a programmable output power range from -20 dBm to +6 dBm.
- Very high degree of integration requiring few external components

The RF transceiver consists of an analog/RF part and a digital part. The analog/RF part consists of the RX chain from LNA to ADC, the TX chain from DAC to the PA and the synthesizer subsystem that generates the LO frequency. The digital block consists of the modulator, demodulator, all calibration engines for radio optimization, timing sequencer for TX and RX and the register interface.

The Receiver chain has a low IF architecture. The Transmitter has a dual-point modulation architecture. The Synthesizer is a Frac-N PLL to generate the required LO frequency. All the blocks are optimized for lower current consumption. The RX and TX chains have multiple pre-burst calibrations that help achieve superior performance. The timing sequencer controls all pre-burst calibrations.

12.6 Power Management Overview

An advanced power management system is implemented on the BLEC. Key low-power circuits include a configurable and highly efficient DCDC converter, low noise bandgap references, low dropout regulators (LDOs), a high frequency RC oscillator for efficient MCU operation, and a high-accuracy, low-frequency, RC oscillator for sleep mode control. A sophisticated digital control system optimizes power consumption

and battery life in all conditions. Two power management configurations are possible, which are DCDC step-up and voltage multiplier. The configuration is automatically detected by the BLEC.

12.6.1 Supply Domains

The power management can have the following voltage supply configuration in both Step-up and Voltage Multiplier configurations.

General configuration:

- VIO is connected to VDDH which is powered by an external 1.8-2.2 V regulator/battery.
- VBAT2 and VCC are connected and can be supplied by either the VDDH regulator/battery or a separate 1.1-1.8 V regulator/battery.
- VBAT2/VCC must not exceed VIO.
- VBAT1 is the output voltage in either mode (DCDC output in step-up mode, switched capacitor (SC) multiplier output in voltage multiplier mode).

Step-up configuration:

- VIO is supplied by the VDDH regulator/battery.
- VBAT2 /VCC can be supplied by the VDDH regulator/battery or by a separate supply, but must be no higher than 1.9 V.
- The condition VIO ≥ VBAT2 must be fulfilled.
- The BLE_SW_DCDC pin is connected externally to a coil/capacitor voltage step-up which feeds an internal DCDC converter.
- The DCDC output is on the VBAT1 pad.

Voltage Multiplier configuration:

- VIO is supplied by the VDDH regulator/battery.
- VBAT2 /VCC can be supplied by the VDDH regulator/battery or by a separate supply to operate at a voltage below VDDH.
- The condition VIO ≥ VBAT2 must be fulfilled.
- The BLE_SW_DCDC pin is connected to ground.
- A voltage is produced by an internal voltage multiplier on the VBAT1 output, with a level of 1.9 V when VBAT2 is lower than 1.9 V, and is higher than 1.9 V when VBAT2 is higher than 1.9 V.

The supply domains in the device are summarized in the following table.

Table 12: Voltage Supply Requirements for each BLEC Power Domain

SUPPLY	Configuration	RANGE [V]	DESCRIPTION
VBAT2 / VCC	Step-up	1.1 – 1.9	External supply (can be same as VIO/VDDH or separate/ lower supply)
	Voltage Multiplier	1.1 – 2.2	
VIO	Step-up / Voltage Multiplier	Connected to VDDH (1.71 V - 2.2 V)	External supply same as VDDH; VIO must be ≥ VBAT2

12.6.2 Operating Modes

The BLEC has several modes of operation including several active, standby and sleep modes. Power consumption is optimized in each mode. Additionally, a deep sleep mode and a chip disable mode are provided for lowest non-active power consumption. Special circuitry is added to keep peak currents to the battery typically less than 12.5 mA when transmit power is set to 0 dBm or lower.

When the BLEC is active, two modes are possible. Active RC Mode is used with a high frequency (HF) RC oscillator for fast turn-on and turn-off performance. This can be used to service the peripherals, for example. When the RF is required, Active XTAL Mode is used with the high-accuracy crystal oscillator for channel frequency precision required by RF standards. The crystal oscillator takes longer to turn on than the RC oscillator and more energy is consumed when in use.

In Sleep Mode and Deep Sleep Mode, the sleep timer clock (device timing reference) can be connected either to the digitally calibrated low frequency (LF) RC oscillator or to the 32 kHz crystal oscillator on the Apollo510B SoC. If the 32 kHz crystal oscillator is used, the LF RC oscillator is switched to a relaxed setting with less supply current and less accuracy.

The LF RC runs all the time since it is used for the power management logic. It can run either in high power mode (HP) or low power mode (LP). The 32 kHz crystal option brings higher clock accuracy (about 10 times while periodically calibrated), which requires a shorter RF window in time for TDMA functions, hence lower average current.

Chip (BLEC) Disable Mode is provided as the lowest power mode possible with the battery voltage still applied to the IC but all functions are disabled. In this mode, digital outputs are put to a Hi-Z condition and the logic states are not maintained. The firmware is also reset.

The BLEC can be in one of the power modes shown in Table 13.

Table 13: BLEC Power Modes

Mode	VDD Operation	Clock CPU	Clock PML	Description
Active RC	LDO and DCDC active	HF RC 48MHz	LF RC HP 500 kHz	CPU enabled, logic power domains controlled by CPU
Active XTAL	LDO and DCDC active	HF XTAL 48MHz	LF RC HP 500 kHz	CPU enabled, logic power domains controlled by CPU RF controlled by CPU
Sleep RC	Sleep mode of power management	None	LF RC HP 250 kHz	CPU powered-down, VCC optionally charged (on by default) Selected DRAM in retention mode Optionally QDEC active
Sleep XTAL	Sleep mode of power management	None	LF RC LP 100 kHz	CPU powered-down, VCC optionally charged (on by default) Selected DRAM in retention mode Ultra-low power POR and PTAT
Deep Sleep RC	Sleep mode low-power of power management	None	LF RC LP 100 kHz	CPU powered-down, VCC not charged QDEC cannot be used Selected DRAM in retention mode Ultra-low power POR and PTAT
Deep Sleep XTAL	Sleep mode low-power of power management	None	LF RC LP 100 kHz	CPU powered-down, VCC not charged QDEC cannot be used Selected DRAM in retention mode Ultra-low power POR and PTAT
Chip disable	None	None	None	A special mode when device is not powered, ENABLE = 0

The diagram in Figure 17 shows the transition between the modes. When the BLEC is powered from the OFF Mode, enabled from Chip Disable Mode, or woken from Sleep Mode or Deep Sleep Mode, it enters the Active RC Mode. Active XTAL Mode is then entered if the radio is to be used to send or receive data or the HF crystal is required for other reasons. When no CPU tasks are pending, the CPU is halted. If there is enough time before the next pending CPU task Sleep Mode is entered.

Alternatively, Deep Sleep Mode can be entered by issuing the appropriate command. The BLEC can be woken up by the sleep timer (scheduled by the link-layer) or from pad activity such as an HCI command and enters active RC Mode as previously described. Chip Disable Mode is entered at any time by setting the ENABLE pin to logic 0.

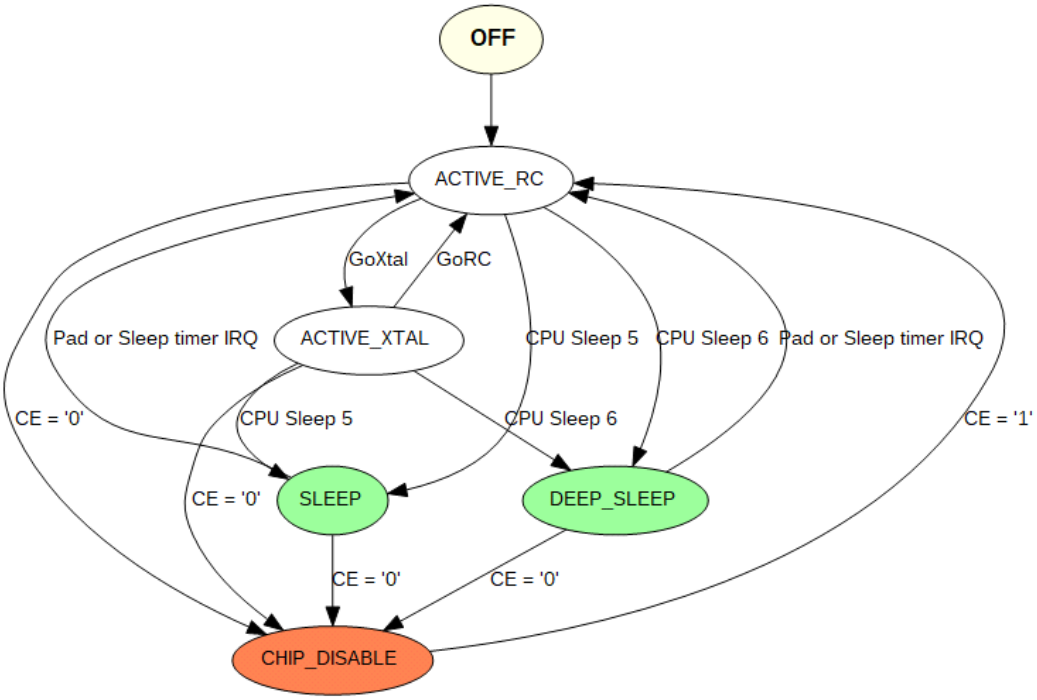

Figure 17. Power Modes Transition Diagram

The transition requirements from sleep modes to active modes are shown in Table 14. A transitions starts by a wake-up event (QDEC, pad or Sleep timer) and finishes when the device is ready to receive HCI commands.

The BLEC supports a SPI Subordinate (with flow control) HCI transport layer. The SPI HCI interface is powered-down in Sleep modes.

Table 14: Timing Characteristics When Changing Mode

From Mode	To Mode	Comments	Min	Typ	Max	Unit
Sleep	Active RC	Step-Up, Voltage multiplier Wake-up activated by HCI command To HCI ready signal VCC charging during Sleep is supposed to be charged	-	1340	-	µs
Active RC	Active XTAL	Depends on Q of HF XTAL XTAL start-up time is dominant	-	280	-	µs

12.7 Pin Description

The pins of the BLEC are described in Table 15. Analog pins include voltage supply pins, pins for crystal oscillators, and an antenna pin for the RF. Power is supplied through BLE_VBAT2, BLE_VIO and BLE_VCC for both power management configurations. Ground is connected to the various ground pins. Two pins are provided for the 48 MHz crystal (BLE_XIN, BLE_XOUT). The RF antenna is connected to the BLE_ANT pin.

The chip enable pin (BLE_ENABLE) is provided to achieve the lowest possible power consumption by the BLEC. The BLEC is not operational when this pin is low, and then it is initialized when this pin is raised high.

Table 15: BLEC Pin Description

Apollo510B Ball Number	Pin Name	Signal Type	Description
E1	BLE_VSS1	Supply	Die attach pad, connect to VSS on PCB
M1	BLE_AVDD_PA	Supply	Analog PA VDD (RF Supply)
N2	BLE_AVSS_RF	Supply	Analog ground
N1	BLE_ANT	RF	RF single ended antenna
M2	BLE_AVSS_ANT	Supply	Antenna analog ground
N6	BLE_XIN	XTAL	48 MHz XTAL
N7	BLE_XOUT	XTAL	48 MHz XTAL
E13	BLE_VIO	Supply	GPIO voltage level
A8	BLE_VBAT1	Output	DCDC / SC Multiplier output, internal BLE NVM supply
A7	BLE_SW_DCDC	DCDC	Coil; configuration detection
A6	BLE_VSS_DCDC	DCDC	Ground of DCDC switches
F1	BLE_VCC	Supply	Analog supply
G1	BLE_VBAT2	Supply	External battery voltage
E5	BLE_ENABLE	Digital	BLE Controller enable

NOTE

GPIO93 on ball E5 (BLE_ENABLE) must be terminated with a weak (~10 MΩ) pull-down resistor.

NOTE

Internally the 48 MHz XTAL clock is routed to the BLE Controller and is then divided by 4 to provide a 12 MHz clock to the GPIO15 pad which is used to source clocks to other modules on the Apollo510B SoC. The GPIO15 pin, ball J5, should not be externally connected and used on the PCB outside of testing purposes.

12.8 Additional Information

Please refer to the following BLEC-related sections for more information.

- “External Voltage Supplies” on page 205
- “Components for the BLE Controller” on page 210
- “Bluetooth Low Energy Controller Current Consumption” on page 216
- “Bluetooth Low Energy Controller” on page 231

13. General Purpose Input/Output (GPIO)

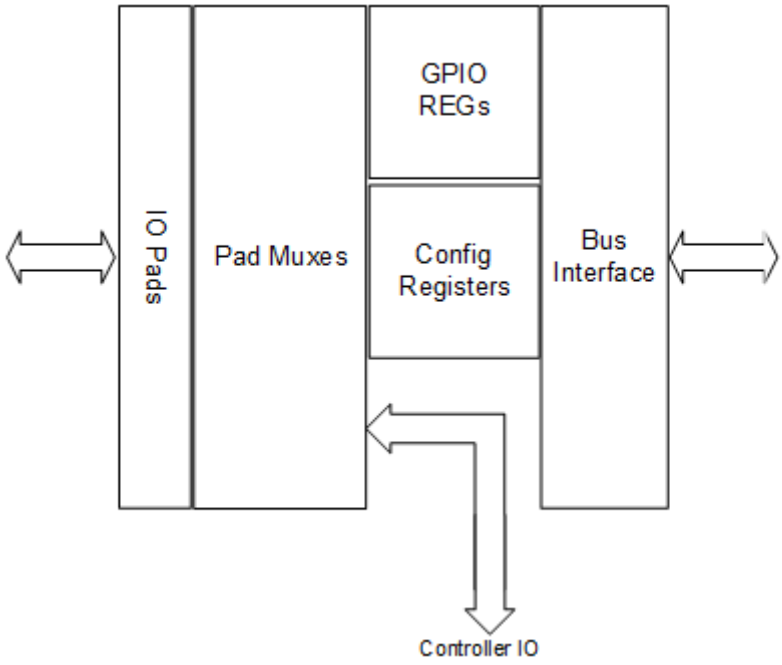

Figure 18. Block Diagram for the General Purpose Input/Output (GPIO) Module

13.1 Features

The GPIO module can be represented by the block diagram shown in Figure 18.

Key features include the following:

- Up to 96 GPIOs depending on derivative and package
- Five selectable I/O voltage domains depending on derivative and package (applies to set of GPIOs)
- 14 programmable GPIO interrupt groups
- Flexible GPIO Controls
  - 50 kΩ pull-down and 1.5 kΩ to 100 kΩ pull-up resistors
  - Multiple drive strengths
  - Multi-edge interrupts
  - Up to 11 function selects per GPIO
  - Grouped or masked interrupts
  - Configurable output drive mode (push-pull, open drain, tri-stated push-pull modes)

13.2 Functional Overview

The Apollo510B SoC's General Purpose I/O and Pad Configuration (GPIO) Module controls connections to up to 96 digital/analog pads. Each pad may be connected to a variety of module interface signals, with all pad input and output selection and control managed by the GPIO module. In addition, any pad may function as a general purpose input and/or output pad to be configured for a variety of external functions. Each GPIO may be configured to generate an interrupt when a transition occurs on the input.

For the Apollo510B SoC, any GPIO pad brought out to an external pin may be configured as a chip enable for any IOM or for the Display Controller. Pins available as chip enables for MSPI instances are as specified starting in Table 17. The pins available for specific MSPI chip enables are shown as function

selections with a “MNCEx_y” entry (orange), where x is the MSPI instance and y is the chip select number for that instance.

NOTE

For high-speed pads (GPIO37-GPIO45, 64-73, 142-146), there are 50 kΩ pull-up/pull-down options and 8 drive strength options (no slew rate).

NOTE

High-speed pads, those with MSPI0 or SWTRACE interface functionality, do not share the ability for the interface pin to be read by setting the pad’s INPEN field when configured as an output, as other GPIO pads do.

13.3 GPIO Interrupts

The Apollo510 architecture has GPIO interrupts in two groups: 0-7 and 8-15. 0-6 are groups of 32 GPIO interrupts, and 8-14 form the second group (GPIO interrupts 7 and 15 are reserved). Each interrupt is enabled, disabled, cleared or set with a standard set of interrupt registers GPIO_MCUN0INTnEN, GPIO_MCUN0INTnSTAT, GPIO_MCUN0INTnCLR and GPIO_MCUN0INTnSET, where n = 0 to 6 for GPIO pads 0 to 31, 32 to 63, 64 to 95, 96 to 127, 128 to 159, 160 to 191, and 192 to 223, respectively[1]. The N0 designation in these registers indicates that these are interrupt register set 0. A duplicate set of registers, with a designation N1, is available and these registers are similarly named GPIO_MCUN1INTnEN, GPIO_MCUN1INTnSTAT, GPIO_MCUN1INTnCLR and GPIO_MCUN1INTnSET. The purpose of this dual set of registers is to enable segregation of an interrupt, or a small set of interrupts, which may have higher importance and thus should be handled at a higher priority level and/or with minimal latency.

13.4 Pad Configuration Functions

Each GPIO on a Apollo510B SoC package can be configured as one of several functions according to the Pin Mapping tables starting with Table 17. Functions are grouped by module per the color coding shown in Table 19.

The I/O voltage source reference for each pad as listed in the “I/O Voltage” column of the Pin Mapping tables equates to the corresponding voltage supply shown in Table 16. See the Electricals “External Voltage Supplies” section for specified voltage range for each supply.

1. Bits used in the GPIO_MCUNmINTn registers depend on the pads used by the specific SoC derivative and package. See the available pads for each package in the Pin Mapping table later in this chapter.

Table 16: I/O Pin Voltage Source

I/O Voltage Reference	Voltage Supply	GPIO Powered	Modules Powered[1]
0	VDDH	GPIO0-14, 16-29, 31-36, 47-49, 83-88, 156-160	ADC, DC, I2S, IOM, IOS, SDIO, SWTRACE, UART, VCOMP, CLKOUT
1	VDDH1	GPIO142-147	SWTRACE
2	VDDH2	GPIO46, 50-51, 57, 95-104, 125-129, 134	DC, I2S, MSPI1, ADC, PDM, SDIO, SWTRACE, VCOMP
3	VDDH3	GPIO37-45, 64-73, 199-200	MSPI0, SWTRACE, ADC, UART, VCOMP, CLKOUT

1. All pads selected for any specific interface must be at the same voltage level.

NOTE

The Secure Bootloader (SBL) uses GPIO28 as the SWO output (1 Mbaud) to make bootup status/information available to the user. This pin is configured as an output and will toggle during bootup. Care should be taken by the user when connecting this pin to an external peripheral.

NOTE

The DPI-2 and DBI-Type B display interfaces are not offered on the Apollo510B SoC.

NOTE

The MOSI and SDAWIR3 functions of the half duplex IOS module are not pinned out on the Apollo510B SoC, and therefore the IOS module is not functional in either SPI or I^2C mode. The other function selections for the IOS module on Pads 11, 13 and 83 (SLx) shown in the Apollo510B SoC Pin Mapping tables should be disregarded and not selected for those pads.

The full duplex IOS modules, IOSFD0 and IOSFD1, with function selections on pads 0-4 (SLFDx) are fully functional for IOS SPI operation.

NOTE

GPIO15 on ball J5 and GPIO136 on ball J9 (not shown as an available GPIO in the below Pin Mapping table) are used internally as BLEC interface signals and should be regarded as reserved and not used.

Table 17: Apollo510B SoC Pin Mapping (Pg 1)

Pad	PADnFNCSEL											I/O Voltage
	0	1	2	3	4	5	6	7	9	10	12	
0	SWTRACECLK	SLFDSCK	-	GPIO0	UART0TX	UART1TX	CT0	NCE0	VCMPO	-	-	0
1	SWTRACE0	SLFDMOSI	SLFDWIR3	GPIO1	UART2TX	UART3TX	CT1	NCE1	VCMPO	SLFD1WIR3	-	0
2	SWTRACE1	SLFDMISO	TRIG1	GPIO2	UART0RX	UART1RX	CT2	NCE2	VCMPO	SLFD1MISO	-	0
3	SWTRACE2	SLFDnCE	SWO	GPIO3	UART2RX	UART3RX	CT3	NCE3	-	I2S1_SDIN	-	0
4	SWTRACE3	SLFDINT	32KHzXT	GPIO4	UART0RTS	UART1RTS	CT4	NCE4	I2S0_SDIN	SLFD1INT	-	0
5	M0SCL	M0SCK	I2S0_CLK	GPIO5	UART2RTS	UART3RTS	CT5	NCE5	-	-	-	0
6	M0SDAWIR3	M0MOSI	I2S0_DATA	GPIO6	UART0CTS	UART1CTS	CT6	NCE6	I2S0_SDOUT	-	-	0
7	M0MISO	TRIG0	I2S0_WS	GPIO7	UART2CTS	UART3CTS	CT7	NCE7	MNCE2_0	MNCE3_1	-	0
8	CMPRF1	TRIG1	-	GPIO8	M1SCL	M1SCK	CT8	NCE8	-	I2S1_CLK	-	0
9	CMPRF0	TRIG2	-	GPIO9	M1SDAWIR3	M1MOSI	CT9	NCE9	I2S1_DATA	I2S1_SDOUT	-	0
10	CMPIN0	TRIG3	MNCE0_0	GPIO10	M1MISO	MNCE2_0	CT10	NCE10	DISP_TE	I2S1_WS	MNCE2_1	0
11	CMPIN1	TRIG0	I2S0_CLK	GPIO11	UART2RX	UART3RX	CT11	NCE11	SLSCL	SLSCK	-	0
12	ADCSE7	TRIG1	I2S0_DATA	GPIO12	UART0TX	UART1TX	CT12	NCE12	CMPRF2	I2S0_SDOUT	-	0
13	ADCSE6	TRIG2	I2S0_WS	GPIO13	UART2TX	UART3TX	CT13	NCE13	SLnCE	-	-	0
14	ADCSE5	TRIG3	-	GPIO14	-	UART1RX	CT14	NCE14	-	I2S0_SDIN	-	0
16	ADCSE3	TRIG1	I2S1_CLK	GPIO16	-	UART1RTS	CT16	NCE16	-	-	-	0
17	ADCSE2	TRIG2	I2S1_DATA	GPIO17	-	UART3RTS	CT17	NCE17	I2S1_SDOUT	-	-	0
18	ADCSE1	-	I2S1_WS	GPIO18	UART0CTS	UART1CTS	CT18	NCE18	-	-	-	0
19	ADCSE0	-	-	GPIO19	UART2CTS	UART3CTS	CT19	NCE19	I2S1_SDIN	-	-	0
20	SWDCK	TRIG1	-	GPIO20	UART0TX	UART1TX	CT20	NCE20	-	-	-	0
21	SWDIO	TRIG2	-	GPIO21	UART0RX	UART1RX	CT21	NCE21	-	-	-	0
22	M7SCL	M7SCK	SWO	GPIO22	UART2TX	UART3TX	CT22	NCE22	VCMPO	-	-	0
23	M7SDAWIR3	M7MOSI	SWO	GPIO23	UART2RX	UART3RX	CT23	NCE23	VCMPO	-	-	0
24	M7MISO	TRIG3	SWO	GPIO24	UART0RTS	UART1RTS	CT24	NCE24	MNCE0_0	MNCE0_1	-	0
25	M2SCL	M2SCK	-	GPIO25	-	UART1TX	CT25	NCE25	-	-	-	0
26	M2SDAWIR3	M2MOSI	-	GPIO26	-	UART1RX	CT26	NCE26	VCMPO	-	-	0
27	M2MISO	TRIG0	MNCE3_0	GPIO27	-	UART1CTS	CT27	NCE27	-	-	-	0
28	SWO	VCMPO	-	GPIO28	UART2CTS	-	CT28	NCE28	-	-	-	0
29	TRIG0	VCMPO	-	GPIO29	UART1CTS	-	CT29	NCE29	-	-	-	0
31	M3SCL	M3SCK	I2S0_CLK	GPIO31	UART2TX	UART2CTS	CT31	NCE31	VCMPO	-	-	0
32	M3SDAWIR3	M3MOSI	I2S0_DATA	GPIO32	UART0RX	UART3CTS	CT32	NCE32	I2S0_SDOUT	-	-	0
33	M3MISO	CLKOUT	I2S0_WS	GPIO33	UART2RX	UART2RTS	CT33	NCE33	DISP_TE	MNCE1_0	-	0
34	M4SCL	M4SCK	SWO	GPIO34	UART0TX	UART2RX	CT34	NCE34	VCMPO	I2S1_CLK	-	0
35	M4SDAWIR3	M4MOSI	SWO	GPIO35	UART2TX	UART3TX	CT35	NCE35	I2S1_SDOUT	I2S1_DATA	-	0
36	M4MISO	TRIG0	MNCE3_0	GPIO36	UART0RX	UART1RX	CT36	NCE36	MNCE1_0	I2S1_WS	-	0
37	MSPI0_10	TRIG1	32KHzXT	GPIO37	UART2RX	UART3RX	CT37	NCE37	-	-	-	3
38	MSPI0_11	TRIG2	SWTRACECLK	GPIO38	UART0RTS	UART2RTS	CT38	NCE38	-	-	-	3
39	MSPI0_12	TRIG3	SWTRACE0	GPIO39	UART2RTS	UART3RTS	CT39	NCE39	-	-	-	3
40	MSPI0_13	TRIG1	SWTRACE1	GPIO40	UART0CTS	UART1CTS	CT40	NCE40	-	-	-	3
41	MSPI0_14	TRIG0	SWTRACE2	GPIO41	UART0TX	UART1TX	CT41	NCE41	SWO	-	-	3
42	MSPI0_15	TRIG2	SWTRACE3	GPIO42	UART2TX	UART3TX	CT42	NCE42	-	-	-	3
43	MSPI0_16	TRIG3	SWTRACECTL	GPIO43	UART0RX	UART1RX	CT43	NCE43	-	-	-	3
44	MSPI0_17	TRIG1	SWO	GPIO44	UART2RX	UART3RX	CT44	NCE44	VCMPO	-	-	3
45	MSPI0_18	TRIG2	32KHzXT	GPIO45	UART0TX	UART1TX	CT45	NCE45	-	-	-	3
46	-	TRIG3	CLKOUT_32M	GPIO46	UART2TX	UART3TX	CT46	NCE46	-	-	-	2
47	M5SCL	M5SCK	-	GPIO47	UART0RX	UART1RX	CT47	NCE47	-	I2S0_CLK	-	0
48	M5SDAWIR3	M5MOSI	-	GPIO48	UART2RX	UART3RX	CT48	NCE48	-	I2S0_WS	-	0
49	M5MISO	TRIG0	MNCE1_0	GPIO49	UART0RTS	UART1RTS	CT49	NCE49	I2S0_DATA	I2S0_SDOUT	MNCE1_1	0

Table 18: Apollo510B SoC Pin Mapping (Pg 2)

Pad	PADnFNCSEL											I/O Voltage
	0	1	2	3	4	5	6	7	9	10	12	
50	PDM0_CLK	TRIG0	SWTRACECLK	GPIO50	UART2RTS	UART3RTS	CT50	NCE50	DISP_TE	-	-	2
51	PDM0_DATA	TRIG1	SWTRACE0	GPIO51	UART0CTS	UART1CTS	CT51	NCE51	-	-	-	2
57	MNCE0_1	TRIG3	SWO	GPIO57	UART0RTS	UART1RTS	CT57	NCE57	I2S1_DATA	I2S1_SDOUT	-	2
64	MSPI0_0	32KHzXT	SWO	GPIO64	UART0RTS	UART2CTS	CT64	NCE64	I2S1_SDIN	-	-	3
65	MSPI0_1	32KHzXT	SWO	GPIO65	UART0CTS	UART1CTS	CT65	NCE65	-	-	-	3
66	MSPI0_2	CLKOUT	SWO	GPIO66	UART0TX	UART1TX	CT66	NCE66	-	-	-	3
67	MSPI0_3	CLKOUT	SWO	GPIO67	UART2TX	UART3TX	CT67	NCE67	-	-	-	3
68	MSPI0_4	SWO	-	GPIO68	UART0RX	UART1RX	CT68	NCE68	-	-	-	3
69	MSPI0_5	32KHzXT	SWO	GPIO69	UART2RX	UART3RX	CT69	NCE69	-	-	-	3
70	MSPI0_6	32KHzXT	SWTRACE0	GPIO70	UART0RTS	UART1RTS	CT70	NCE70	-	-	-	3
71	MSPI0_7	CLKOUT	SWTRACE1	GPIO71	UART0CTS	UART3RTS	CT71	NCE71	-	-	-	3
72	MSPI0_8	CLKOUT	SWTRACE2	GPIO72	UART0TX	UART1TX	CT72	NCE72	VCMPO	-	-	3
73	MSPI0_9	-	SWTRACE3	GPIO73	UART2TX	UART3TX	CT73	NCE73	-	-	-	3
83	MSPI2_9	32KHzXT	DISP_QSPI_D3	GPIO83	SWTRACE3	UART3RTS	CT83	NCE83	DISP_SPI_RST	SLMISO	-	0
84	-	-	SDIF0_DAT0	GPIO84	-	-	CT84	NCE84	-	-	-	0
85	-	-	SDIF0_DAT1	GPIO85	-	-	CT85	NCE85	-	-	-	0
86	-	-	SDIF0_DAT2	GPIO86	-	-	CT86	NCE86	-	-	-	0
87	-	-	SDIF0_DAT3	GPIO87	-	-	CT87	NCE87	DISP_TE	-	-	0
88	-	-	SDIF0_CLKOUT	GPIO88	-	-	CT88	NCE88	-	-	-	0
95	MSPI1_0	-	-	GPIO95	-	-	CT95	NCE95	I2S0_SDIN	-	-	2
96	MSPI1_1	-	-	GPIO96	-	-	CT96	NCE96	-	-	-	2
97	MSPI1_2	-	-	GPIO97	-	-	CT97	NCE97	-	-	-	2
98	MSPI1_3	-	-	GPIO98	-	-	CT98	NCE98	-	-	-	2
99	MSPI1_4	-	-	GPIO99	-	-	CT99	NCE99	-	-	-	2
100	MSPI1_5	DISP_QSPI_D0_OUT	DISP_QSPI_D0	GPIO100	DISP_SPI_SD	DISP_SPI_SDO	CT100	NCE100	I2S0_CLK	-	-	2
101	MSPI1_6	-	DISP_QSPI_D1	GPIO101	DISP_SPI_DCX	-	CT101	NCE101	I2S0_DATA	I2S0_SDOUT	-	2
102	MSPI1_7	-	DISP_QSPI_SCK	GPIO102	DISP_SPI_SCK	-	CT102	NCE102	I2S0_WS	-	-	2
103	MSPI1_8	-	DISP_QSPI_D2	GPIO103	DISP_SPI_SDI	-	CT103	NCE103	-	-	-	2
104	MSPI1_9	-	DISP_QSPI_D3	GPIO104	DISP_SPI_RST	-	CT104	NCE104	-	-	-	2
125	SDIF1_DAT0	-	-	GPIO125	-	-	CT125	NCE125	-	-	-	2
126	SDIF1_DAT1	-	-	GPIO126	-	-	CT126	NCE126	-	-	-	2
127	SDIF1_DAT2	-	-	GPIO127	-	-	CT127	NCE127	-	-	-	2
128	SDIF1_DAT3	-	-	GPIO128	-	-	CT128	NCE128	-	-	-	2
129	SDIF1_CLKOUT	-	-	GPIO129	-	-	CT129	NCE129	-	-	-	2
134	SDIF1_CMD	-	-	GPIO134	-	-	CT134	NCE134	-	-	-	2
142	SWTRACECLK	-	-	GPIO142	-	-	CT142	NCE142	-	-	-	1
143	SWTRACE0	-	-	GPIO143	-	-	CT143	NCE143	-	-	-	1
144	SWTRACE1	-	-	GPIO144	-	-	CT144	NCE144	-	-	-	1
145	SWTRACE2	-	-	GPIO145	-	-	CT145	NCE145	-	-	-	1
146	SWTRACE3	-	-	GPIO146	-	-	CT146	NCE146	-	-	-	1
147	SWTRACECTL	-	-	GPIO147	-	-	CT147	NCE147	MNCE0_0	MNCE3_0	-	1
156	SDIF0_DAT4	MNCE2_1	-	GPIO156	-	-	CT156	NCE156	-	-	-	0
157	SDIF0_DAT5	MNCE2_0	-	GPIO157	-	-	CT157	NCE157	-	-	-	0
158	SDIF0_DAT6	-	-	GPIO158	-	-	CT158	NCE158	-	-	-	0
159	SDIF0_DAT7	-	-	GPIO159	-	-	CT159	NCE159	-	-	-	0
160	SDIF0_CMD	-	-	GPIO160	-	-	CT160	NCE160	-	-	-	0
199	-	MNCE0_0	-	GPIO199	-	-	CT199	NCE199	-	-	-	3
200	-	MNCE0_1	MNCE0_0	GPIO200	-	-	CT200	NCE200	-	-	-	3

Table 19: Pad Function Color Code

Color/Symbol	Module
Analog	Analog Modules (ADC, VCOMP)
CLKOUT	Clock Output
CT	Counter/Timer
DBIB	MIPI DBI Type B Display Interface
Debug	Debug/Special
DISP	Display Interface
GPIO	General Purpose Input/Output
I2S0	Inter-IC Sound 0
I2S1	Inter-IC Sound 1
IOM0	I2C/SPI Manager 0
IOM1	I2C/SPI Manager 1
IOM2	I2C/SPI Manager 2
IOM3	I2C/SPI Manager 3
IOM4	I2C/SPI Manager 4
IOM5	I2C/SPI Manager 5
IOM6	I2C/SPI Manager 6
IOM7	I2C/SPI Manager 7
IOS	I2C/SPI Subordinate
MSPI0	Multi-bit Serial Peripheral Interface 0
MSPI1	Multi-bit Serial Peripheral Interface 1
MSPI2	Multi-bit Serial Peripheral Interface 2
MSPI3	Multi-bit Serial Peripheral Interface 3
NCE/MNCE	IOM/MSPI Chip Enables
PDM0	PDM-to-PCM Converter
SDIF0	Secure Digital Input Output Interface 0
SDIF1	Secure Digital Input Output Interface 1
UART0	Universal Asynchronous Receiver/Transmitter 0
UART1	Universal Asynchronous Receiver/Transmitter 1
UART2	Universal Asynchronous Receiver/Transmitter 2
UART3	Universal Asynchronous Receiver/Transmitter 3
USB	Universal Serial Bus

NOTE

IOM6, MSPI2 and MSPI3 are not pinned out on the Apollo510B SoC.

13.5 Additional Information

Please refer to the GPIO registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

14. General Purpose ADC and Temperature Sensor Module

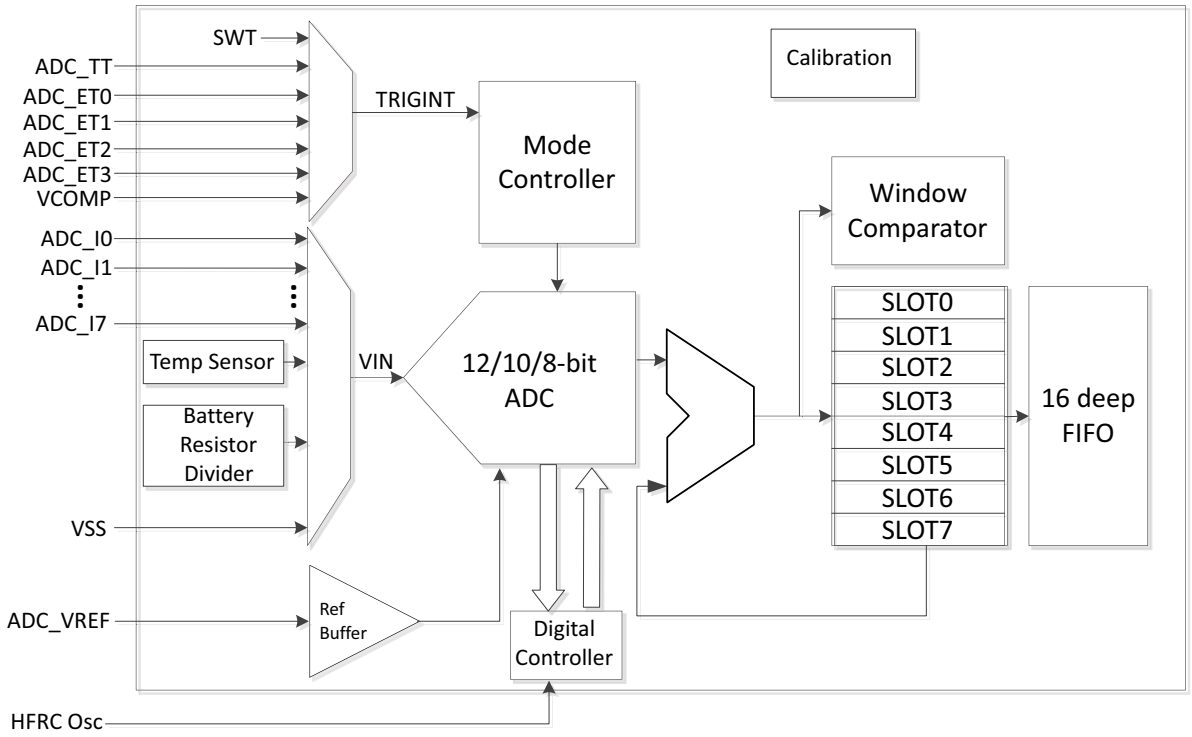

Figure 19. Block Diagram for ADC and Temperature Sensor

14.1 Features

The general purpose Analog-to-Digital Converter (ADC) and Temperature Sensor Module include a single-ended 12-bit multichannel Successive Approximation Register (SAR) ADC as shown in Figure 19.

Key features include:

- 11 user-selectable channels with sources including:
  - 8 single ended external pins
  - Internal voltage (VSS)
  - Voltage divider (battery)
  - Temperature sensor with ±3ºC accuracy
- Configurable automatic low power control between scans
- Optional Battery load enable for voltage divider measurement
- Single shot, repeating single shot, scan, and repeating scan modes
- Variable sample tracking time, configurable on per-slot basis
- User-selectable clock source for variable sampling rates
- Automatically accumulate and scale module for hardware averaging of samples
- A 16-entry FIFO and DMA capability for storing measurement results and maximizing MCU sleep time
- Supports ping-pong DMA jobs
- Window comparator for monitoring excursions of voltage into or out of user-selectable thresholds
- Up to 2.8 MS/s effective continuous, multi-slot sampling rate (at 8-bit resolution)
- Interrupts for FIFO full, FIFO 75% full, Scan Complete, Conversion Complete, Window Incursion, Window Excursion, and various DMA-related notifications

14.2 Functional Overview

The Apollo510B SoC integrates a 12-bit successive approximation Analog to Digital Converter (ADC) block for sensing both internal and external voltages. The block provides eight separately managed conversion requests, called slots which are serially sequenced. The result of each conversion requests is delivered to a 16 deep FIFO. Firmware can utilize various interrupt notifications to determine when to collect the sampled data from the FIFO or from a buffer written by DMA. This block is extremely effective at automatically managing its power states and its clock sources.

The ADC supports one internal reference source used for the analog to digital conversion step. The reference voltage is 1.19 V and is not user settable. ADC input voltages > 1.19 V exceed the ADC range and return full scale code, but will not damage ADC inputs.

DMA jobs may be ping-pong processed to allow software to pre-process and/or post-process one DMA job while hardware is processing another DMA job.

14.3 Voltage Divider and Switchable Battery Load

The Apollo510B SoC's ADC includes a switchable voltage divider that enables the ADC to measure the input voltage to the VDD rail. In most systems this will be the battery voltage applied to the SoC. The voltage divider is only switched on when one of the active slots is selecting analog mux channel 9. That is only when the mode controller is ultimately triggered and powers up the ADC block for a conversion scan of all active slots. Otherwise, the voltage divider is turned off.

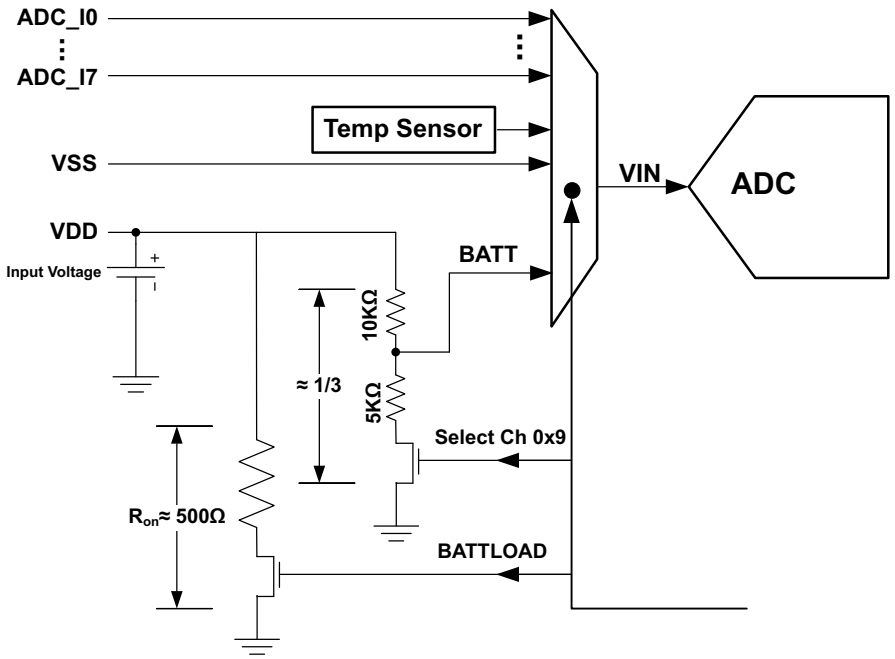

Figure 20. Switchable Battery Load

The switchable load resistor is enabled by the BATTLOAD bit as shown in the ADCBATTLOAD Register of the MCUCTRL Registers.This feature is used to help estimate the health of the battery chemistry by estimating the internal resistance of the battery.

14.4 Additional Information

Please refer to the ADC registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

15. Voltage Comparator (VCOMP)

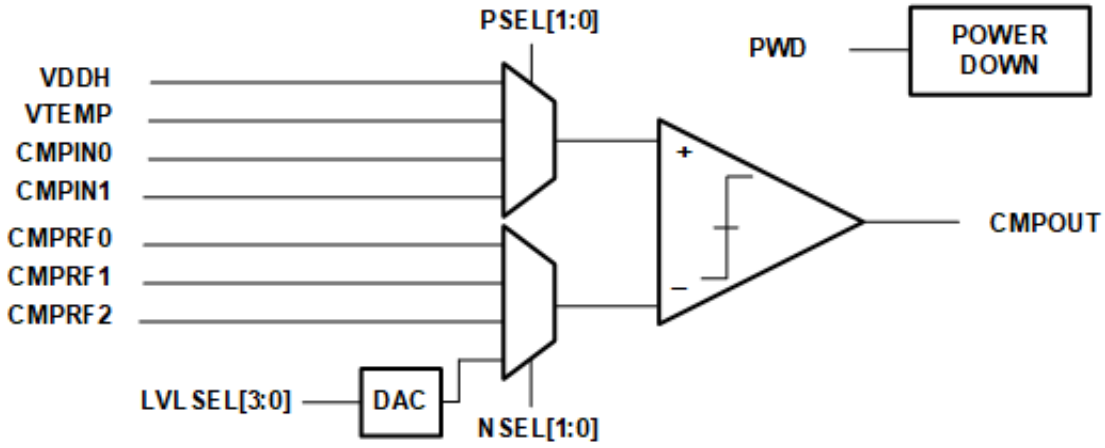

Figure 21. Voltage Comparator Block Diagram

15.1 Features

The Voltage Comparator (VCOMP) includes features shown in Figure 21 and listed below.

- Measures a user-selectable voltage
- Multiple options for input and reference voltages
- Provides interrupt and software access to comparator output
- Can generate an interrupt when monitored voltage rises above or drops below a user-configurable threshold
- Monitored voltage may be any of:
  - Supply voltage (VDDH)
  - The PTAT voltage from the temperature sensor (VTEMP)
  - One of two external voltage channels - CMPIN0, CMPIN1
- Reference voltage may be any of:
  - Three external voltage channels - CMPRF0, CMPRF1, CMPRF2
  - Internally generated reference voltage (VREFINT) tunable using on-chip DAC with level select signal LVLSEL[3:0].
- VCOMPOUT output remains high while the positive input is above reference input and transitions low when the positive input falls below the reference input
- CMPOUT output directly accessible via register read
- Two settable interrupts
  - OUTHI can trigger if VCOMPOUT transitions high
  - OUTLOW can trigger if VCOMPOUT transitions low

15.2 Functional Overview

The Voltage Comparator Module in the Apollo510B SoC measures a user-selectable voltage at all times. It provides interrupt and software access to the comparator output with multiple options for input and reference voltages. It can be configured to generate an interrupt when the monitored voltage rises above a user-configurable threshold or when the monitored voltage drops below a user-configurable threshold.

The voltage to be monitored is selected by programming the comparator's positive terminal signal, CFG_PSEL[1:0] and may be any of:

1. The supply voltage (VDDH)

2. The PTAT voltage from the temperature sensor (VTEMP)
3. Two external voltage channels selected by a GPIO function (CMPIN0 and CMPIN1)

The reference voltage is selected by programming the comparator's negative terminal, CFG_NSEL[1:0] and may be either of:

1. Three external voltage channels selected by a GPIO function (CMPRF0, CMPRF1, CMPRF2)
2. The internally generated reference voltage selected by CFG_LVLSEL

The internal reference voltage is tuned using an on-chip DAC with level select signal LVLSEL[3:0]. When using external inputs or reference inputs, the associated pads must be configured using the GPIO function selects explained in the GPIO document section.

The Voltage Comparator CMPOUT output will remain high while the voltage at the positive input is above the voltage at reference input. The CMPOUT output will transition low when the voltage at the positive input to the comparator falls below the reference input taking into account hysteresis. The CMPOUT output is directly accessible by software by reading the CMPOUT field in the status register. The OUTHI interrupt will be set if enabled and the CMPOUT transitions high or if it is high at the time the interrupt is enabled. Similarly, the OUTLOW interrupt will be set if enabled and the CMPOUT output transitions low or if it is low at the time the interrupt is enabled.

15.3 Additional Information

Please refer to the VCOMP registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

16. Multi-bit Serial Peripheral Interface (MSPI)

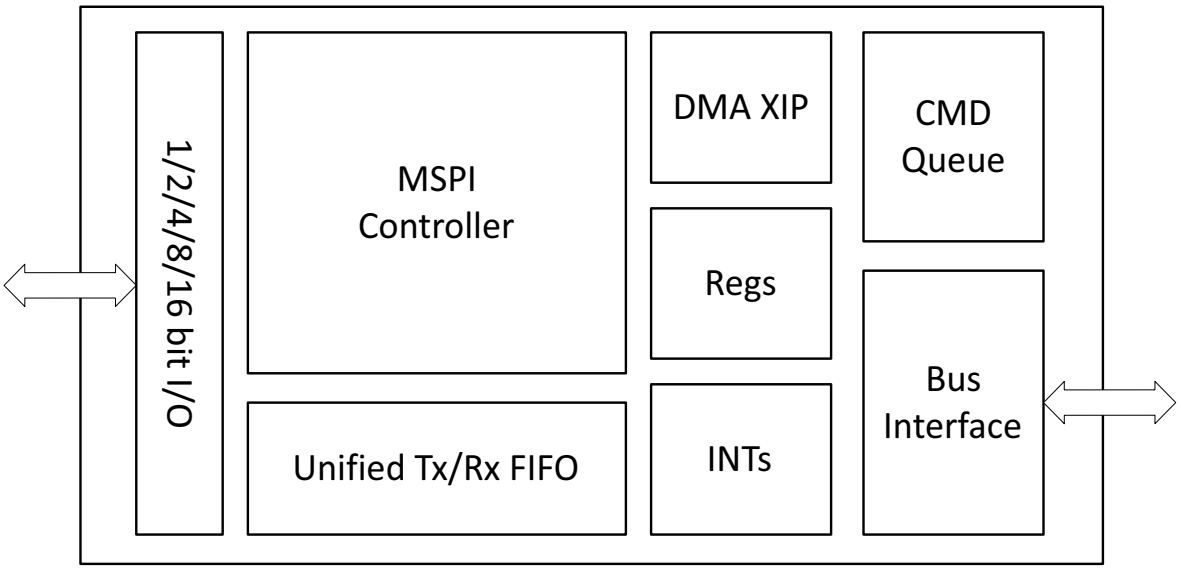

Figure 22. MSPI Module Block Diagram

16.1 Features

Each of the Multi-bit Serial Peripheral Interface (MSPI) modules includes the major functional blocks as shown in Figure 22.

Key MSPI features include:

- 1x HexSPI controller
  - 1/2/4/8/16-bit SPI interface
  - SDR/DDR modes
  - Up to 125 MT/s SDR and 250 MT/s DDR throughput on MSPI0
  - Supports up to 256 MB devices on MSPI0
  - Interoperability with JESD-251 rev C-compliant devices
- 1x OctalSPI controller
  - 1/2/4/8-bit SPI interface
  - SDR/DDR modes
  - Up to 96 MT/s SDR and DDR throughput on MSPI1
  - Supports up to 64 MB devices
- 9-bit command mode support
- XiP support
- DMA with peripheral-to-memory and peripheral-to-peripheral support
- Command Queue support
- All four SPI CPOL/CPHA modes supported

NOTE
There is no full-duplex operation in 4-wire SPI mode of an MSPI on the Apollo510B SoC. As well, MSPI 4-wire mode does not support reads of an arbitrary length, instead it always reads multiples of 4.

Please refer to the MSPI registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

ERRATUM NOTICE

An explicit memory access (read, write and instruction fetch) or a data and instruction pre-fetch to a memory that is in a powered down or unclocked state may cause a system hang. If there is dirty data in the data cache, a cacheable access to another data region may cause a cache-line eviction when attempting to write back the cache line to memory. If that memory is powered down, then a system hang may occur.

See “ERR009: MSPI: Accessing some powered-down/unclocked memory interfaces can cause system hangs” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

When an MSPI clock source lower than or equal to 48 MHz is selected, not all MSPI peripheral accesses can be guaranteed. Thus, for MSPI0, only HFRC_96MHz, HRFC2_125MHz, HFRC_192MHz or HRFC2_250MHz may be selected in the CLKGEN_MSPIIOCLKCTRL_MSPInIOCLKSEL register fields. For MSPI1, only HFRC_96MHz or HFRC_192MHz may be selected.

See “ERR016: MSPI: Peripheral accesses not guaranteed when the clock source <= 48 MHz” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

A DMA transfer which has a start address near the upper boundary of a memory block and the transfer extends into the next memory block, a device hang occurs. The root cause is that a DMA burst is fixed to 0, so the DMA address will not change when it crosses the memory boundary.

This condition applies for several boundaries, which are the DTCM - SRAM0, SRAM0 - SRAM1 and SRAM1 - SRAM2 boundaries. The address ranges for the affected memory spaces are the following for the Apollo510/Apollo510B devices:

- DTCM: 0x20000000 - 0x2007FFFF
- SSRAM0: 0x20080000 - 0x2017FFFF
- SSRAM1: 0x20180000 - 0x2027FFFF
- SSRAM2: 0x20280000 - 0x2037FFFF

In addition, this susceptibility to device hang occurs when a DMA transfer crosses a 4 kB boundary in DTCM.

See “ERR018: MSPI: Crossing a memory boundary during DMA transfer causes device hang” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

Behavior of the upper data lines (IO2 and IO3) during the instruction phase of mixed-mode (1-1-4 or 1-4-4) transfers is preventing IO3 to function properly as the nHOLD signal, as is done on certain NAND devices. When nHOLD is pulled low at the start of the transaction and despite pull-ups present, it causes the chip to ignore all other signals. The SoC should leave the upper data lines floating during the instruction phase of mixed-mode transfers.

See “ERR019: MSPI: Upper data lines are pulled low instead of staying in high impedance mode” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

A glitch occurs on the D0 line between address and data in mixed mode D4, or 1-1-4. The glitch is observed only during write operation in 1-1-4 mode and its occurrence may cause data write failures. Read operation is not affected and therefore it does not pose a problem for XIP/XIPMM reads

See “ERR020: MSPI: Mixed Mode 1-1-4 does not work as expected” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

16.2 Functional Overview

The Apollo510B SoC integrates two MSPI modules which can be used to connect to external memory mapped devices. One MSPI controller supports DDR operation up to 125 MHz and can transfer in serial, dual, quad, octal and hex (x16) modes. The other controller supports DDR operation up to 48 MHz (96 MT/s) and can transfer in serial, dual, quad, and octal modes.

Each MSPI module has a unified 32-entry FIFO (32 bits wide) that is used for both transmit and receive data. To ensure that transactions are not dropped because of system or software latency, the MSPI controller pauses the clock (and thus the transfer on the bus) if the TX FIFO empties or the RX FIFO fills during an operation. It automatically resumes once the FIFO condition has cleared.

MSPI transfers generally consist of transmitting a 1-byte instruction, a 1-byte to 4-byte address (optional), and 1 byte to 16 MB of write or read data (with an optional number of turnaround clock cycles between address0 and RX data, as well as an optional number of turnaround clock cycles between address and RX data).

Most devices use the same number of pins to transmit instruction, address, and data (for example, all are quad or all are serial). However, some devices utilize mixed transfer modes to implement parallel data transfer on top of an inherently serial command structure. These devices are supported by the MSPI by utilizing the XIPMIXEDn configuration, which forces the MSPI to switch into dual or quad modes of operation for a portion of the transfer.

To utilize mixed mode transfers, the MSPI's normal configuration should be set to match the device's transfer characteristics for commands (usually serial), which allows the MSPI to communicate with the device in its native mode. The XIPMIXEDn field in the DEVnXIP register should then be programmed to indicate whether the data phase (and optionally address phase) of the command should be performed in dual or quad mode. The MSPI will automatically switch to the new mode after transmitting the command to the device for all DMA and XIP operations.

The MSPIn modules of the Apollo510B SoC are directly attached to the system AXI bus and are memory mapped. For example, data read/write accesses and instruction accesses (referred to as XIP for eXecute In Place) for MSPI0 are via the 0x60000000 - 0x6FFFFFFF (non-secure) address range. Each MSPIn device register space has provisions to support two independent devices, however this is not currently supported in the Apollo510B SoC. Only the DEV0* registers which configure the first device are valid. The device selected for the transaction can be specified in the PIODEV field (for PIO operations), DMADEV field (for DMA operations), or by the address range for memory-mapped operations. Each MSPIn device supports the configuration of two external devices which can be mapped within the MSPIn's memory region using the DEVnAXI configuration registers.

The MSPI modules of the Apollo510B SoC are memory mapped as follow:

- MSPI0: 0x60000000 - 0x6FFFFFFF
- MSPI1: 0x80000000 - 0x83FFFFFF

Access to the MSPI devices is as follows:

- Cortex-M55 instruction accesses to XIP space are read-only and handled through the Cortex-M55 I-cache (which must be enabled).
- Cortex-M55 data accesses to XIP space are read/write and handled through the Cortex-M55 D-cache (which must be enabled). The GFX and the display controller access data directly through the XIP interface.
- PIO: The SoC can initiate PIO-based operations to manage basic device configuration and other low-level manual operations.
- DMA: MSPI module can autonomously transfer data between the external device and internal memory or NVM.

Note that XIP and DMA do not enforce hardware coherency, so the cache must be managed by software when performing DMA or XIP operations to regions that contain code which may be cached. In each of these modes, the MSPI module also supports data scrambling on accesses within a programmable address range having boundaries aligned to 64 kB address boundaries. Once the external devices are configured, the MSPI supports a simple DMA model, where software can program the internal (SRAM or flash) address and external device address, transfer direction, and transfer size. Once enabled, the MSPI DMA interface will move data between the system and external flash and interrupt when complete. The MSPI also supports a higher-level command queuing (CQ) protocol, where software can construct a buffer of operations in SRAM (or internal flash memory) and the MSPI will execute the series of operations autonomously. The MSPI can also power itself down at the end of DMA or CQ operations.

While each MSPI module can be used as a generic SPI device (with two chip enables), in addition to supporting serial, dual, and quad displays, it is primarily designed to support serial NAND/NOR flash memory or PSRAM memory. It is intended to be used to initialize the external memory devices and then be configured with the parameters matching the flash access characteristics. Devices can then be accessed through DMA or XIP operations with minimal software overhead.

The DMA address range has been expanded to support the larger flash and SRAM sizes, and the MSPI DMA/transfer length has been expanded to 24 bits to allow burst transactions of more than 64 kB.

The MSPI module also contains:

- A DEVnBOUNDARYn register which can be programmed to break a single long MSPI DMA into smaller transfers at periodic intervals (DMATIMELIMITn bit field).
- Address boundaries (DMABOUNDn bit field) to provide breaks in DMA for XIP traffic and satisfy the page crossing and maximum refresh times of external PSRAM devices.

NOTE

The DMATIMELIMITn is approximate since the MSPI will continue transmitting to the next 32-bit word boundary before disengaging on the bus. For this reason, a device requiring an 8 µs maximum transmission time should be set to have about a 7.5 µs time limit.

NOTE

For DMABOUNDn to properly break at a page crossing, the DMADEVADDR for the transfer must be 4-byte aligned. If a non-aligned starting edge of the transfer is required, software should manually break the transaction into two parts, with the first transaction ending on the page boundary. Failure to observe this limitation will result in data loss as the MSPIn may write 1-3 additional bytes past the boundary which will either wrap within the device's page or be discarded by the device.

16.2.1 Configuring MSPI as a DMA Target and a DMA Client Concurrently

A DMA deadlock may occur when there is heavy traffic of concurrent DMA accesses such as when the MSPI is used as both a “DMA client”, where MSPI is sourcing or sinking data through the DMA, and a “DMA target”, where MSPI is a memory-mapped source or destination for other peripheral DMA. For example, a situation may exist when the ADC is targeting a memory device through the MSPI XIPMM aperture as a the ADC sample “DMA target” at the same time that the MSPI is using DMA itself to target SSRAM or TCM. This condition may result in a DMA deadlock due to a circular dependency when the APBDMA-AXI, MSPI-AXI, MSPI-XIPDMA and APBDMA-ARBITOR states are blocking or waiting for DMA resources.

To avoid this potential problem, software should control the DMA’s configuration to alternate between MSPI as a DMA client and as a DMA target so as not to allow overlap of these DMA accesses. Note that there should not be a threat of this deadlock situation when short CPU accesses such as XIP or memory mapped MSPI are occurring, due to the location of arbitration against DMA traffic.

16.3 Pad Configuration and Enables

For the Apollo510B SoC, both of the MSPI modules, MSPI0 and MSPI1, support serial, dual, quad or octal mode, while MSPI0 additionally supports hex mode. Each MSPI module supports the external connections shown in the following tables. The columns to the right indicate which bits are used in each configuration (S=serial, D=dual, Q=quad, O=octal with CE#). Within the table, O=output pin, I=input pin, and X=bidirectional.

> NOTE
>
> Maximum clock speed of a specific SPI interface is dependent on the timing characterization of the chip enable (CEn) for each MSPI instance. Those speeds are specified in the Electricals chapter.

Table 20: MSPI0 Pin Muxing (Serial, Dual, Quad, Octal, Hex)

Pin Name	Direction	GPIO	Description	S0	S1	D0	D1	Q0	Q1	O0	O1	H0	H1
MSPI0.0	Output	10, 24, 147, 199. 200	MSPI0 CE0	O		O		O		O		O	
MSPI0.1	Output	24, 57, 200	MSPI0 CE1		O		O		O		O		O
MSPI0_18	Input/Output	45	MSPI0 DM1/DQS1 (Hex)									X	X
MSPI0_17	Input/Output	44	MSPI0 Data Bit 15									X	X
MSPI0_16	Input/Output	43	MSPI0 Data Bit 14									X	X
MSPI0_15	Input/Output	42	MSPI0 Data Bit 13									X	X
MSPI0_14	Input/Output	41	MSPI0 Data Bit 12									X	X
MSPI0_13	Input/Output	40	MSPI0 Data Bit 11									X	X
MSPI0_12	Input/Output	39	MSPI0 Data Bit 10									X	X
MSPI0_11	Input/Output	38	MSPI0 Data Bit 9									X	X
MSPI0_10	Input/Output	37	MSPI0 Data Bit 8									X	X
MSPI0_9	Input/Output	73	MSPI0 DM0/DQS0 (Octal/Hex)							X	X	X	X
MSPI0_8	Output	72	MSPI0 CLK	O	O	O	O	O	O	O	O	O	O
MSPI0_7	Input/Output	71	MSPI0 Data Bit 7						X	X	X	X	X
MSPI0_6	Input/Output	70	MSPI0 Data Bit 6						X	X	X	X	X
MSPI0_5	Input/Output	69	MSPI0 Data Bit 5		I		X		X	X	X	X	X
MSPI0_4	Input/Output	68	MSPI0 Data Bit 4		O		X		X	X	X	X	X
MSPI0_3	Input/Output	67	MSPI0 Data Bit 3					X		X	X	X	X
MSPI0_2	Input/Output	66	MSPI0 Data Bit 2					X		X	X	X	X
MSPI0_1	Input/Output	65	MSPI0 Data Bit 1	I		X		X		X	X	X	X
MSPI0_0	Input/Output	64	MSPI0 Data Bit 0	O		X		X		X	X	X	X

Table 21: MSPI1 Pin Muxing (Serial, Dual, Quad, Octal)

Pin Name	Direction	GPIO	Description	S0	S1	D0	D1	Q0	Q1	O0	O1
MSPI1.0	Output	33, 36, 49	MSPI1 CE0	O		O		O		O	
MSPI1.1	Output	49	MSPI1 CE1		O		O		O		O
MSPI1_9	Input/Output	104	MSPI1 DM0/DQS0 (Octal)							X	X
MSPI1_8	Output	103	MSPI1 CLK	O	O	O	O	O	O	O	O
MSPI1_7	Input/Output	102	MSPI1 Data Bit 7						X	X	X
MSPI1_6	Input/Output	101	MSPI1 Data Bit 6						X	X	X
MSPI1_5	Input/Output	100	MSPI1 Data Bit 5		I		X		X	X	X
MSPI1_4	Input/Output	99	MSPI1 Data Bit 4		O		X		X	X	X
MSPI1_3	Input/Output	98	MSPI1 Data Bit 3					X		X	X
MSPI1_2	Input/Output	97	MSPI1 Data Bit 2					X		X	X
MSPI1_1	Input/Output	96	MSPI1 Data Bit 1	I		X		X		X	X
MSPI1_0	Input/Output	95	MSPI1 Data Bit 0	O		X		X		X	X

*Not pinned out on the WLCSP package

The PADOUTEN register should be programmed to enable the proper pins for the selected mode. If using any mode with a data width less than Octal, the output clock can selectively be switched from the standard clock pin, MSPIn_8, to data bit 4 by setting the CLKOND4 bit. Typically, most serial SPI devices use a separate MOSI and MISO when operating in serial mode. The SEPIO0 or SEPIO1 bits in the DEV0CFG or DEV1CFG registers, respectively, should be set when software needs to read data from devices in serial mode, since it redirects the MISO input from pin 1 down to input data pin 0 of the MSPI's RX logic.

Table 22 below shows the required field configurations for typical MSPI operating modes. It should be noted that if the PADOUTEN_CLKOND4 is set to move the CLK pin from MSPIn_8 to MSPIn_4 (serial, dual or quad mode), then the PADOUTEN_OUTEN field must be adjusted accordingly, e.g., 0x101 becomes 0x011.

The I/O widths for data, address and instruction phases do not need to be the same in either PIO mode or XIP/DMA mode. 1-4-4 and other such mixed modes refer to the width of the instruction, address and data phases of the MSPI bus, respectively. The width(s) of the data phase, or both the address and data phases, of a command are selected by the PIOMIXED field of the MSPI_CTRLn register or by the XIPMIXEDn field of the MSPI_DEVnXIP register, where n is device0 or device1 for the particular MSPI instance. Depending on the I/O widths supported by the MSPI instance, the data width or both data and address widths can be specified as dual, quad or octal width.

Table 22: Required Settings for Typical MSPI Configurations

Mode (Data Lines and CE)					DEV0CFG_ DEVCFG0	DEV0CFG_ SEPIO0	DEV0XIP_ XIPMIXED0	PADOUTEN_ OUTEN
Instruction	Address	Data	Separate IO	Chip Enable (CE)				
Serial	Serial	Serial	Yes	0	SERIAL0 (1)	1	NORMAL (0)	0x101
Serial	Serial	Serial	No	0	SERIAL0 (1)	0	NORMAL (0)	0x101
Serial	Serial	Serial	Yes	1	SERIAL1 (2)	1	NORMAL (0)	0x110
Serial	Serial	Serial	No	1	SERIAL1 (2)	0	NORMAL (0)	0x110
Serial	Serial	Dual	No	0	SERIAL0 (1)	0	D2 (1)	0x103
Serial	Serial	Dual	No	1	SERIAL1 (2)	0	D2 (1)	0x130
Serial	Dual	Dual	No	0	SERIAL0 (1)	0	AD2 (3)	0x103
Serial	Dual	Dual	No	1	SERIAL1 (2)	0	AD2 (3)	0x130
Serial	Serial	Quad	No	0	SERIAL0 (1)	0	D4 (5)	0x10F
Serial	Serial	Quad	No	1	SERIAL1 (2)	0	D4 (5)	0x1F0
Serial	Quad	Quad	No	0	SERIAL0 (1)	0	AD4 (7)	0x10F
Serial	Quad	Quad	No	1	SERIAL1 (2)	0	AD4 (7)	0x1F0
Dual	Dual	Dual	No	0	DUAL0 (5)	0	NORMAL (0)	0x103
Dual	Dual	Dual	No	1	DUAL1 (6)	0	NORMAL (0)	0x130
Quad	Quad	Quad	No	0	QUAD0 (9)	0	NORMAL (0)	0x10F
Quad	Quad	Quad	No	1	QUAD1 (0xA)	0	NORMAL (0)	0x1F0
Octal	Octal	Octal	No	0	OCTAL0 (0xD)	0	NORMAL (0)	0x3FF
Octal	Octal	Octal	No	1	OCTAL1 (0xE)	0	NORMAL (0)	0x3FF
Hex	Hex	Hex	No	0	HEX0 (0x11)	0	NORMAL (0)	0x7FFFF
Hex	Hex	Hex	No	1	HEX1 (0x12)	0	NORMAL (0)	0x7FFFF

16.4 Board/Package Considerations for MSPI Pin Timing

16.4.1 Delay Step Size

Each delay step discussed in this section represents a delay of 80 to 200 ps / LSB per the DDR Delay Step Size provided in the MSPI section of the Electrical Characteristics.

16.4.2 SDR Mode with non-DQS

The timing parameters specified in the datasheet are based on 0-tap delay on both TX and RX delay lines, regardless of the actual number of taps being programmed. TX delay taps will delay the SCLK as illustrated by the red dotted line in Figure 23.

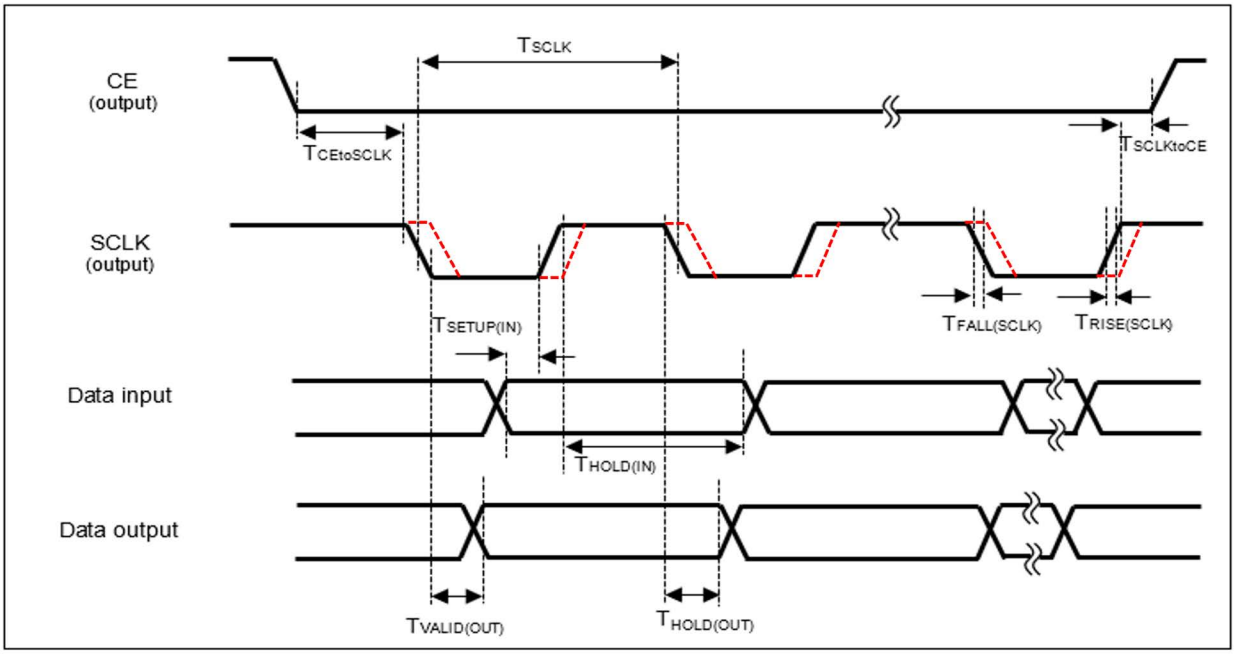

Figure 23. SDR Mode with Non-DQS

With more TX delay taps, Tvalid(out) will be sooner with respect to the delayed SCLK, but Thold(out) will be sooner as well.

The RX delay tap will delay the internal sampling clock (not shown in the timing diagram). With more RX delay taps, it allows a longer Tsetup(in) for external device, but a shorter Thold(in).

16.4.3 DDR Mode with DQS

The timing parameters specified in the MSPI section of the Electricals chapter are based on 0-tap delay on both TX and RX delay lines, regardless of the actual number of taps being programmed.

TX delay taps (TXDQSDELAY0) will delay the SCLK, as illustrated by the red dashed lines in the SCLK (output) waveform of Figure 24. With more TX delay taps, Tvalid(out) will be sooner with respect to the delayed SCLK, but Thold(out) will be sooner as well.

RX delay tap (RXDQSDELAY*0) will delay the DQS input in the chip, as illustrated by the red dashed lines in the DQS (input) waveform of Figure 24. With more RX delay taps, it allows a longer Tsetup(in) for external device, but a shorter Thold(in).

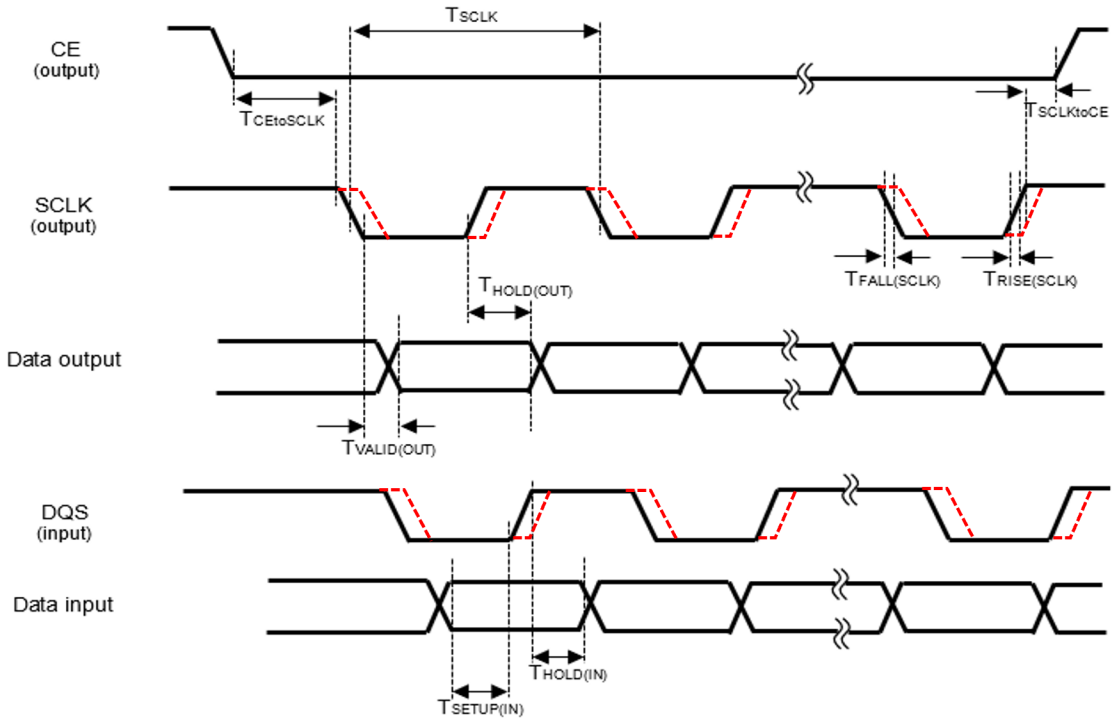

Figure 24. DDR Mode with DQS

Figure 25 shows DQS0 delay parameters in Octal/Hex DDR Mode with DQS, with respect to the input (RX) data byte (lower data byte for Hex) when RXDQSDELAYNEGEN = 0 and when RXDQSDELAYNEGEN = 1. See the fields in the DEVnDDR register which set these parameters.

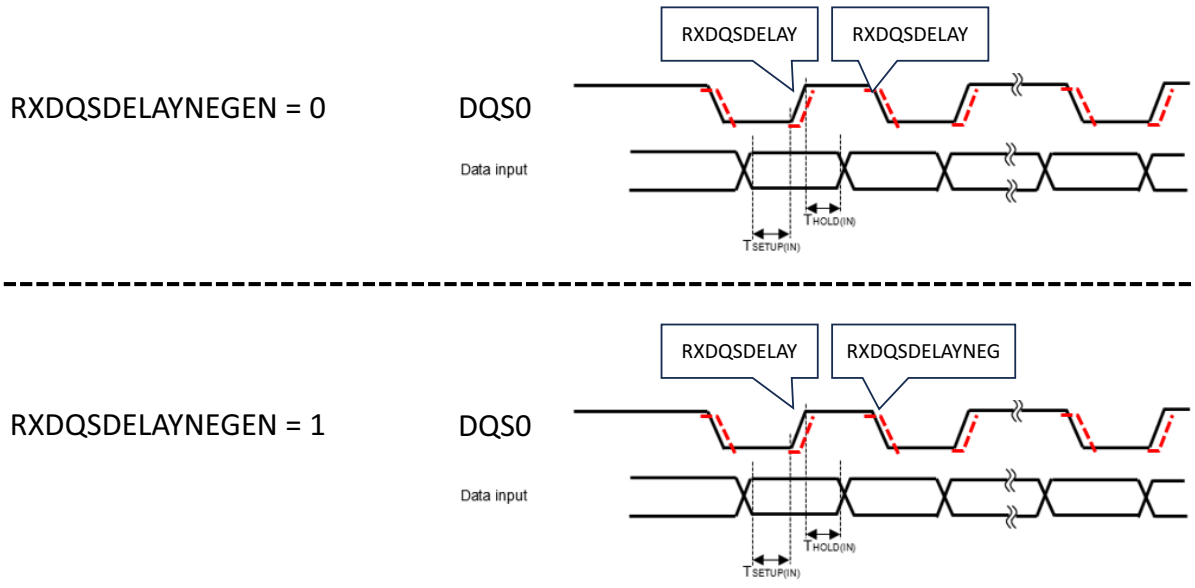

Figure 25. Octal/Hex DDR Mode with DQS - Read Delay Lines - Lower Data Byte DQS

Figure 26 shows DQS1 delay parameters in Hex DDR Mode with DQS, with respect to the upper input (RX) data byte under the following conditions:

1. RXDQSDELAYHIEN = 0 and RXDQSDELAYNEGEN = 0
2. RXDQSDELAYHIEN = 0 and RXDQSDELAYNEGEN = 1
3. RXDQSDELAYHIEN = 1 and RXDQSDELAYNEGEN = 0
4. RXDQSDELAYHIEN = 1 and RXDQSDELAYNEGEN = 1

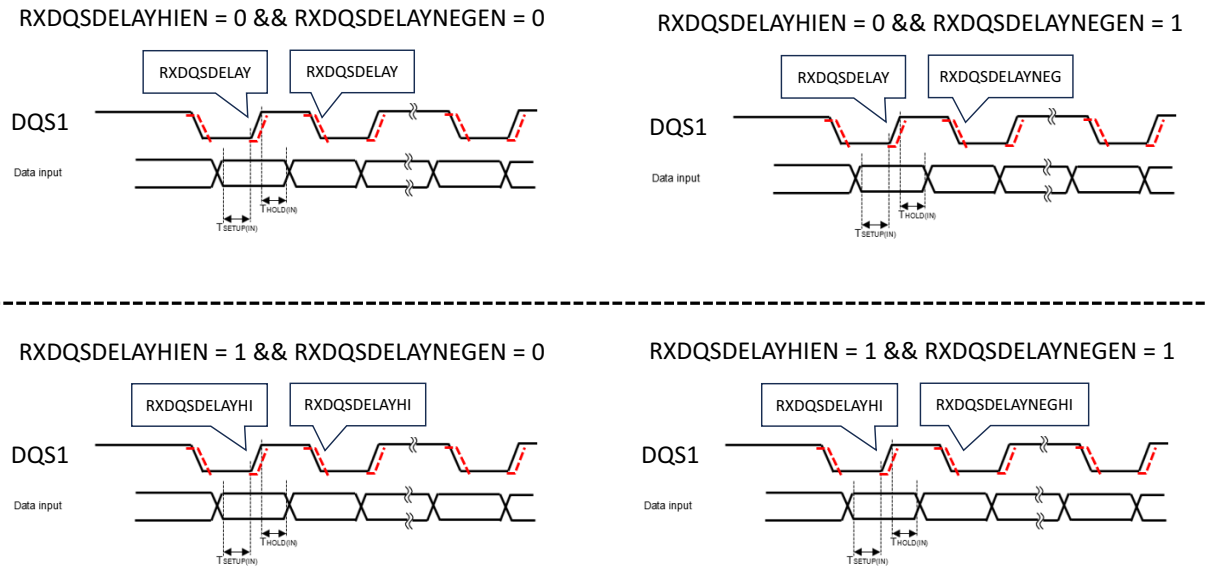

Figure 26. Hex DDR Mode with DQS - Read Delay Lines - Upper Data Byte DQS

16.5 Additional Information

Please refer to the MSPI registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

17. I²C/SPI Manager (IOM)

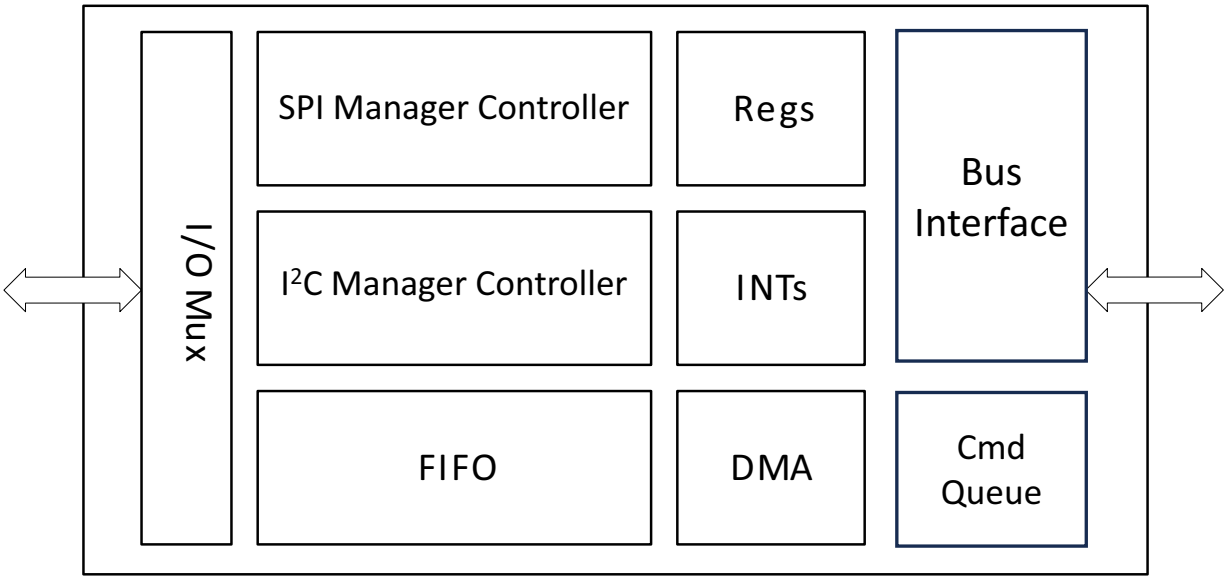

Figure 27. IOM Block Diagram

17.1 Features

The I²C/SPI Manager Module includes features shown in Figure 27 and listed below.

- Seven (7) controller instances supporting up to 4 chip selects per instance
- Up to 48 MHz clock for SPI interface
- I²C and SPI modes
- DMA with peripheral-to-memory and peripheral-to-peripheral supported
- Command Queue support

NOTE
There is no full-duplex transfer operation for IOM DMA on the Apollo510B SoC.

17.2 Functional Overview

The Apollo510B SoC includes 7 I²C/SPI high-speed manager modules, each of which functions as the manager of an I²C or SPI interface as selected by the IOMm_SUBMODCTRL_SMODnEN bit (m = 0 to 6, n=0 or 1) register field. A 64-byte bidirectional FIFO and a sophisticated command mechanism allow simple initiation of I/O operations without requiring software interaction.

In I²C mode the I²C/SPI Manager supports 7- and 10-bit addressing, multi-manager arbitration, interface frequencies from 1.2 kHz to 1.0 MHz and up to 4095-byte burst operations. In SPI mode the I²C/SPI Manager supports up to 4 subordinates with automatic nCE selection, 3- and 4-wire implementation, all SPI polarity/phase combinations and up to 4095-byte burst operations, with both standard embedded address operations and raw read/write transfers. Interface timing limits are as specified in the Serial Peripheral Interface (SPI) Manager Interface table of the Electrical Characteristics chapter.

NOTE

I2C clock stretching operation is not guaranteed on this SoC. If an I2C peripheral device that performs clock stretching is used, the recommendation is to perform compatibility testing with the Apollo510 I2C interface.

ERRATUM NOTICE

In normal read operation, the FIFO threshold interrupt (THR) and associated register bit (INTSTAT_THR) are asserted when the number of valid bytes in the read FIFO (FIFOPTR_FIFOnSIZ) equals or exceeds the value set in the read threshold field (FIFOTHR_FIFORTHR), and similarly for write operation.

When doing a FIFO read transaction (DMA or non-DMA), the write threshold check is not gated off. This could trigger an incorrect/invalid write interrupt which should be ignored. If the application uses the wrong interrupt to check the read data, incorrect data processing could result.

See “ERR008: IOM: FIFO threshold interrupt incorrectly triggered” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

17.3 Data Alignment

All data accesses between the MCU and the IOM interface are word aligned. Since the transfer size is specified in bytes, unused bytes within the word will either be discarded (for write operations) or filled with zero (read operations) to align to the next word boundary. DMA operations support a byte starting address, and the programmed DMA address does not have to be word aligned. Direct mode write operations will start transferring the least significant byte of the word (little endian style) at the current write FIFO pointer. If any remaining bytes are unused in a word at the end of the write operation, they will be discarded, and the write pointer will be set to the next word location. Direct mode read operations will store the first received byte into the least significant byte of location specified by the read FIFO pointer, and will fill any unused byte locations with zero if the transaction size is not a word multiple. The FIFO read pointer will point to the next FIFO location in the read FIFO, which will be word aligned.

17.3.1 Direct Mode Data Transfers

Direct mode data is enabled when DMA is disabled via the IOMn_DMACFG_DMAEN and the data transfer size (TSIZE) is greater than 0. In this mode, the MCU transfers data via direct writes or reads to registers in the IOM. The IOM maintains separate FIFO pointers for the read and write FIFOs, and updates these when a PUSH or POP register is accessed. Writing to the IOMn_FIFOPUSH register will perform a push event of the word into the FIFO and update the write pointer by 4 bytes. Only word accesses are supported to the IOM, and any unused bytes within a word will be discarded. An example of a 5 byte write transfer is shown below.

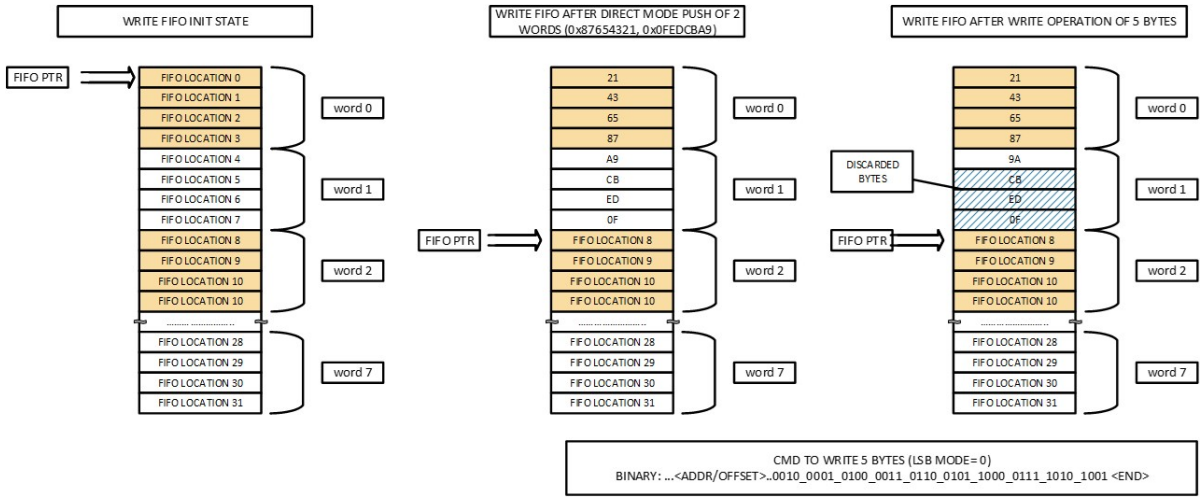

Figure 28. Direct Mode 5-byte Write Transfer

Reading from the IOMn_FIFOPOP register will perform a POP operation, return 4 bytes of data and advance the internal read FIFO pointer by 4 bytes. Any unused bytes within the read data will be filled with zeros and aligned to a word boundary at the end of the transaction. An example of a 5 byte read operation is shown below.

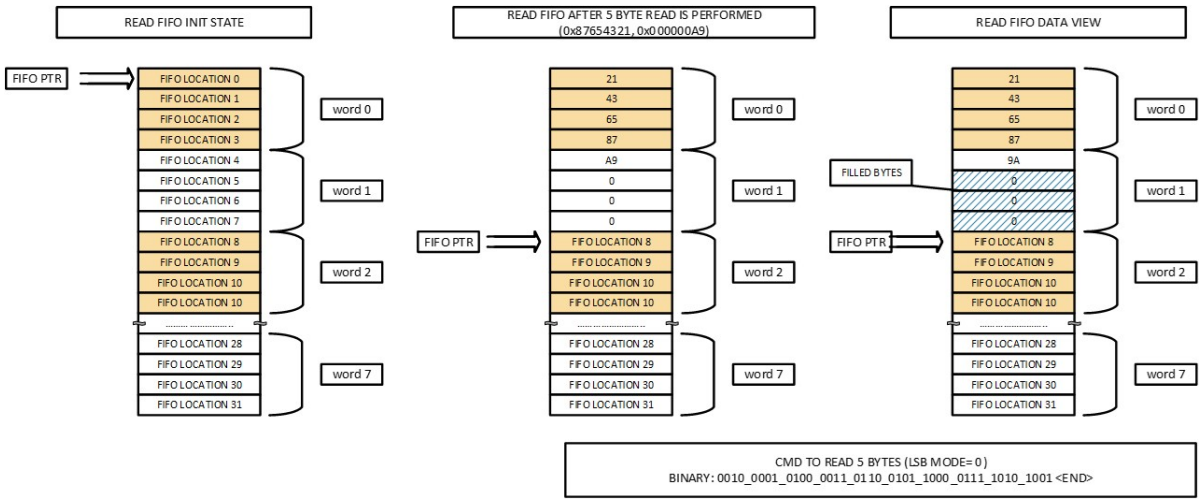

Figure 29. Direct Mode 5-byte Read

The IOM also supports a non-destructive POP mechanism to prevent unintended POP events from occurring. If the IOMn_FIFOCTRL_POPWR field is active (1), a write to the IOMn_FIFOPOP register will be required in order to complete the POP event. Reads will return the current data.

An active transaction will be paced by data availability and will hold the clock low if there is not enough data to continue write operations, or if the read FIFO is full during read operations. This wait condition is indicated when the IOMn_CMDSTAT_CMDSTAT field is 0x6. Once new data or FIFO locations are present, the command will continue operation automatically.

17.3.2 DMA Data transfers

DMA transfers are enabled by configuring the DMA related registers, enabling the DMA channel, and then issuing the command. The command will automatically fetch and store the data associated with the command without MCU intervention. The DMA channel is enabled via the IOMn_DMACFG_DMAEN field. P2M DMA operations transfer data from peripheral to memory and are used in IOM READ operations. M2P DMA operations transfer data from memory to peripheral and are used in IOM write operations. DMA transfer size is programmed into the IOMn_DMATOTCOUNT register and supports up to 4095 bytes of data transfer. The DMA transfer size is independent from the transaction size, and allows a single DMA setting to be used across multiple commands. The direction of DMA data transfer must match the command. The IOMn_DMACFG_DMAEN field enables/disables the DMA transfer capability and must be set last when configuring the DMA, generally prior to sending the command.

The DMA engine within the module will initiate a transfer of data when a trigger event occurs. There are 2 types of triggers available, threshold (THR) and command completion (CMDCMP). The THR trigger will activate when the threshold programmed into the FIFOWTHR or FIFORTHR in the IOMn_FIFOTHR register meets the data criteria. Because the MCU access to the interface is 32 bits wide, only the word count of the selected THR is used, and the low order bits of the FIFOWTHR or FIFORTHR are ignored.

During the transfer, the TOTCOUNT register is decremented to reflect the number of bytes transferred.

For IOM write operations (data written from IOM out to an external device), the THR trigger will activate when the write FIFO contains FIFOWTHR[5:2] free words. If the remaining DMA transfer size is less than this, only the needed number of words are transferred.

For IOM read operations (data read from external device), the THR trigger will activate when the read FIFO contains FIFORTHR[5:2] words of valid data. If the remaining DMA transfer size is less than the RTHR words, then the CMDCMP trigger can be enabled to transfer the remaining data. If the CMDCMP trigger is disabled, and the number of bytes in the read FIFO is greater to or equal to the current TOTCOUNT, a DMA transfer of TOTCOUNT will be done to complete the DMA operation. This mode requires that the THR trigger be enabled as well.

The CMDCMP trigger activates when the command is complete and will transfer the lesser of the TOTCOUNT or the number of bytes in the read FIFO. Note that this trigger is not needed for write operations, and the THR trigger should be used in this case. If a read operation is done, and the THR trigger is disabled, and only the CMDCMP trigger is enabled, and the transaction size is greater than the FIFO size (32 bytes), the module will hang, as there is no trigger to cause a DMA operation, and the logic will pause the interface until there is room within the read FIFO to store data.

If DMA transfer size is matched to the IOM transaction size, it is recommended to program both the FIFORTHR and FIFOWTHR to 0x10 (16 bytes) and only enable the THR trigger.

17.4 Transaction Initiation

To start a transaction, the IOM module must be powered up and the target external pins enabled via the GPIO module. For SPI transactions, this will generally require 4 pins to be enabled via the function select field of the PADREG registers in the GPIO module. The CEN pin for SPI transaction requires setting of the FNCSEL field of the appropriate pin, as well as the CFGREG of the corresponding pin. This also includes the setting of the default value of the CEN. This is needed to allow the IOM module to power down and not activate the CEN signal.

Once the IOM module is powered on, and the external pins configured, the IOM submodule must be enabled via the IOMn_SUBMODCTRL register. This will activate either the SPI or I^2C interface. Once this is complete, the submodule specific registers should be configured to set the desired mode and features. If DMA is desired, the DMA registers should also be set, with the IOMn_DMACTRL_DMAEN field set last. The registers relating to DMA operations are as follows:

- IOMn_DMATRIGEN – Sets the trigger source for starting a DMA transfer

- IOMn_DMACFG – Sets the DMA direction and enable for DMA
- IOMn_DMATOTCOUNT – Sets the total count of bytes to be transferred via the DMA operation. Recommended to match the IOMn_CMD.TSIZE field for simplicity.
- IOMn_DMATARGADDR – The source or destination address of the DMA data. Sources can be either SRAM or storage. Destination address can only be SRAM. This is the memory mapped address of the DMA data as accessed by the MCU.

After the module setup is complete, the command register is written. This will start the IO transfer. The IOMn_CMD register contains the command itself, along with other fields used in the command, such as channel number, offset counts and transfer size. The IOM supports 2 main commands, read and write. A read command will write user selectable number of offset bytes (0 to 3), and then read IOMn_CMD_TSIZE bytes, storing the data into the read FIFO. A write command will write the user selectable number of offset bytes (0 to 3), followed by a write of IOMn_CMD_TSIZE bytes sourced from the write FIFO. Transfer sizes can be 0-4095 bytes for SPI operations and 0-512 bytes for I^2C operations. The number of offset bytes for each command is specified in the IOMn_CMD_OFFSETCNT field.

17.5 Command Queue

The IOM module can also fetch register write data from SRAM or storage, and update the registers as if the write was performed via the MCU. Register data is stored as a doublet of 2 words. The first word is the module register address offset, word aligned. The second word is the write data value. Once enabled, the command queue (CQ) will fetch the address and perform a write to the register. If no command is started by the register write, the next doublet will be fetched by the CQ. If a command is started (write to IOMn_CMD register is done), the CQ processing will wait until the transaction is complete before fetching the next register write doublet. This is shown in the diagram below. No prefetching is done via the CQ, and the register write operations are performed in series with the transactions. This allows a predictable path for execution of commands. DMA enabled commands should be used during CQ operation, as there is no support to perform a direct mode read operation via the CQ.

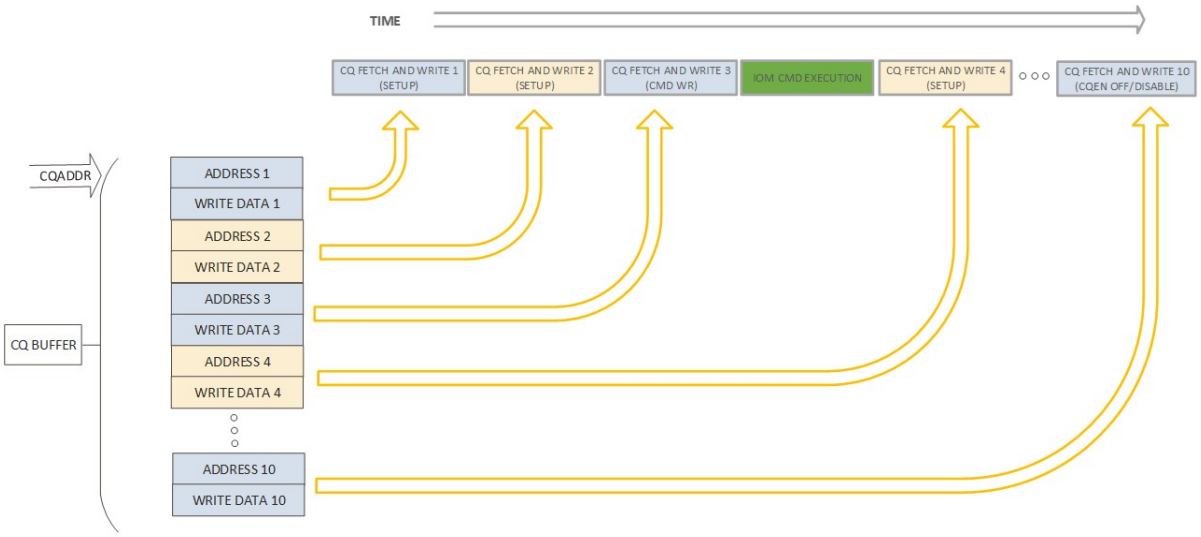

Figure 30. Register Write Data Fetches

The CQ starting fetch address is specified in the IOMn_CQADDR register. The CQ operation will start to fetch when the IOMn_CQCFG.CQEN field is set. This field should only be set when the IOM is idle and the FIFOs are empty. Once enabled, the CQ will continue to fetch sequentially until it encounters a pause event. A pause event can be caused by a CQ register write operation, or from external signals. This is

shown in the sequence below.

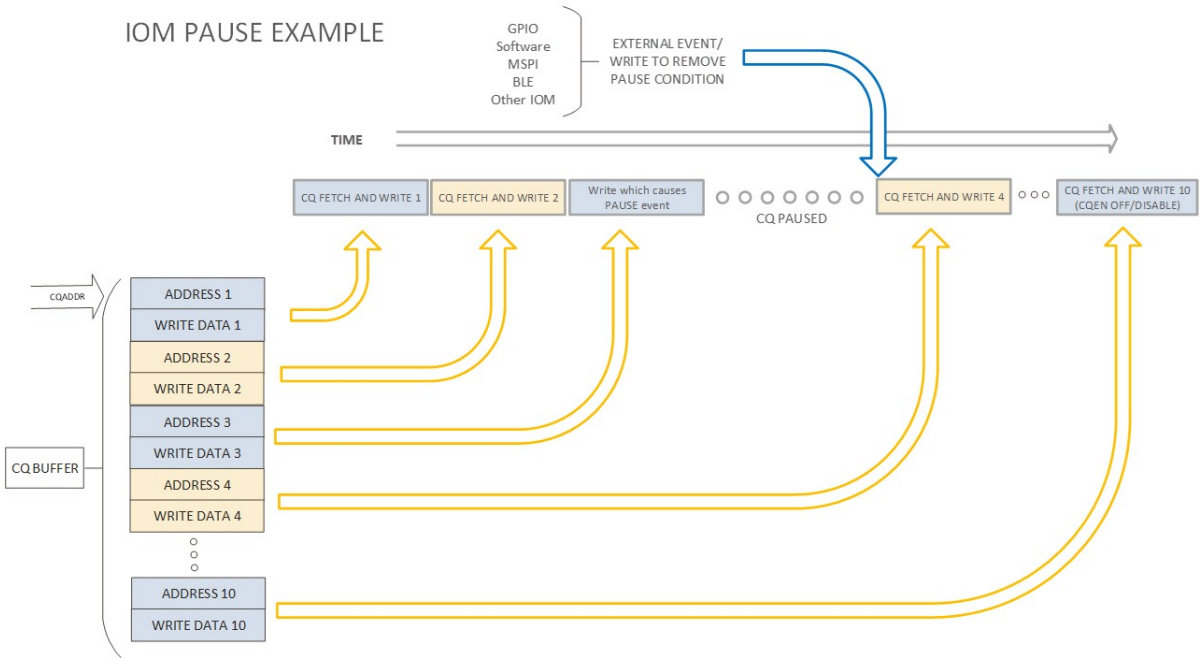

Figure 31. IOM Pause Example

Each pause source is independently enabled via the IOMn_PAUSEEN register. In addition to independent enable of the pause bits, there is also independent control of which pause event will signal a CQPAUSE interrupt. This is controlled through the IOMn_CQFLAGS.CQIRQMASK field.

There are 16 possible pause sources. When the value of the pause source is set, and the pause is enabled in the IOMn_PAUSEEN register, the CQ will stop fetching. The IOMn_CQADDR is updated after each fetch, and when paused, will point to the next doublet to be fetched when the pause condition is removed. The connection of the pause bits are shown below. The SW Flags are accessed via the IOMn_CQSETCLEAR register.

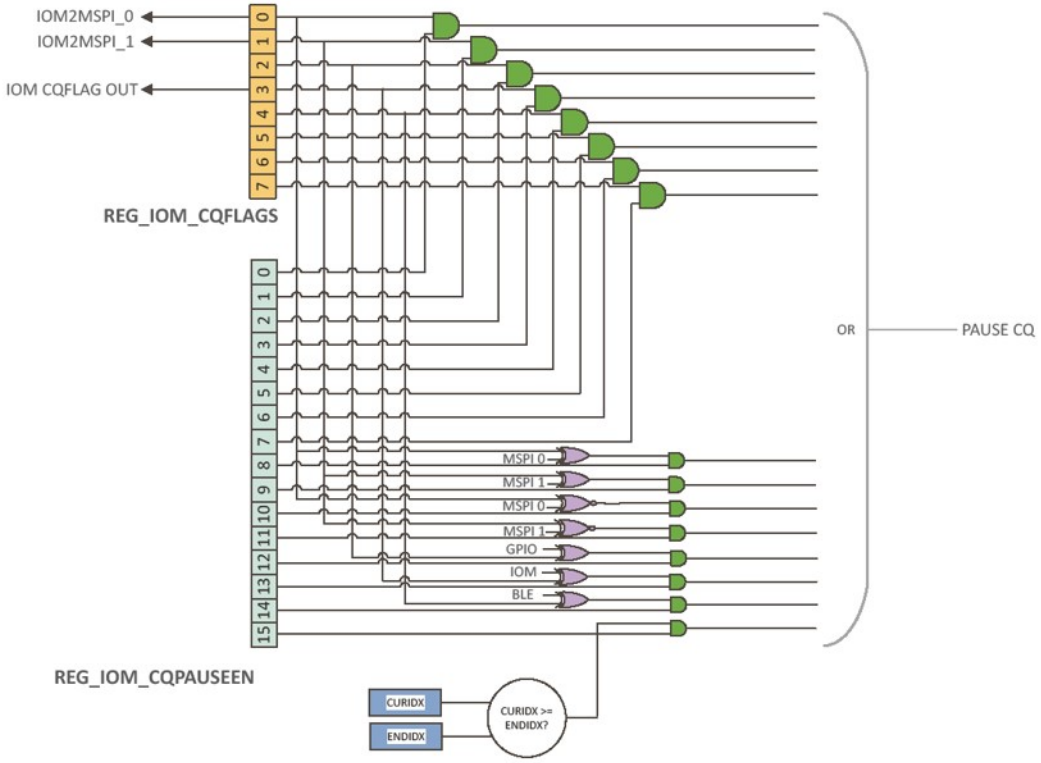

Figure 32. CQ Pause Bit Fetching

The first 8 pause sources (bits 7:0) are register bits which are directly writable via the MCU or through the CQ. These first 8 locations are called SW Flags. Because the CQ does not support a read-modify-write operation, special facilities are available to set, reset or toggle the SW Flags. This is accessed through the IOMn_CQSETCLEAR register. The 3 fields in this register allow a per bit set, reset or toggle of the SW Flag bits.

The next 7 pause sources (bits 14:8) use the SW Flags along with an external signal to set the pause event. The external signals are from the GPIO module, the MSPI module, or other IOM modules. On some cases, such as the MSPI interface, 4 of the SW Flags are used and combined with 2 similar signals from the MSPI module to facilitate a ping pong method of sharing 2 buffers and preventing overruns without MCU intervention.

The last pause source (bit 15) is used for index pausing. If this pause bit is enabled, the CQ will pause when the value of the IOMn_CURIDX matches the IOMn_ENDIDX. This is useful for software to be able to update the CQ buffer without causing a race condition between the CQ data buffer writes and the CQ fetches.

17.5.1 CQ Programming Notes

Following are some points to consider when programming command queue operation.

- Additional restrictions when using the CQ function is that the DMA must be disabled prior to writing the IOMn_CQADDR register, either from the MCU or from the CQ itself.
- For multiple commands using DMA, the DMAEN must be reset after the command is done and before the DMA registers are set for the next transaction.
- It is possible for the CQ to write the IOMn_CQADDR register during the CQ operation. The new address will take effect on the next fetch and allows the CQ to be relocated or looped.

- When starting the CQ operation, 1 doublet will be fetched regardless of the state of the pause status and bits. If any pause is active, it will take effect after the first fetch. For this reason, it is generally advisable to have a dummy register write as the first CQ doublet.

CQ write operations to SW flags used in combination with pause events 15:8 must first disable the pause enable, perform the SW flag write, then re-enable the pause enable register. SW flags 7:0 can be written without this restriction and will cause a pause immediately if activated.

17.6 Additional Information

Please refer to the IOM registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

18. Full Duplex SPI Subordinate (IOSFD)

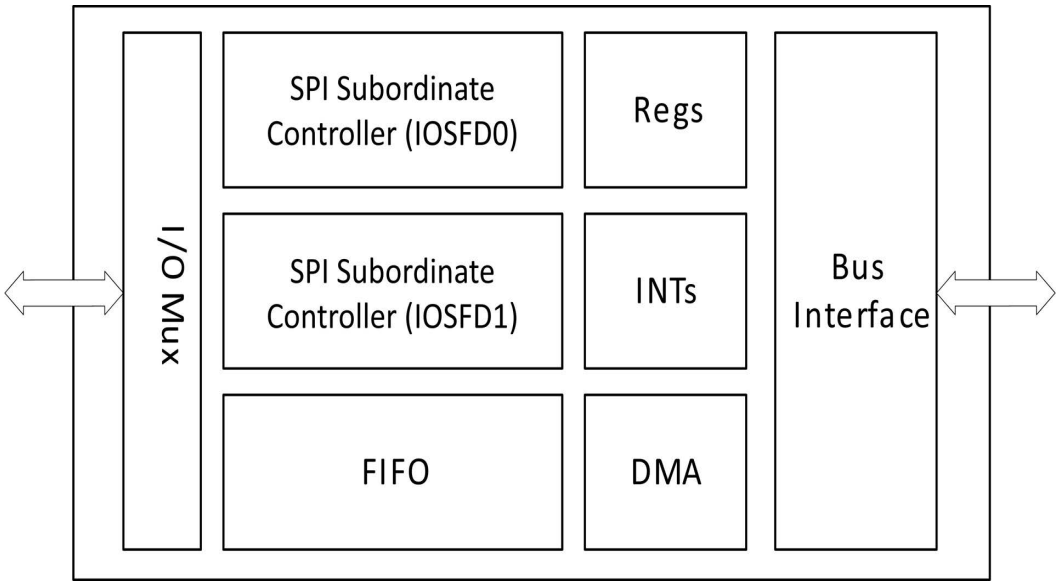

Figure 33. Full Duplex IOS SPI Subordinate Controller Pair (IOSFD0 / IOSFD1)

18.1 Features

The Apollo510B SoC includes two instances of the Full Duplex SPI Subordinate and both instances are designed to work in tandem to enable full duplex (FD) operation. Features of the controller pair are shown in Figure 33 and listed below.

- Functions as a synchronous communications subordinate in a SPI configuration
- Supports DMA mode
  - DMA total transfer count support for 64 kB data
  - Supports DMA complete and DMA error interrupts
- Supports full duplex operation when both instances are used in combination
- Each instance can work individually to provide half duplex operation
- May be placed in a sleep mode and still operate over the I/O interface
- Each controller contains 64 bytes of Local RAM (LRAM) maintained in deep sleep mode for data/parameter storage, which can be configured flexibly as three operational blocks
- Extensive set of interrupts to control data flow and command processing, and provide alerts for writes to various locations

NOTE

Restrictions on IOSFD operation:

1. Only one IOSFD can be operational at a time when operating in half duplex mode due to interface signals of both instances using the same set of IO pads.
2. Simultaneous DMA read and write operations are not supported for an IOSFD configured for half duplex. The DMA transfer direction should be configured properly.
3. Command Queue is not supported for IOSFD.
4. DMA mode is supported only for IOSFD FIFO mode (Host read/write to IO address 0x7F).

ERRATUM NOTICE

When configured as a SPI subordinate using the IOSFD module, the Apollo510 does not tri-state the MISO pin when CE is deasserted. Instead, the MISO pin is driven static low when CE is driven high.

See “ERR011: IOS: MISO line is not tri-stated when CE is deasserted” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

When using the IOSFD, the XCMPRF (Read from FIFO space transfer complete) flag is incorrectly set, instead of the XCMPRR (Read from register transfer complete) flag, on host reads of the 0x7C FIFOCNTLO (FIFO Counter Low-Byte) Host Address Register. This same behavior is seen during host reads of 0x7D FIFOCNTUP (FIFO Counter High-Byte) Host Address Register) as well.

See “ERR037: IOS/IOSFD: Erroneous XCMPRF interrupt triggered” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

18.2 Functional Overview

The Apollo510B SoC includes two instances of the Full Duplex SPI Subordinate module, IOSFD0 and IOSFD1, which in combination support full duplex operation. Only SPI mode is supported in the IOSFD module, and it supports all polarity/phase combinations and interface frequencies as specified in the Serial Peripheral Interface (SPI) Subordinate Interface sub-section of the Electricals. The IOSFD0 module can function as a half duplex SPI interface. The device may be placed in a sleep mode and still receive operations over the I/O interface. The subordinate may be configured to generate an interrupt on specific references.

Each IOSFD instance contains 64 bytes of LRAM which is only accessible when the module is enabled. This RAM may be flexibly configured into three spaces:

- A block directly accessible via the I/O interface.

- A block which functions as a FIFO for read operations on the interface. This area is required because DMA transfers must utilize the FIFO.
- A block of generally accessible RAM used to store parameters during deep sleep mode. Although this can be configured for use in IOSFD, it is not recommended.

18.3 Full Duplex DMA Features

The IOSFDn interface connection options are configured on the following pads with the functions selected with the Function Select (FNCSEL) values as shown:

- GPIO0 (FNCSEL = 1) - SLFDSCK - the input clock which is connected to both IOSFD0 and IOSFD1.
- GPIO1 (FNCSEL = 1) - SLFDMOSI - the input data which is connected to both IOSFD0 and IOSFD1.
- GPIO1 (FNCSEL = 2) - SLFDSDAWIR3 - the bidirectional data in/out which is connected to IOSFD0.
- GPIO1 (FNCSEL = 10) - SLFD1WIR3 - the bidirectional data in/out which is connected to IOSFD1.
- GPIO2 (FNCSEL = 1) - SLFDMISO - the output data which is connected to IOSFD0.
- GPIO2 (FNCSEL = 10) - SLFD1MISO - the output data which is connected to IOSFD1.
- GPIO3 (FNCSEL = 1) - SLFDnCE - the input nCE which is connected to both IOSFD0 and IOSFD1.
- GPIO4 (FNCSEL = 1) - SLFDINT - the interrupt out which is connected to IOSFD0.
- GPIO4 (FNCSEL = 10) - SLFD1INT - the interrupt out which is connected to IOSFD1.

The output data from IOSFD1 instead of IOSFD0 may be connected to GPIO2 by selecting SLFD1MISO. The interrupt output from IOSFD1 instead of IOSFD0 may be connected to GPIO4 (by selecting SLFD1INT). This allows half duplex testing of both IOSFD modules.

In normal operation, GPIO2 is connected to IOSFD0 and IOSFD0 is configured to execute a DMA write transaction (DMACFGn_DMADIR = 0). IOSFD1 is configured to execute a DMA read transaction (DMACFGn_DMADIR = 1). Separate memory addresses (in DMATARGADDR_TARGADDR) must be configured in the two IOSFD modules, but the transfer length DMATOTCOUNT_TOTCOUNT may or may not be the same in both modules. Once the modules are enabled, they both respond independently to a full duplex transfer on the interface, with the read and write DMA operations proceeding in parallel. DMA completion and error interrupts will typically occur in both modules simultaneously.

Configuring a full duplex DMA environment involves several steps:

1. Configure the pinmux to connect the four IOSFD pads to both IOSFD0 and IOSFD1, with IOSFD0 supplying the MISO signal and executing the DMA write and IOSFD1 executing the DMA read.

   [Note that the DMA direction is the opposite of the interface direction, which may be confusing. On a DMA write, data is read over the interface (using MISO) and written to memory. On a DMA read, data is read from memory and written over the interface (using MOSI).]

2. Set DMADIR to 0 in IOSFD0 and to 1 in IOSFD1.
3. Set the DMACFG_FRCDMA bit to 1 in both modules. Set the DMACFG_FRCRDWRT bit to 1 in IOSFD0 and to 0 in IOSFD1.
4. Set the DMACFG_PADBYTEEN bit to 1 in IOSFD0 and configure the desired DMACFG_PADBYTE value. These fields can also be set in IOSFD1 but have no effect on DMA reads.

The Host must send an address byte at the beginning of the transfer, but the R/W bit is ignored and each IOSFD module executes the desired transfer.

Figure 34 shows the basic environment and test structures. A full duplex configuration is shown.

18.4 Full Duplex DMA Transfers in SPI Mode

Full duplex transfers are implemented by configuring a DMA read in one IOSFD (IOSFD1 in Figure 34) and a DMA write in the other IOSFD module (IOSFD0 in Figure 34). The configurations force IOSFD1 to treat the transfer as a read and IOSFD0 to treat the transfer as a write, independent of the R/W bit. Both

modules are connected to SCK and nCE so they execute a synchronized transfer. The Host sends the DMA read data on MOSI (to IOSFD1) and receives the DMA write data on MISO (from IOSFD0).

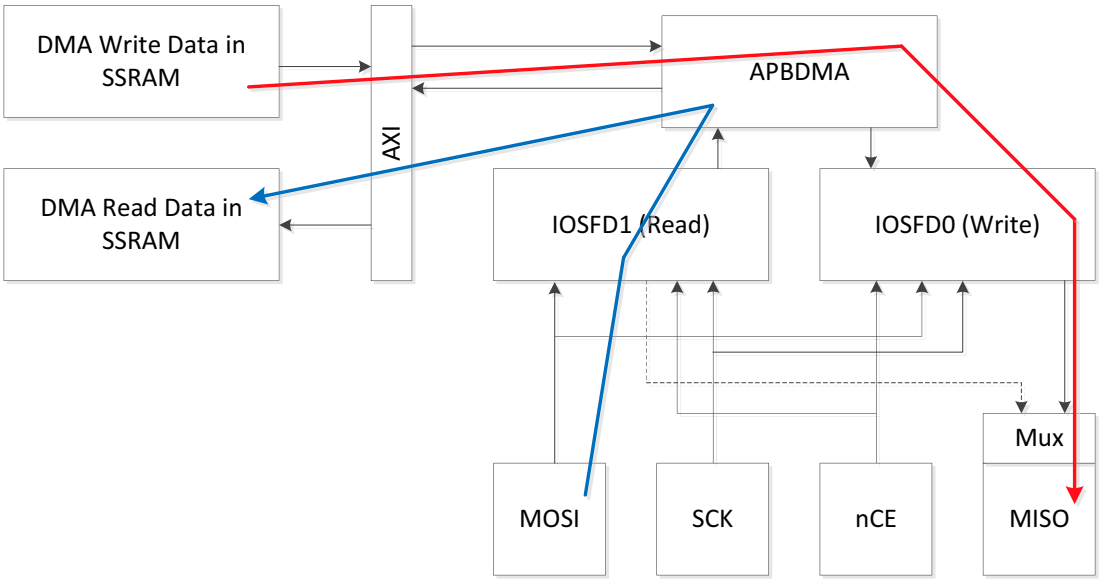

Figure 34. Full Duplex IOS DMA Transfers in SPI Mode

18.5 Half Duplex DMA Reads in SPI Mode

Half duplex DMA reads use the data flow path shown by the blue arrow in Figure 35.

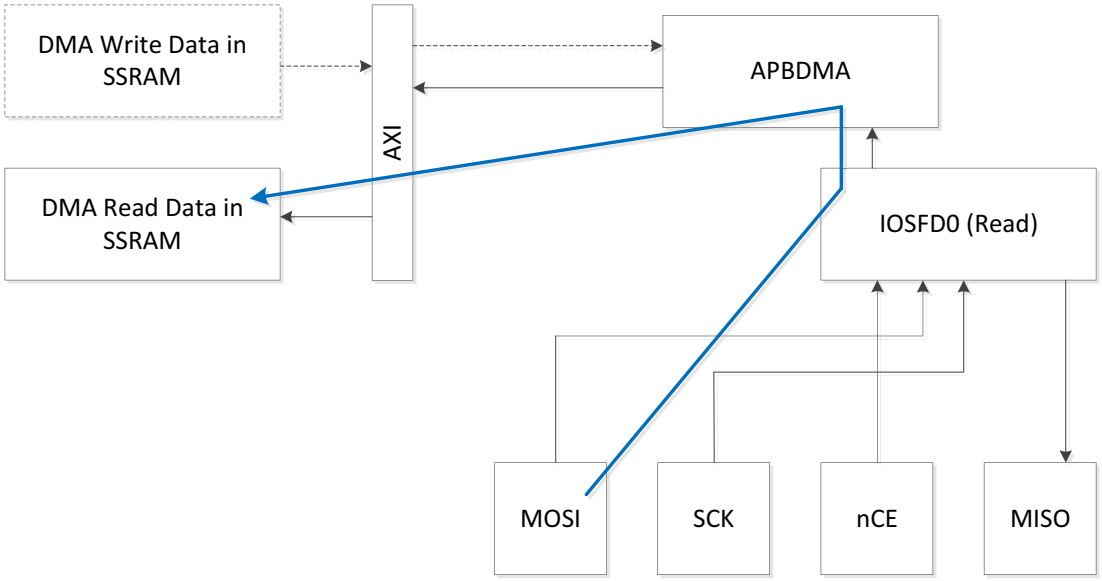

Figure 35. Half Duplex IOS DMA Reads in SPI Mode

Once the DMA transfer is configured in the IOSFD0 module, the Host initiates a write transfer, generating the clock SCK and the chip enable nCE with data coming in on the MOSI pad. The transfer address must be the FIFO address 0x7F. The data flows through the IOSFD FIFO in the LRAM, and the APBDMA

Controller reads that data over the APB and writes it into the target memory (such as SSRAM0) via the AXI bus.

18.6 Half Duplex DMA Writes in SPI Mode

Half duplex DMA writes use the data path shown by the red arrow in Figure 36.

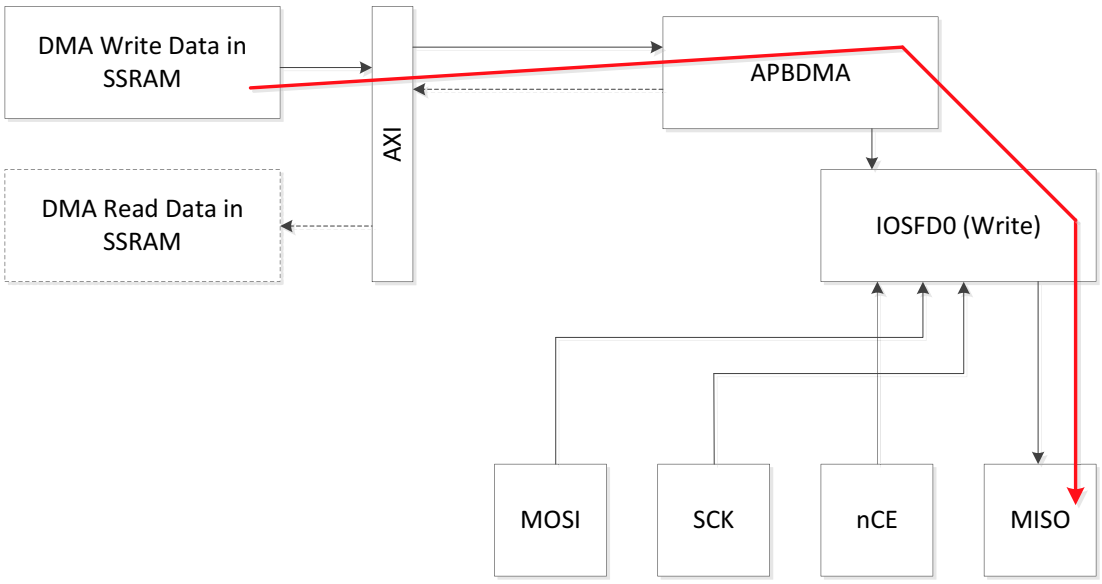

Figure 36. Half Duplex IOS DMA Writes in SPI Mode

IOSFD0 makes DMA requests and the APBDMA controller transfers data from the source memory (such as SSRAM1) via the AXI bus to the IOSFD0 FIFO in the LRAM. The Host initiates a read transfer, generating the clock SCK and the chip enable nCE with data flowing out of IOSFD0 on the MISO pad. The transfer address must be the FIFO address 0x7F.

18.7 IOSFD DMA Registers

Several registers are included in the IOSFDn register set to support DMA operations. Please refer to the IOSFD registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

18.8 IOSFD LRAM Configuration for DMA

The first step in configuring the IOSFD is to allocate the LRAM memory regions. Since we often want the Host to be able to transfer commands into the IOSFD, we typically assign a small part of memory, i.e., 8 or 16 bytes, as the Direct region by setting FIFOBASE to 1 or 2. We can then use the REGACC interrupts to signal the CPU that there is a command available. If we don't need any LRAM area, which is by far the most common case, the remaining LRAM is typically assigned to the FIFO area by setting FIFOMAX to 32. All DMA transfers will go through the FIFO area. If the Direct Area of memory is not used, FIFOBASE can be set to 0 to maximize the size of the FIFO.

The IOSFD modules, IOSFD0 and IOSFD1, contain 64 bytes of LRAM each. FIFOMAX must be 8 or less, and FIFOBASE must be small enough to configure at least 48 bytes of FIFO space.

18.9 Executing a DMA Operation

An operation is initiated by the Host signaling to the MCU that a transfer will be executed, i.e., sending a command. This requires an interrupt to be generated to the CPU, waking it up if necessary, which can be done in several ways:

- Generating a hardware interrupt to the SLINT input pad from a Host pin.
- Generating a hardware interrupt to a GPIO input pad from a Host pin.
- Generating a software interrupt by writing to the HOST_WCS register in the IOSFD at address offset 0x7B.
- Generating a software interrupt by writing to the Direct memory area with the appropriate REGACC interrupt(s) configured. This is the recommended method.

Once the command has been detected, software on the CPU determines what the desired DMA parameters are - transfer direction, length and target address. Software then configures the DMA transfer in APB_DMA and IOSFD and starts the DMA operation. At this point the CPU must send a handshake signal to the Host indicating that the IOSFD is ready for the transfer. This handshake can be through a GPIO output pad to a Host pin.

When the Host detects that the IOSFD is ready for a transfer, it initiates a burst transfer (read or write) to the first address in the FIFO area, which is typically address offset 8 or 16. The Host then streams as much data as specified. The IOSFD transfers this data to or from the Host, and initiates DMA transfers as necessary to empty/refill the FIFO in the LRAM. The addresses in the LRAM rolls over from FIFOMAX-9 to FIFOBASE. When the DMATOTCOUNT_TOTCOUNT reaches 0, the operation terminates and a DMASTAT_DMACPL interrupt is generated.

After the operation is complete, the system waits for the receipt of another command from the Host, and the process continues.

18.10 Interrupt Processing

Two new interrupts, DCMP and DERR, are included in the IOSLAVEINT interrupt register. DCMP indicates the end of a DMA transfer, and the XCMPRR/XCMPRF and XCMPWR/XCMPWF interrupts are used as the Transfer Complete interrupts for read and write bursts respectively.

The DCMP interrupt (and the DMACPL status bit) is set when the DMA transfer completes, and the XCMPRF/XCMPWF interrupts (and the DMASTAT_XFRCMP status bit) is set when the IO transfer completes on the interface. In general software should enable the DCMP interrupt on P2M transfers (Peripheral-to-Manager, or DMA reads), and should enable the XCMPRF interrupt on M2P transfers (Manager-to-Peripheral, or DMA writes). The expected behavior is described in Table 23:

Table 23: DMA Interrupt Processing

DMADIR	Host-TOT	Interrupt	DMACPL	UNDFL	TOTCOUNT	DMAFSIZE	XCMPWF
0:P2M	==	DCMP	1	0	0	0	1
0:P2M	<	DCMP	1	0	Note 1	0	1
0:P2M	>	DCMP	1	0	0	Note 2	Note 2
1:M2P	==	XCMPRF	1	0	0	0	0
1:M2P	<	XCMPRF	Note 3	0	Note 4	Note 5	0
1:M2P	>	XCMPRF	1	1	0	Note 5	0

Table Notes:

Note 1: (Initial TOTCOUNT - Final TOTCOUNT) = number of bytes written to memory.

Note 2: If XCMPRF = 1, if DMAFOVF = 0, DMAFSIZE contains the number of valid bytes in the FIFO which were received from the Host but not written to memory. If DMAFOVF = 1, the number of valid bytes in the FIFO is unknown because the FIFO has been overwritten. It is possible that for a very slow interface executing a very long transfer, XCMPF will still be 0 when the DCMP interrupt is serviced. If software needs the remaining FIFO information it must wait until XCMPRF becomes 1 to read DMAFSIZE and DMAFOVF.

Note 3: If the Host interface is very fast, the internal buses are heavily utilized and the CPU responds very quickly to interrupts. There is a very small probability that DMACPL is not asserted when the XCMPRF interrupt is received. But in any case, it will be set soon after that.

Note 4: (Initial TOTCOUNT - Final TOTCOUNT) = number of bytes read from memory. This will be more data than was actually transferred on the Host interface and is not a useful value.

Note 5: DMAFSIZE is not valid.

The XFRCOUNT register field contains the number of bytes actually transferred on the interface on a DMA read, and the number of bytes actually transferred + 1 on the interface on a DMA write or in the write IOSFD in a full duplex transfer. This is very useful in determining any “extra” data in the FIFO at the completion of an operation.

For a full duplex transfer, the terminating interrupt should be DCMP on the IOSFD that is implementing the DMA read, which is typically iOSFD1. The status values in each IOSFD is a function of the configured DMA length, which may be different in each IOSFD, and the Host transfer length, which is the same in both IOSFDs.

18.11 Full Duplex DMA Processing

At the completion of each DMA operation, after reading all relevant status information, DMAEN should be set low. This will reset many of the status register bits and prepare the module for the next operation. All configuration fields should be written and all status and interrupt bits cleared *before* DMAEN is set to 1.

For full duplex transfers, the following sequence should be used. This assumes IOSFD0 is implementing the DMA write and IOSFD1 is implementing the DMA read.

1. Make sure DMAEN is clear in IOSFD0 and IOSFD1.
2. Configure each IOSFD instances for its respective transfer. Clear any writable status bits like DMAUNDFL and DMAERR.
3. Enable the DCMP interrupt on IOSFD1. This will be the last interrupt status set on a correct transfer.
4. Set DMAEN for both IOSFD instances.
5. Wait for the DCMP interrupt from IOSFD1 (not from IOSFD0). At this point the Host should have read the correct data (not all PADBYTES).
6. The XCMPRF and DCMP interrupts should be set for IOSFD0, and the XCMPWF interrupt should be set for IOSFD1. These should be checked.
7. Read any status (TOTCOUNT, XFRCOUNT, etc.) to determine the transfer result.
8. Clear DMAEN for both IOSFD instances.

After DMAEN is set on the DMA read side (IOSFD1 in the typical case), the first transfer executed by the Host MUST be the actual full duplex transfer. The Host must not attempt to access any other interface address, such as the Direct Address space or the IOINT module.

Once the interface transfer is complete, the Host may then access other offsets within the IOSFD. These accesses (reads and writes) will all go to the IOSFD configured for the DMA write transfer (IOSFD0 in the typical case). No interface accesses will occur to the other IOSFD module.

18.12 Additional Information

Please refer to the IOSFD registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

19. Universal Asynchronous Receiver/Transmitter (UART)

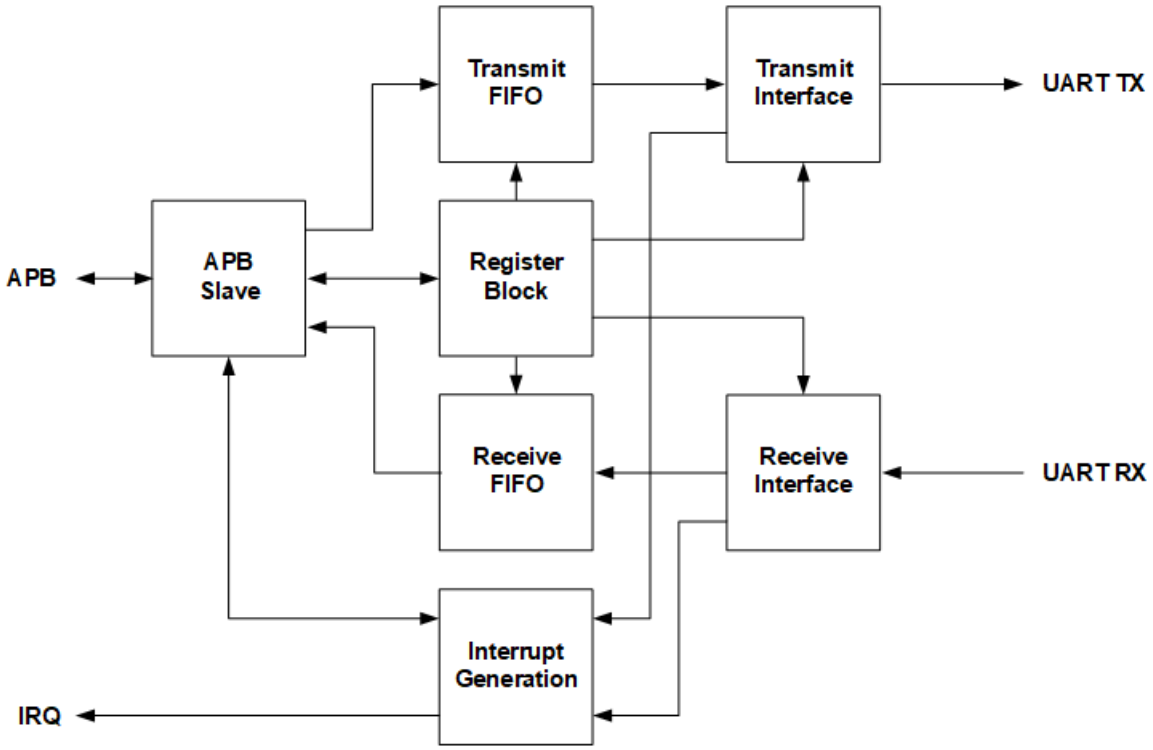

Figure 37. UART Block Diagram

19.1 Features

The Universal Asynchronous Receiver/Transmitter (UART) includes features shown in Figure 37 and listed below.

There are four (4) Universal Asynchronous Receiver/Transmitter (UART) instances on the Apollo510B SoC. The UART Module includes the following key features:

- Operates independently, allowing the MCU to enter a low power sleep mode during communication
- 32 x 8 transmit FIFO and 32 x 12 receive FIFO to reduce MCU computational load
- Programmable baud rate generator capable of achieving a maximum rate of 3 Mbps
- Fully programmable data size, parity, and stop bit length
- Programmable hardware flow control
- Support for full-duplex and half-duplex communication
- Supports DMA (half-duplex mode only)
- Loop-back functionality for diagnostics and testing

NOTE

To be able to receive data reliably at 3 Mbps baud rate on any of the UARTs, the UART clock source must be set to the SYSPLL by setting the UARTn_CR_CLKSEL = PLL_CLK. Also when the baud rate is set higher than 1.5 Mbps, the PCLK for the UART in use must be set to always on by setting the MCUCTRL_D2ASPARE_UARTnALWAYSON bit. When any of bits 22 to 25 of this register is set, it forces the PCLK clock enable for UART0 to UART3, respectively, to be always on.

To receive at baud rates lower than 3 Mbps, it is not necessary to set this bit or to use the SYSPLL as the UART's clock source.

NOTE

Since UART DMA is only supported in half-duplex mode, two UART instances are required (one for TX and one for RX) to support full-duplex DMA. In this full-duplex mode, the TX instance should be configured to use 2 stop bits and the one for RX should use 1 stop bit setting. The external UART TX needs to use 2 stop bits setting.

19.2 Functional Overview

Each UART converts parallel data written through the APB Subordinate port into serial data which is transmitted to an external device. It also receives serial data from an external device and converts it to parallel data, which is then stored in a buffer until the CPU reads the data.

The UART Module includes a programmable baud rate generator which is capable of operating at high baud rates. An interrupt generator optionally sends interrupts to the CPU core for transmit, receive and error events.

Internally, the UART Module maintains two FIFOs. The transmit FIFO is 1-byte wide with 32 locations. The receive FIFO is 12-bits wide with 32 locations. The extra four bits in the receive FIFO are used to capture any error status information that the Apollo510B SoC needs to analyze.

NOTE

In accordance with the PC16550 UART specifications, the CTS interrupt triggers (when enabled) if the state of the CTS input changes from low to high or from high to low. Additionally, if the CTS input is high during the initialization and enabling of the UART, the CTS interrupt will be triggered. Software should handle such interrupt events appropriately.

19.3 Additional Information

Please refer to the UART registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

20. Universal Serial Bus (USB)

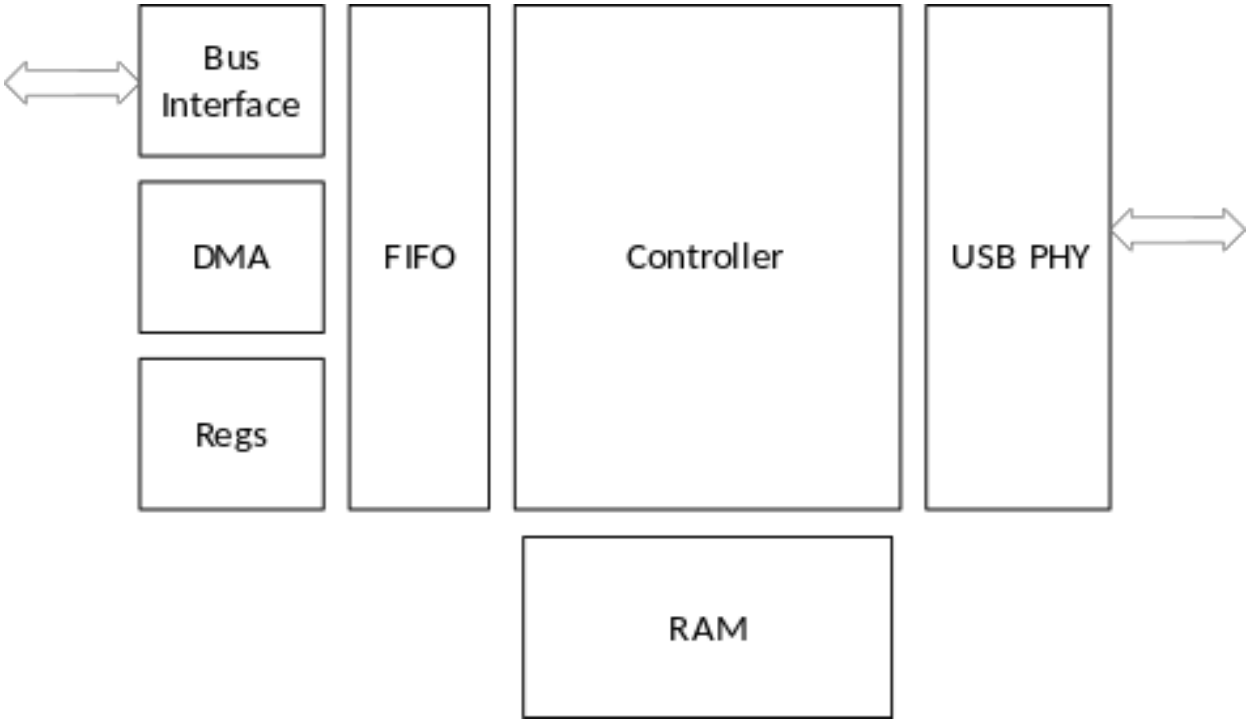

Figure 38. USB Block Diagram

20.1 Features

The Universal Serial Bus (USB) Subsystem includes features shown in Figure 38 and listed below.

- USB 2.0 FS/HS Device Mode
- Dynamic FIFO sizing: 4 kB total FIFO
- IN endpoints: 5
- OUT endpoints: 5
- IN bulk packet splitting supported
- OUT bulk packet combining supported
- Concurrent DMA supported for all IN/OUT BULK endpoints
- Soft connect/disconnect supported
- Suspend mode
- Supported classes
  - Communication Device Class (CDC)
  - Mass Storage Class (MSC)
  - Device Firmware Upgrade (DFU) Class
  - Human Interface Device (HID) Class
- Charging Support
  - Battery Charging 1.2 (BC1.2) supported for battery charger detection
  - Selected 3rd-party proprietary charger detection supported

20.2 Functional Overview

The USB subsystem provides support for USB 2.0 Full Speed (12 Mbps) and High Speed (480 Mbps) interface. This interface is primarily used for bulk data transfer, firmware updates and charging detect.

The USB controller supports up to 5 IN / 5 OUT endpoints plus 1 control. The FIFO sizing for each endpoint is dynamically configurable up to 4 kB, with the restriction that IN and OUT port sizing must be up to half the total FIFO size. The controller also supports DMA transfers to/from system memory.

The Apollo510B SoC has an integrated USB 2.0 PHY with support for Suspend Mode operation. Battery charger detection is supported within the PHY to enable battery charge algorithm execution and control of the external battery charge / power management IC. The charger detection supports Battery Charging Specification 1.2 (BC1.2) as well as the majority of proprietary (non-BC1.2 standard) chargers.

ERRATUM NOTICE

An output pulse on the D+ line while VDDUSB0P9 and/or VDDUSB33 are/is rising may be interpreted by a host as a connect event immediately followed by a disconnect one, causing the host USB SW to report about the unexpected disconnect from Apollo510. Such a report/message could be safely ignored for the USB-compliant hosts which would attempt USB device re-enumeration. An enumeration attempt performed when all USB power rails are stable succeeds.

See “ERR031: USB: Induced D+ output pulse may cause unintended disconnect” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

20.3 Power States

The USB subsystem supports power states as shown in Figure 39 and described below.

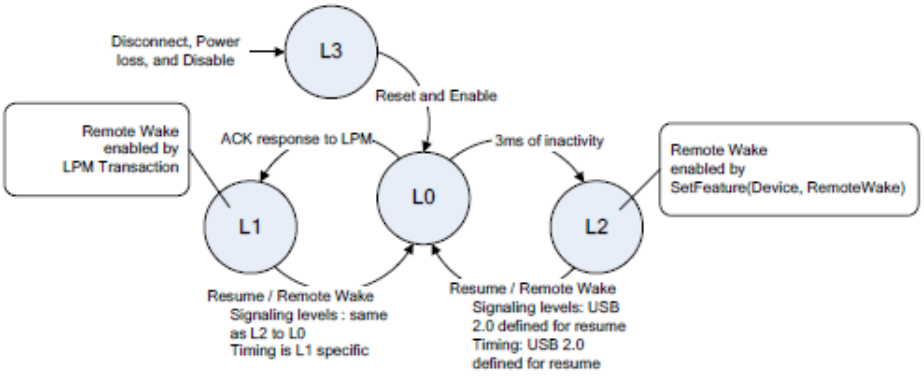

Figure 39. USB Power States Transitioning Diagram

L0 (On)

In this state, the port is enabled for propagation of transaction signaling traffic. A port in L0 is either actively transmitting or receiving data (L0-Active) or able to do so but not currently transmitting or receiving information (L0-Idle). While in this state Start-of-Frame (SOF) packets are issued by the host at a rate corresponding to the speed of the client device (1ms for full-speed, 125?s for high-speed). Note, the host transmits keep-alives or the USB 2.0 hub translates some SOFs into keep alives if the device connected on the downstream port is a Low-speed device. The line state during L0-Active and L0-Idle vary according link speed as does the mechanism by which the host detects device hot-removal (e.g. during SOF phase for high-speed devices). Entry to L0 is via reset or resume signaling (either from L1 or L2).

L1 (Sleep)

The L1 (Sleep) state is not supported on the Apollo510B SoC.

L2 (Suspend)

This is the formalized name for USB 2.0 Suspend, see Section 7.1.7.6 in the USB 2.0 specification. Entry to L2 is nominally triggered by a command to a hub or host port to transition to suspend, at which point the port ceases repeating signaling down the port (and may transition the port out of high-speed mode). The device discovers the suspend condition via observing 3ms of inactivity. The resultant line state is either Low or Full-speed idle. L2 also imposes power draw requirements (from VBUS) on the attached device. Exit from this state is via remote wake, resume signaling, reset signaling or disconnect.

L3 (Off)

In this state, the port is not capable of performing any data signaling. It corresponds to the powered-off, disconnected, and disabled states. The L3 state is transitioned to when the Apollo510B SoC receives an assertion or deassertion of the “PowerOK” signal from the Power Management / Charger IC.

20.4 Hardware Design Guidelines

The following sub-sections provide design guidelines for the use of the USB Controller and PHY. Please consult the USB section of the Electricals for voltage, power and timing requirements of the PHY.

20.4.1 Battery Charger Detection

Charger detection capabilities are as follows:

- Dedicated Charging Port (DCP) as per Battery Charging Specification Version 1.2 (BC1.2)
- Charging Downstream Port (CDP) as per BC1.2
- Standard Downstream Port (SDP) as per BC1.2
- Custom Charger

Not supported and/or non-applicable BC 1.2 features are listed below.

- OTG device
- Accessory Charger Adapter (ACA)
- ACA-Dock
- SuperSpeed Consideration
- Personal System 2 (PS2) - PHY DP/DM pads do not tolerate 5V

20.4.1.1 Battery Charger Detection during USB Connection

Charger detection during USB connection follows the flow shown in Figure 40.

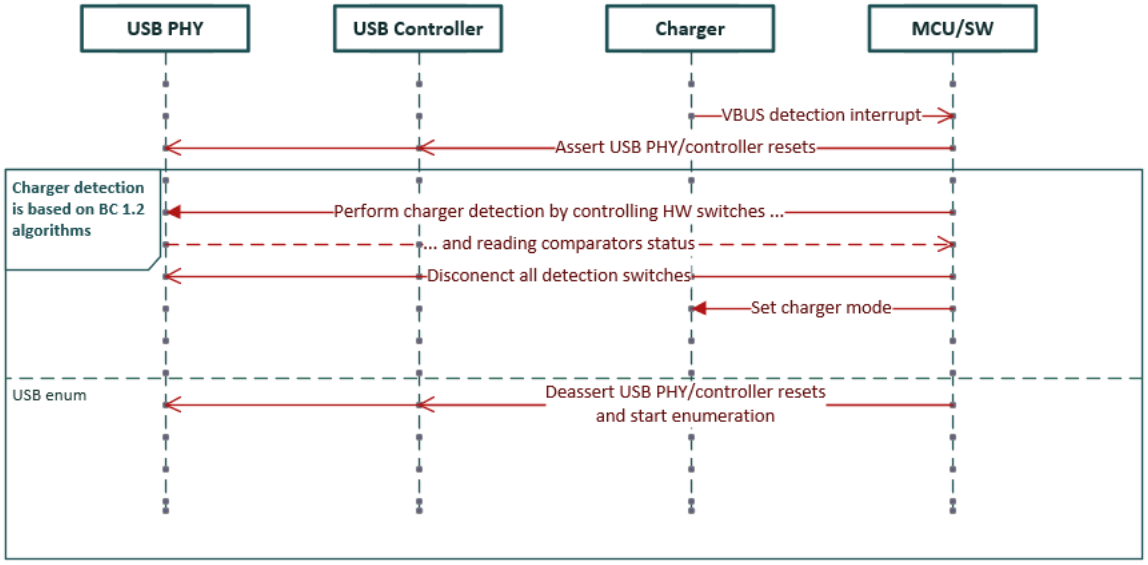

Figure 40. Charger Detection in USB Connection Flow

The charging detection algorithm in Figure 41 is based on the BC 1.2 specification. Weak Battery Algorithm (Figure 42) and Good Battery Algorithm (Figure 43) should be implemented in an interrupt-driven manner to take full advantage of the device's power saving features. Note that debouncing software timers and their interrupts are not shown in the diagram for clarity, but must be implemented according to BC 1.2 specification.

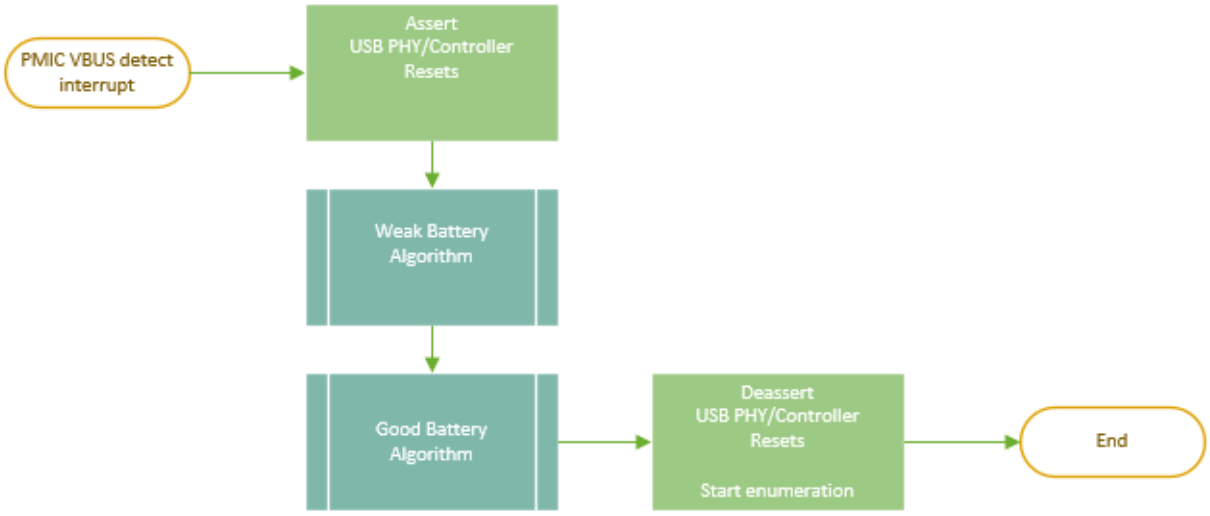

Figure 41. Charging Detection Algorithm

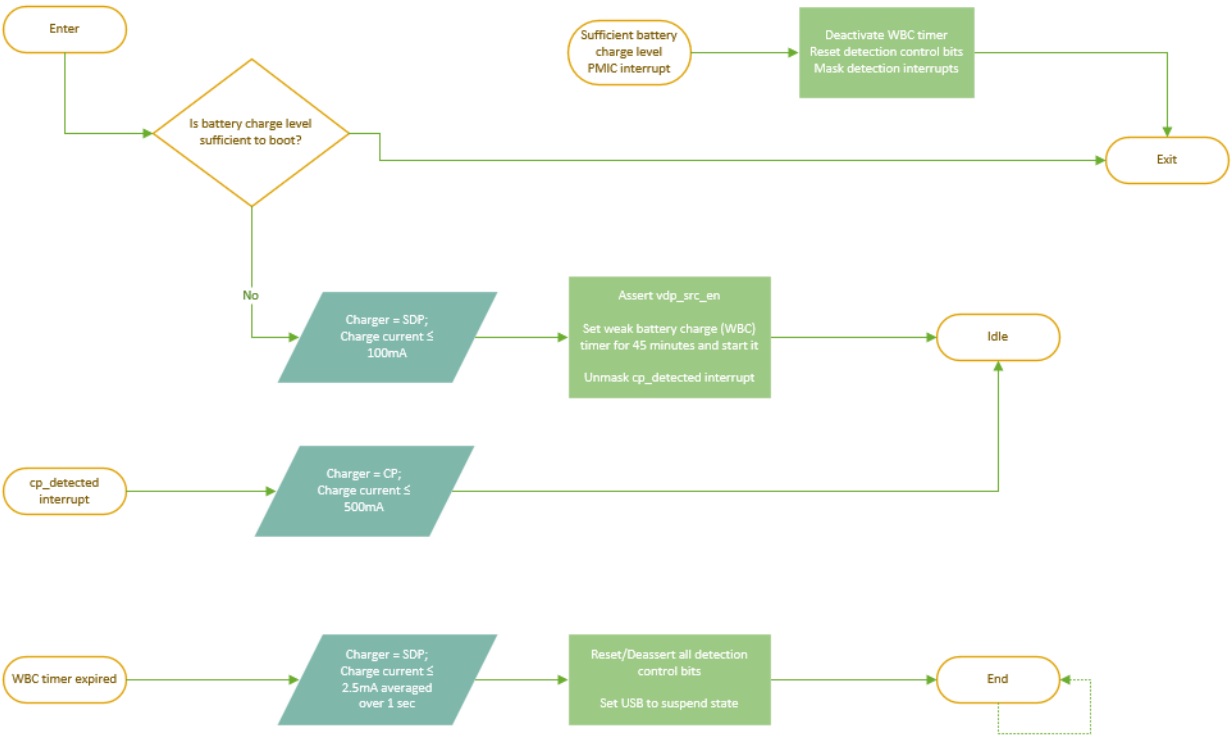

Figure 42. Interrupt-driven Weak Battery Algorithm

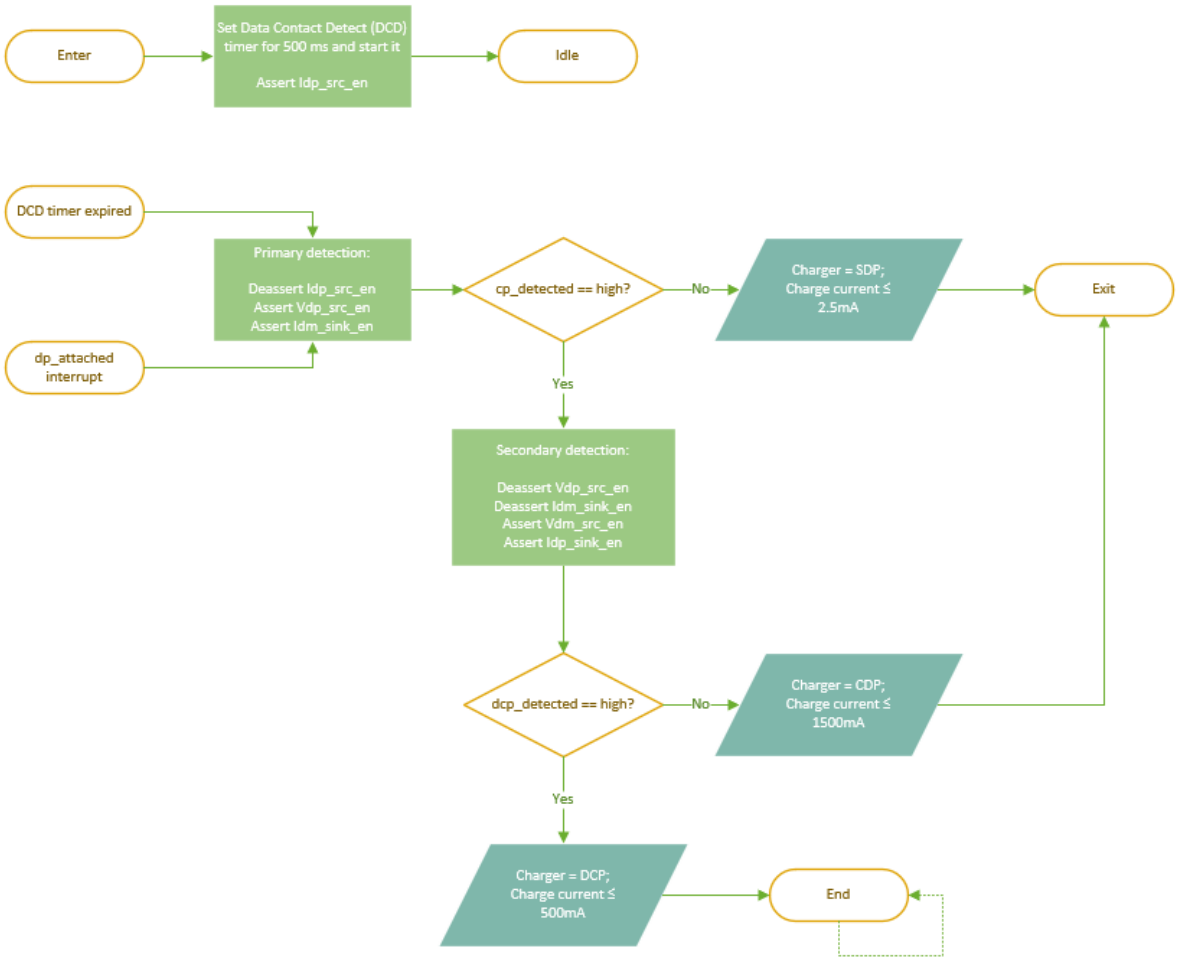

Figure 43. Interrupt-driven Good Battery Algorithm

Charger detection algorithms should take into account timings between assertion/deassertion control signal and status signal change as shown in Figure 44.

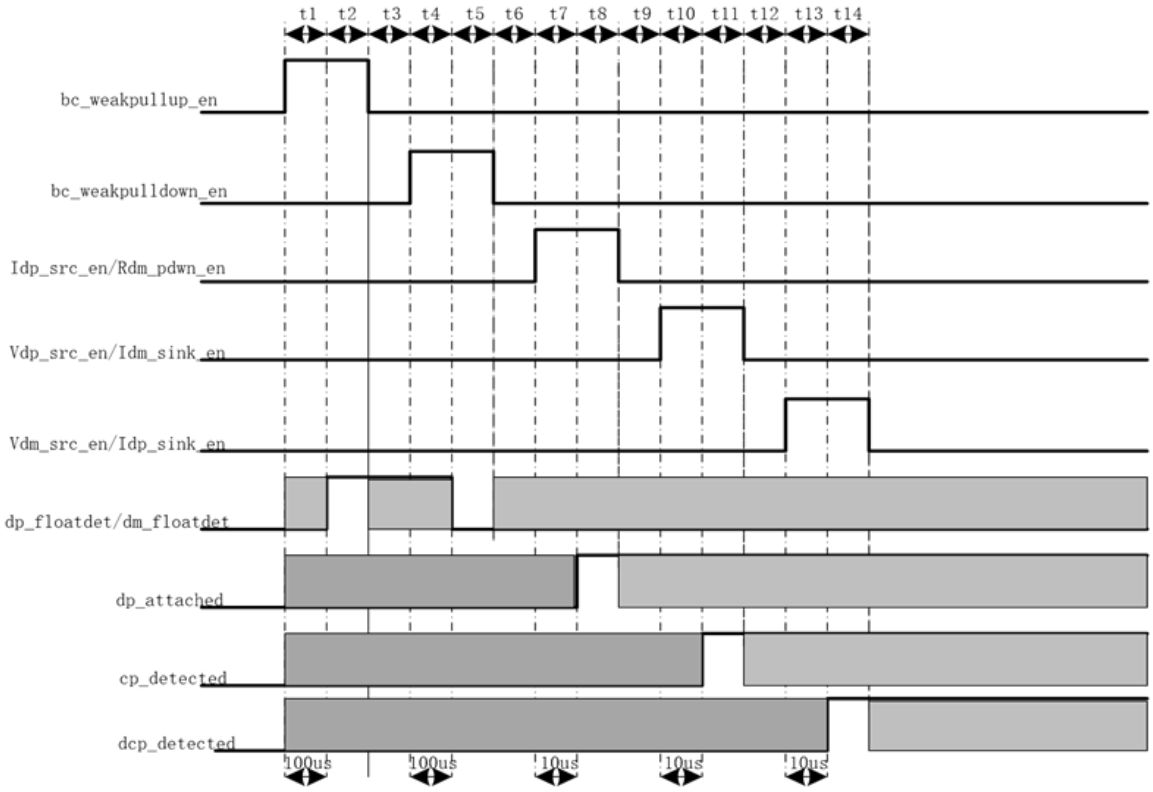

Figure 44. Battery Charging Sequence

20.4.2 System Power Sequencing for USB

The power sequence for the relevant power supplies is contingent on the PHY(s) used in the system. The sections below cover the case for the USB PHY and addresses the proper sequence which includes powering the VDDUSB33 (3.3 V) and VDDUSB0P9 (0.9 V) supplies.

Refer to the USB PHY section in the Electricals for supply voltage specifications.

Powering 3.3 V and 0.9 V rails from the external VBUS-sourced PMIC optimizes the Apollo510B SoC platform power consumption.

See “Power Sequencing” on page 214.

ERRATUM NOTICE
When VDDUSB33 is powered while VDDUSB0P9 is not powered, up to 34 mA may be consumed by the USB PHY. This situation should be avoided as it could lead to unnecessary current draw. However, if this scenario is unavoidable due to system design constraints, a 2 MΩ pull-down resistor can be added to both the D+ and D- lines to help mitigate the issue. This will bring the 3.3V leakage current below 1 µA when the 0.9 V rail is unpowered, minimizing potential power consumption. See “ERR046: USB: High leakage current in USB PHY” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

20.4.2.1 Recommended Termination of Unused Interface

1. USB data pads (USB0PP and USB0PN) left open
2. Both USB PHY power rails VDDUSB33 and VDDUSB0P9 connected to ground

WARNING
Connecting the VDDUSB0P9 power rail to ground while powering VDDUSB33 will cause permanent damage to the 0.9 V LDO.

20.4.2.2 Power Tree

The recommended power tree for this configuration is as follows:

1. VDDUSB33 and VDDUSB0P9 should be powered by an LDO with output discharge and ON/OFF control over I^2C or GPIO. It is recommended to source VDDUSB33 and VDDUSB0P9 power from USB VBUS to minimize system power consumption from the battery. Some examples of suitable standalone small form factor LDOs for USB PHY rails are as follows:
   - ST Micro LDBL20 in 0.47 x 0.47 x 0.22 mm STSTAMP™ package
   - ST Micro LD39130S in 0.69 x 0.69 x 0.5 mm CSP package
   - TI LP5910 0.74 x 0.74 x 0.4 mm DSBGA package
2. Required system power-on state: VDDUSB33 is OFF, VDDUSB0P9 is OFF

20.4.2.3 Recommended Interface ESD protection and Common Mode Filtering

ESD protection on the USB data lines, USB0PP and USB0PN, is required. An integrated CMF and TVS solution, such as the Nexperia PCMF1USB3B/C or Panasonic EXC-14CS900H, is recommended.

If the design achieves EMC compliance without CMF on the USB data lines, then a TVS-only solution, such as the TI ESD122DMXR, may be used.

20.4.2.4 USB VBUS Detection

The SoC has no 5V-tolerant pins. Therefore, it relies on the external circuit for getting VBUS power OK (VBUS connected) status. The recommended solution is to connect PMIC/charger VBUS_OK output to interrupt-capable GPIO pin.

20.4.2.5 USB Handling in AmbiqSuite SDK

1. The USB initialization routine in the AmbiqSuite SDK should be used to enable Suspend State by setting the ENABLE bit of the USB_CFG0 Register of the USB Controller.
2. To minimize power in the USB Suspend State, the software should turn off the FS differential receiver in the Suspend ISR. This may be done by clearing bit 1 of the USB PHY register at offset 0x10. The Resume ISR requires powering on the FS receiver by setting this same bit.
3. An API for registering a given GPIO as the USB VBUS interrupt source is available in the SDK. It can be configured with various triggering options such as level/edge and positive/negative edge triggering).
4. Please refer to the AmbiqSuite's HAL functions (i.e., am_hal_usb.c) for USB PHY initialization, shutdown, tuning and other procedures.

20.4.3 Suspend State Power Consumption

USB PHY power consumption in Suspend State when both 3.3 V and 0.9 V are supplied is as specified in the Electricals.

20.4.4 USB Data Line Filtering

A TVS on the data lines, USB0PP and USB0PN, is required. An integrated CMF and TVS solution, such as the Panasonic EXC-14CS900H, is recommended. If the design achieves EMC compliance without CMF on the USB data lines, then a TVS-only solution, such as the TI ESD122DMXR, may be used.

20.4.5 Charger Detection and USB Enumeration Requirements

The SoC has no 5V-tolerant pins. Therefore, it relies on the external circuit for getting VBUS power OK (VBUS connected) status. The recommended solution is connecting PMIC/charger VBUS_OK output to an interrupt-capable GPIO pin.

20.5 Additional Information

Please refer to the USB and USBPHY registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

21. Secure Digital Input Output (SDIO)

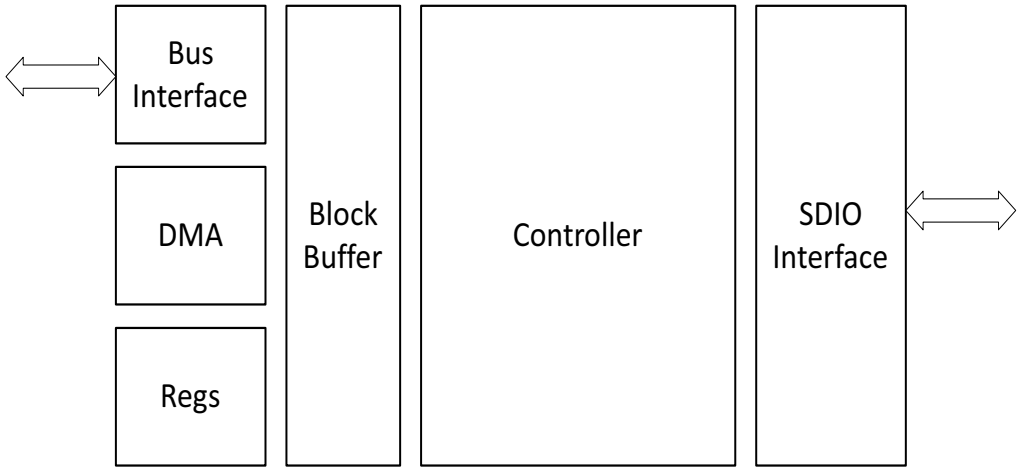

Figure 45. SDIO Block Diagram

21.1 Features

The Secure Digital Input Output (SDIO) Module includes features shown in Figure 45 and listed below.

- 2x SDIO Controller instances allowing for concurrent eMMC and SDIO interface support
- SDIO card specification Version 3.0
- Host clock rate variable between 0 and 96 MHz
- Up to 48 MB/s data rate using 4 parallel data lines (SDR50/DDR50 mode)
- Transfers data in 1-bit and 4-bit SD modes
- Transfers data in SDR50 or DDR50 modes
- SDIO0 transfers data in 8-bit eMMC mode for 96 MB/s maximum transfer rate; SDIO1 transfers data in 4-bit eMMC mode for 48 MB/s maximum transfer rate
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity
- Variable-length data transfers
- Performs Read Wait Control, Suspend/Resume operation

21.2 Functional Overview

The SDIO host controller provides support for higher bandwidth device transfer. A typical application is for Wi-Fi IC connectivity. The SDIO controller supports up to 2 kB block buffering as well as dedicated DMA controller support to provide maximum host offload. The DMA algorithm supported is the Advanced DMA version 2 (ADMA2) which allows for flexibility in memory allocation. The controller interface supports a programmable DLL to allow for timing tuning for optimal windowing.

NOTE

The default value for the Card Detect (CD) and the Write Protect (WP) pins for both SDIO channels is GPIO127, which is also the (only) GPIO option for the SDIO1 DATA2 line. The SDIFnWP and SDIFnCD fields in the GPIO_SDIF0CDWP and GPIO_SDIF1CDWP registers must be set (before SDIO channel initialization) so as not to cause any pin conflict.

21.3 Additional Information

Please refer to the SDIO registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

22. Display Subsystem

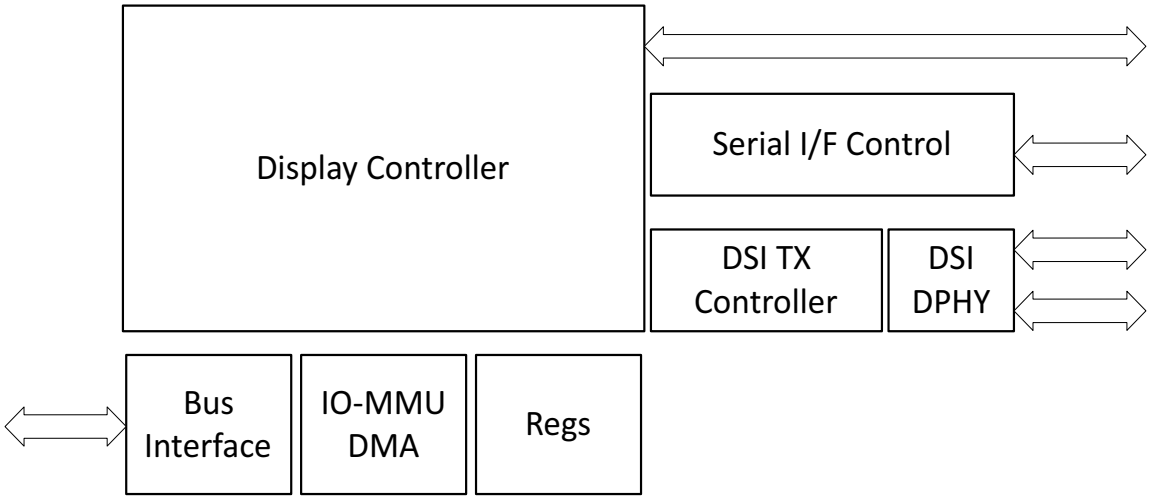

Figure 46. Block Diagram of the Display Subsystem

22.1 Features

The Apollo510B SoC's integrated Display Subsystem contains several smart tools and functions to compose multiple graphics, improving image quality and contributing significantly to the reduction of the SoC power consumption. The Display Controller supports composition features, a wide range of display interfaces and advanced proprietary framebuffer compression technology. The core is designed to lessen the workload of the Graphics Processing Unit (GPU) and the host processor (CPU), and minimize the memory bandwidth in GPU-less systems. Multiple layers can be scaled, clipped, positioned and composed on the final display by overlaying graphics, cursors or application windows, with or without transparency.

The Display Subsystem is represented by the block diagram shown in Figure 46. Its key features include the following:

- Supports up to 1920 x 1080[1] resolution
- Up to 24-bit color
- Configurable stride/pitch enabling panning and clipping
- Up to 4 layers with alpha blending and scaling
- Multiple Input Surface formats
  - RGBX8888, XRGB8888 (32-bit)
  - RGB888 (24-bit mode)
  - RGBX5551, RGB565 (16-bit)
  - YUYV (32-bit, 2 pixels / word)
  - RGB232, LUT8, Grayscale (8-bit)
- Display Interfaces
  - 3-4 Wire SPI (Serial Peripheral Interface) bus
  - DualSPI (Dual Serial Peripheral Interface) bus
  - QuadSPI (Quad Serial Peripheral Interface) bus
- Compressed frame buffer and frame buffer decompression support:

1. Ignoring frame-rate, the Display Controller can support up to 1920 x 1080 resolution. The resulting frame rate at any particular resolution depends upon display interface speed, bus-fabric bandwidth and complexity of the graphics assets and related operations. Typically a resolution of 640 x 480 at 60 frames per second can be supported for most applications.

  - 4-bit
  - 6-bit (with/without Alpha)
  - 12-bit (with/without Alpha)
- Adaptive sync
- Adaptive brightness
- Powerful composition
- Programmable size, offset and format per layer
- Programmable stride/pitch enabling panning and clipping
- Per layer palette
- Global or per layer gamma correction
- Dithering for better results on 18-bit displays
- Programmable event interrupt
- Smart DMA support

NOTE

24-bit, 16-bit and 8-bit color formats work only when the frame buffer resolution is set to a multiple of 4, as is the case for the startX and startY coordinates for all TSC color formats. If the panel resolution is not a multiple of 4, then the frame buffer should be sized slightly larger than the panel resolution to make it a multiple of 4.

Since the frame buffer size is just the input of each layer, the start position of the layer as the output to the panel can be any desired value. And since it is just the frame buffer that must be larger, the desired output resolution is not restricted (i.e., can be a partial frame output or full frame of resolution that is less than the frame buffer size).

ERRATUM NOTICE

Failures in the form of incorrect data being read or the AXI bus hanging occur if the Display Controller (DC) is fetching data from multiple memories for its multiple layers and one of the memories is MRAM.

See “ERR002: DC: Limitations with MRAM AXI bus read transactions” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

Incorrect pixel data output order from the DC SPI causes color distortion in the displayed image. This is a reported NemaDC hardware erratum: Not supported: 24-bit/16-bit/8-bit color formats with layer size which is not a multiple of 4.

See “ERR039: DC: Incorrect pixel data output order from the DC SPI” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

NOTE
The DPI-2, Parallel RGB and DBI-Type B display interfaces are not offered on the Apollo510B SoC.

22.2 Functional Overview

The Display Subsystem offers flexibility for system designers to select the number of layers, functionality of composition modules and processing methods tailored to their requirements. This section provides a high-level description of the main functions, the proprietary TSC™ compression/decompression, the supported color formats, and the display format interfaces.

22.2.1 Display Controller Functionality

The Display Controller is a dedicated hardware block allowing the offload of display interface and control functions. The configuration register file controls the operation of the display controller. Timing parameters are programmable and data are fetched for each layer by a dedicated DMA engine. Additional functions include:

- Gamma adjustment
- Dithering application
- RGB conversion to YCbCr/YUV format

22.2.1.1 Layer Overlays

The Display Controller supports up to four layers sourced from different memory regions. Each layer can have separate color modes, alpha blending, and filtering attributes. The main control registers for each layer is the LAYERn_MODE (n = 0-3) registers. Optionally, the layer can support scaling.

22.2.1.2 Blending Modes

During blending process, a translucent foreground color (current layer) with a background color (previous layer) are combined and a new blended color is produced. Foreground color's translucency may range from completely transparent to completely opaque. If the foreground color is completely transparent, the blended color will be the background color and if the foreground color is completely opaque, the blended color will be the foreground color. When the translucency ranges in between, the blended color is computed as a weighted average of the foreground and background colors.

22.2.1.3 Palette/Gamma Correction

The Display Controller supports palette color mapping and gamma correction per layer.

22.2.1.4 Dithering

Dithering is the process of degrading the color image with a method that tries to produce better results than information truncation. Dithering is used to create the illusion of "color depth" in images with a limited color palette. In a dithered image, colors that are not available in the palette are approximated by a diffusion of colored pixels from within the available palette. The human eye perceives the diffusion as a mixture of the colors within it.

22.2.2 Display Serial Interface (DSI) Controller

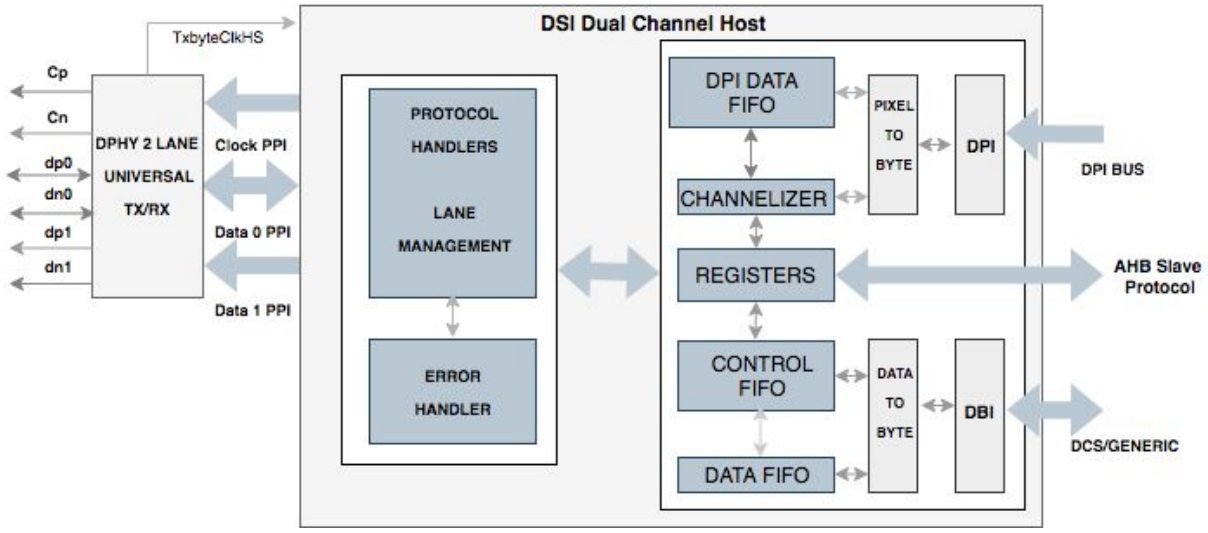

Figure 47. DSI Controller Block Diagram

22.2.2.1 DSI Features

The DSI on the Apollo510B SoC supports the features listed below.

- Standard D-PHY transceiver compliant to MIPI Specification
- Type1 display architecture in command mode
- Can be programmed to support command mode in single channel mode
- Generic read and write commands
- Low power data transfer for both DBI/generic
- Pixel formats of types:
  - 16bpp [RGB565]
  - 18bpp [RGB666] and [Loosely packed RGB666]
  - 24bpp [888RGB]
- Recovery from contention
- Timers and recovery schemes to come out of mode fault errors
- Watchdog timers to monitor D-PHY activity:
  - in low power mode
  - in high speed mode
  - during turn-around
- Interrupts to report protocol errors and expiry of timers
- Programmable device initialization timers
- Programmable maximum return packet size command
- One or two PHY data lanes
- DBI interface for DCS commands and data transfer
- Data lane switching to low power mode during idle time
- Signals tearing effect
- Ultra low power mode switching
- Bus turn-around
- EOT disabling capacity to suit backward compatible displays
- Clock stop enabling feature during idle time
- Added support for deskew calibration
- Supported display resolutions:

- QCIF
- QVGA
- CIF
- VGA

The DSI is compliant with the following standards:

- DSI MIPI specification for Display Serial Interface (Version 1.3.1)
- D-PHY standard MIPI specification (Version 1.2)
- MIPI Alliance Standard for Display Bus Interface version 2.0 0
- MIPI Alliance Standard for Display Command Set Version 1.02

NOTE
The DSI supports Type 1 display architecture in command mode only. Video Mode is not supported.

22.2.2.2 Functional Overview

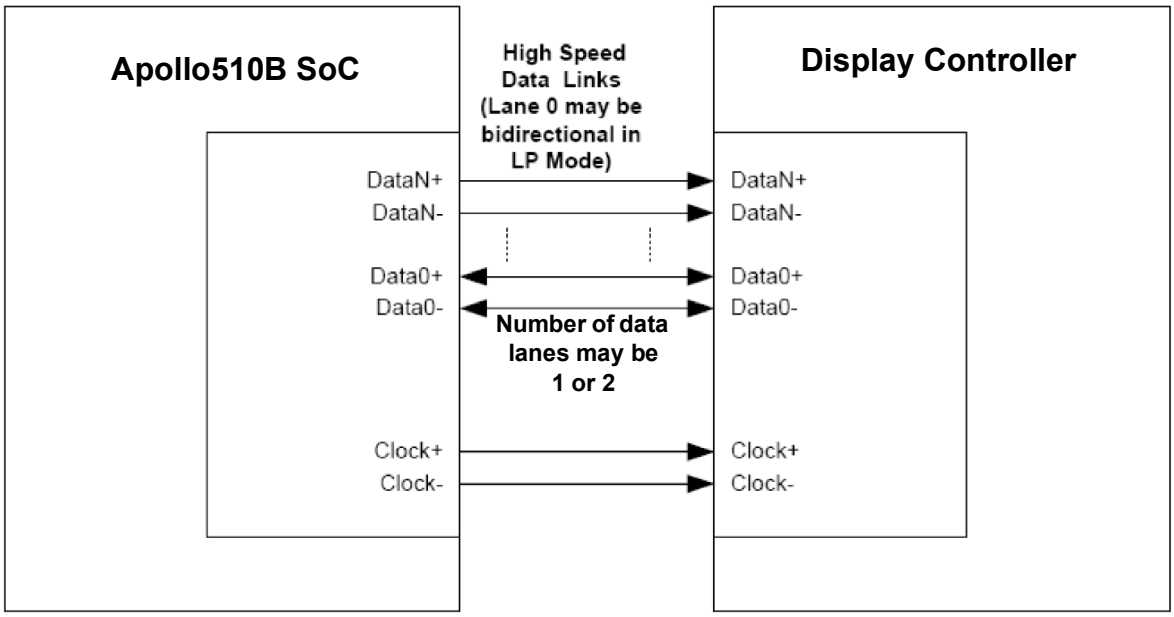

Figure 48. Display Serial Interface Bus with DSI Devices

The Display Serial Interface bus (DSI) on the Apollo510B SoC is a type of serial bus that enables transfer of data between a transmitter device and a receiver device. The DSI device has a point-to-point connection with DSI devices via D-PHYs as shown in Figure 48.

The DSI module is configured to specify the interface and provide a connection between the MCU and a peripheral such as a display module. It is built on existing MIPI Alliance standards by adopting pixel formats, controlling pins and a command set specified in DCS standards.

Please refer to the DSI registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

The D-PHY's data lane signals are transferred point-to-point as differential signals using two signal lines and a clock lane. There are two signaling modes: high speed mode that operates at a rate of 768 Mbps per lane (1.536 Gbps total) and a low power mode (LP) that operates at a lower transfer rate of 10 Mbps. The mode is set to a low power mode and a stop state at start up / power up. Depending on the desired data transfer type, the lanes switch between high and low power modes. High speed data transfer is unidirectional and data transfer at low speed can be unidirectional or bidirectional.

DSI devices operate in a layered fashion. There are 4 layers identified both at receiver and transmitter ends. Figure 49 shows the layers in the DSI data transfer model.

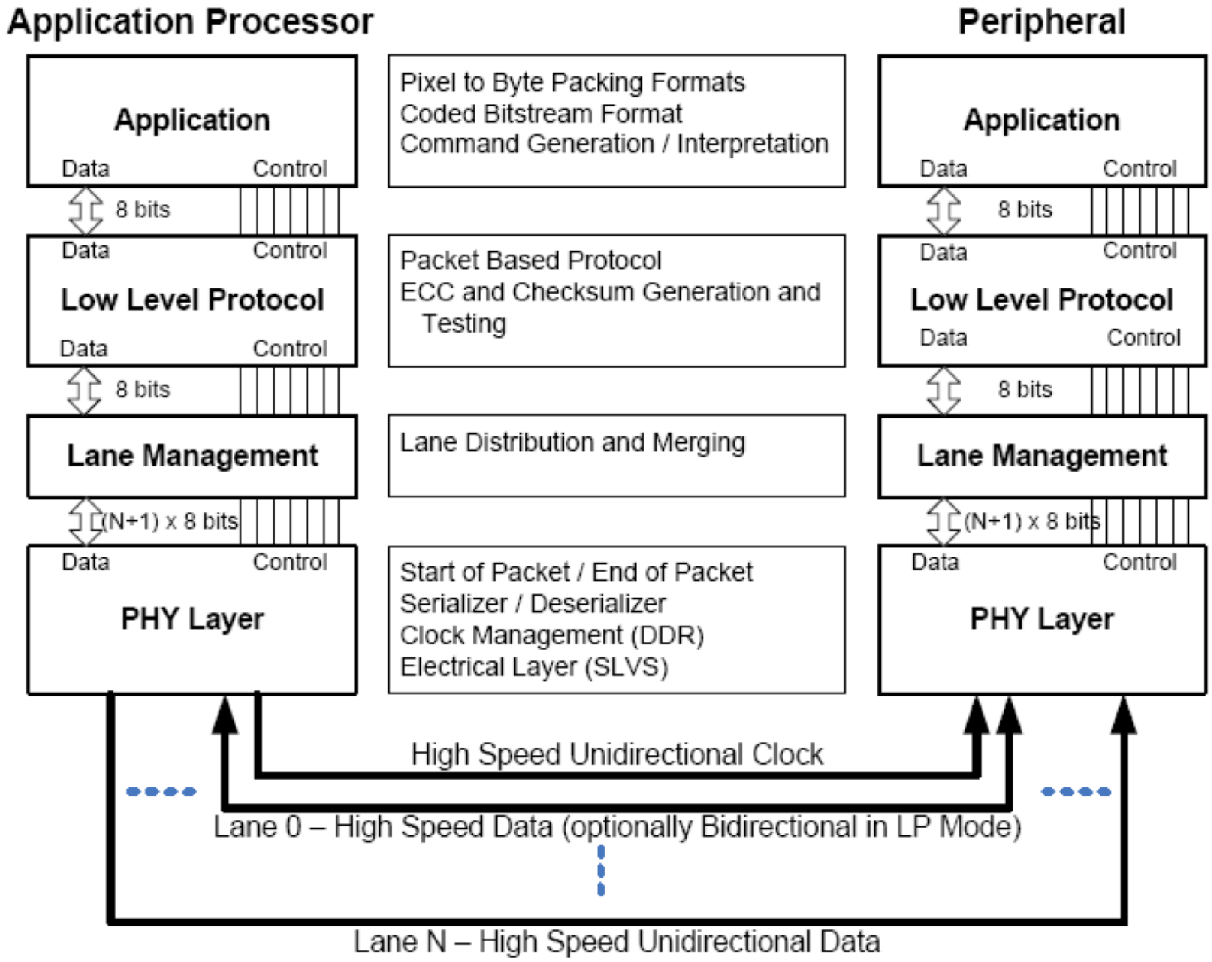

Figure 49. Layers in the DSI Data Transfer Model

PHY Layer: An embedded electrical layer that sends and detects start-of-packet and end-of-packet signaling on the data lanes. It has a serializer and deserializer unit to dialogue with the PPI / lane management unit. It also has clock divider unit to source and receive clock during different modes of operation.

PPI / Lane Management Unit: This layer does the lane buffering and distributes the data in the lanes as programmed in a round robin manner and also merges them to stream line to the LLP/ PLI unit.

PLI / Low Level Protocol Unit: This layer packetizes as well as depacketizes the data with respect to channels, frames, colors and line formats. There is an ECC generator and corrector unit to recover the

data free from errors in the packet headers. It has a CRC checker or CRC generator unit to pack the payload data with CRC checksum bits for payload data protections.

Application: This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module.

22.2.2.3 Hardware Design Guidelines

The following sub-sections provide design guidelines for the use of the Apollo510B SoC's DSI PHY.

22.2.2.3.1 System Power Sequencing for DSI TX Interface

The following sub-sections cover the DSI TX interface (D-PHY) and addresses the proper power sequence which includes powering the VDD18 supply. Refer to the Recommended Operating Conditions section in the Electricals for VDD18 supply voltage specifications.

22.2.2.3.1.1 DSI PHY Power Tree

The recommended power tree for this configuration is as follows:

1. VDD18 is powered by LDO rails with output discharge and ON/OFF control over I^2C or GPIO.

The following power-on (default) state is allowed: VDD18 is OFF.

> NOTE
>
> On earlier revisions of Apollo510B SoC, powering VDD18 without powering the DSI TX/D-PHY internal power rails results in uncontrolled current leakage to VDD18 and may lead to long-term reliability issues. This uncontrolled current leakage to VDD18 has been resolved in Apollo510 version B2. Therefore turning power on and off to VDD18 in the initialization sequence reduces to:
>
> 1. Power on VDD18 and VDDF_DSIPHY_SW in any order.
> 2. Configure DSI TX to desired mode.

22.2.2.3.1.2 DSI TX Initialization and Shutdown Sequences

Please refer to the AmbiqSuite's HAL functions (i.e., am_hal_dsi.c) for DSI PHY initialization, shut-down and other procedures.

22.3 Additional Information

Please refer to the Display Controller and DSI registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

23. Graphics Processing Unit (GPU)

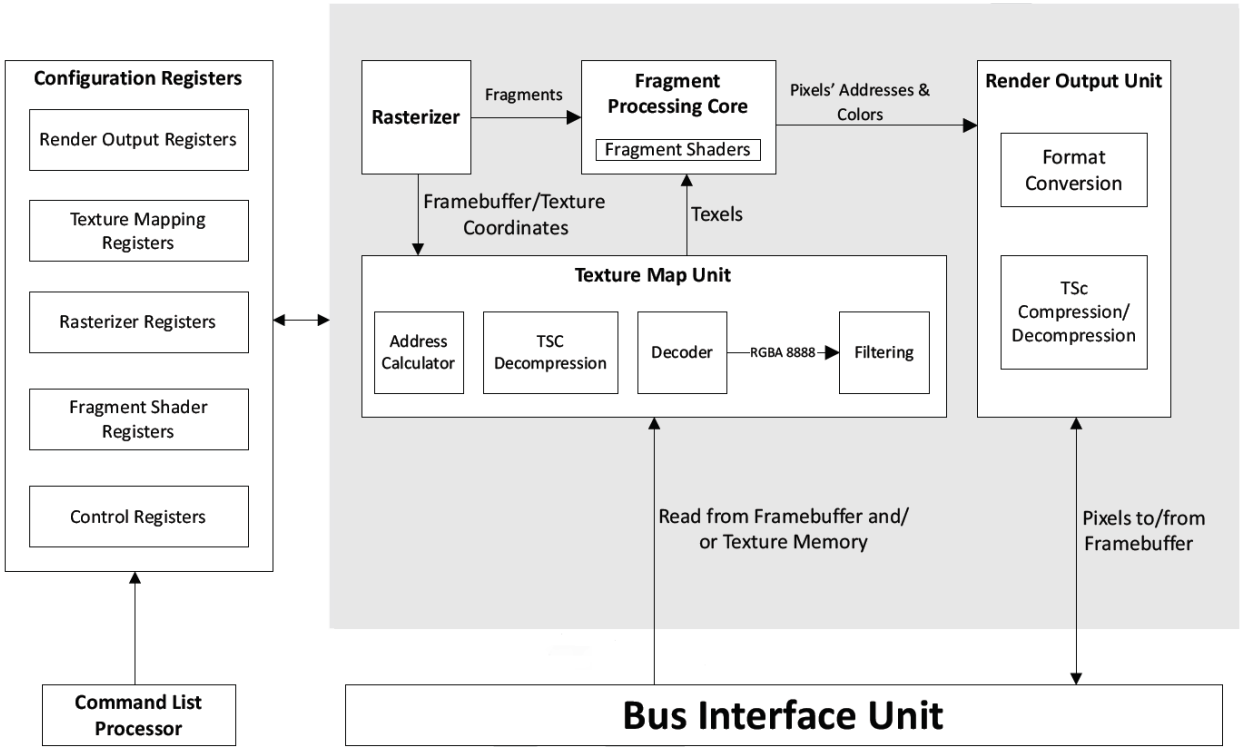

Figure 50. GPU Block Diagram

23.1 Features

The GPU Module is depicted in Figure 50. The Graphics Subsystem provides the following features:

- Fully programmable VLIW-based engine
- Fixed point functional units
- Command list based DMAs to minimize CPU overhead
- Compression schemes:
  - 4-bit
  - 6-bit (with/without Alpha)
  - 12-bit (with/without Alpha)
- 2.5D drawing
  - Pixel / Line drawing
  - Filled rectangles
  - Triangles (Gouraud Shaded)
  - Quadrilateral
- Blit support
  - Rotation
  - Mirroring
  - Stretch (independently on x and y axis)
  - Source and/or destination color keying
  - Format conversions
- Color formats
  - 32/24/16/8 bit with or without Alpha
  - Grayscale

  - RGB
- Full Alpha blending
  - Programmable blending modes
  - Source/Destination color keying
- Anti-Aliasing support
- Dithering support
- Image transformation
  - 2.5D Perspective Correct Projections
  - Texture mapping
    - Point sampling
    - Bilinear filtering
- Vector Graphics (VG) supported by dedicated hardware accelerator
- Configurable burst length
- Radial/Conical fill
- TrueType Font (TTF)
- Dedicated hardware to support the following:
  - Vertex Transformation
  - Bezier Tessellation
  - Bezier Draw

23.2 Functional Overview

The GPU on the Apollo510B SoC brings high quality graphics for user interfaces in a very small power budget. The GPU supports entry level IoT platforms, wearable and embedded devices with low cost and ultra-low power requirements and provides fluid graphics experience for a wide range of applications. Developers are able to create compelling Graphical User Interfaces (GUIs) and software applications with ultra-long battery life at a significantly lower cost for power-memory-area constrained IoT devices.

23.3 Additional Information

Please refer to the GPU registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

24. PDM-to-PCM Converter Module (PDM)

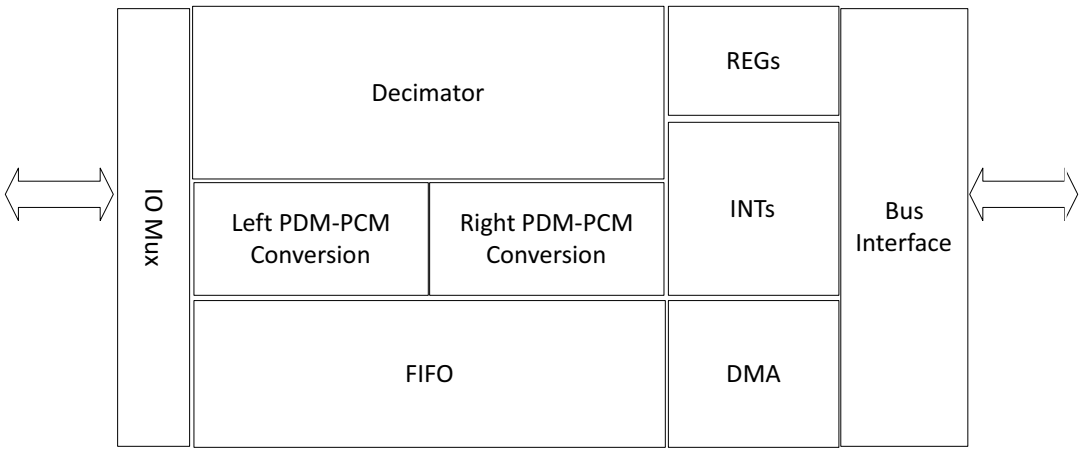

Figure 51. PDM Block Diagram

24.1 Features

The PDM-to-PCM Converter Module (PDM) includes features shown in Figure 51 and listed below.

- Support for up to 2 digital microphones
- Stereo/Mono Dual Mode PDM-to-PCM conversion
- 1-bit PDM (pulse-density modulated) input
- 24-bit PCM digital data output
- Programmable performance modes
- Supports ping-pong DMA jobs
- Supports digital microphone clock rate at 512 kHz, 750 kHz, 1.024 MHz, 1.536 MHz, 2.048 MHz, 3.072 MHz
- Supports granular decimation rates from 1x to 254x (64x typ)
- Supports PCM sampling rates of 8, 16, 24, 32 and 48 kHz
- PGA gain: -12 dB to +34.5 dB in 1.5 dB/step

ERRATUM NOTICE

In sampling configurations/frequencies with high Oversampling Ratio (> 128), the audio from the digital mic has distortion during speech. Most of the distortion comes from aliasing which is occurring during the PDM-to-PCM conversion. With a DMIC clock of 3.072 MHz and an OSR of 192, there is distortion from 1.6 kHz to 16 kHz. When OSR = 192, the MIC input signal bandwidth is greater than Fs/2 (= 16/2 = 8 kHz). If the mic input signal spectrum is wider than 8 kHz, a significant amount of aliasing occurs. Therefore, a maximum OSR of 128 is supported.

See “ERR021: PDM: High OSR causes aliasing and PDM mic distortion to occur during the PDM-to-PCM conversion” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

24.2 Functional Overview

The Apollo510B SoC supports 1x stereo PDM controller. The PDM controller features low power stereo/ mono PDM-to-PCM converter with register programming.

The PDM controller operates in dual mode (stereo or mono). In stereo mode, the controller converts 1-bit stereo pulse-density modulated (PDM) bit stream data from external digital microphones into 24-bit pulse-code modulated (PCM) data for base-band processing. In default operation, the PDM data sampled on the rising-edge of digital microphone clock is assumed to be left channel input, while data on the falling-edge is assumed to be right channel input. Optional channel swap is available through register setting. In mono mode, only the left channel PCM output is valid while the right channel output is zero (not toggling).

The PDM-to-PCM converter typically supports a data sampling rate of 16 kHz for voice applications. It is capable of supporting output sampling rates (Fs) of 8, 16, 24, 32 and 48 kHz at different manager clock conditions. After input sampling, the PDM data bits are fed into digital filters for data conversion and gain amplification.

DMA jobs may be ping-pong processed to allow software to pre-process and/or post-process one DMA job while hardware is processing another DMA job.

24.3 Additional Information

Please refer to the PDM registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

25. Low Power Analog Audio Interface

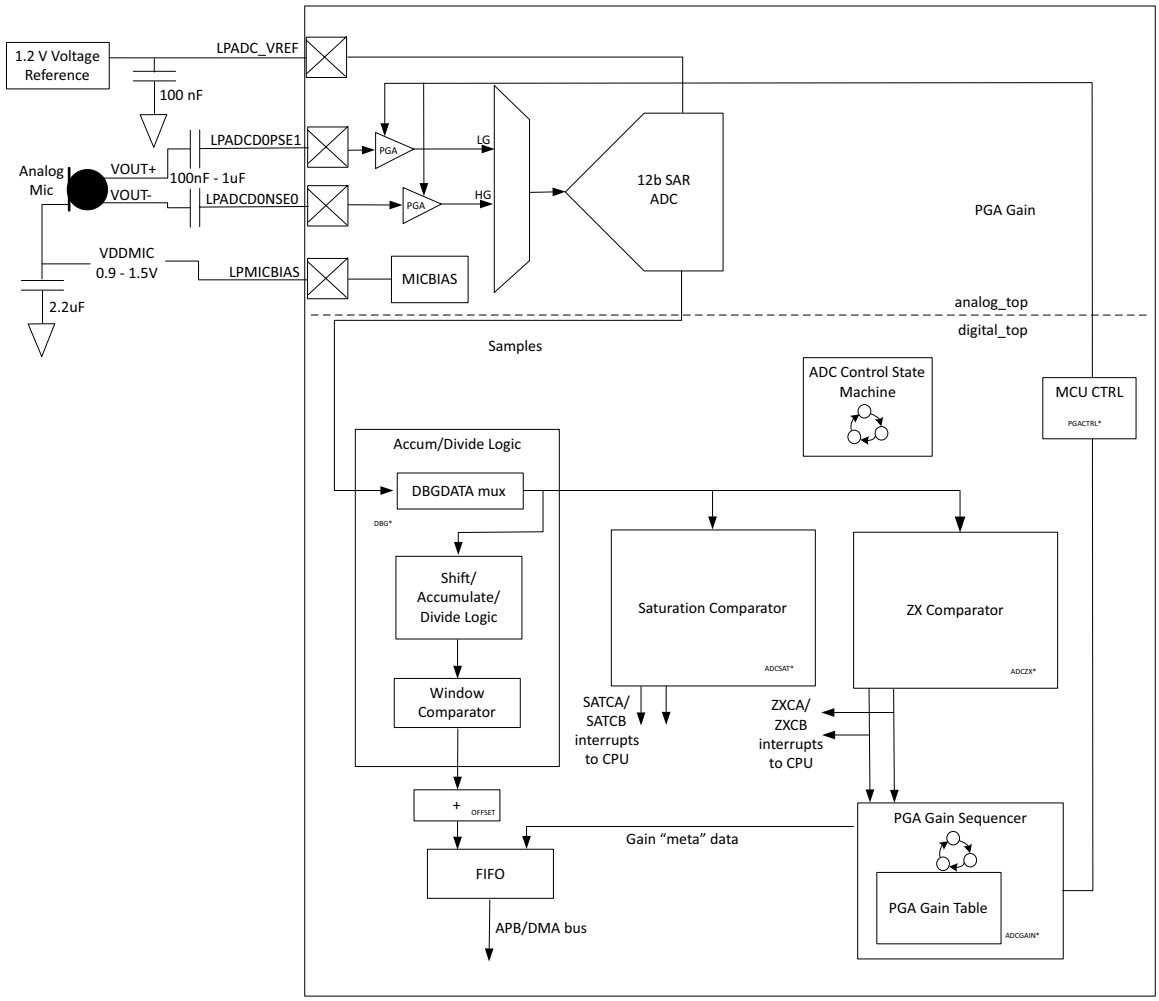

Figure 52. Low Power Analog Audio Interface Block Diagram

25.1 Features

The Low Power Analog Audio Interface is comprised of 2 channels of Programmable Gain Amplifiers (PGAs), 12-bit 2-channel Audio Analog-to-Digital Converter (AUDADC), and 1 low power microphone bias (MICBIAS) as shown in Figure 52.

Key features of the PGAs include:

- Programmable gain for AC-coupled audio inputs (20 Hz - 20 kHz) to drive AUDADC
- Audio inputs may be microphone or line inputs
  - Single Ended (SE)
  - Pseudo Differential (PD)
  - Fully Differential (FD)
- Full Scale Voltage
  - SE/PD: 0.5 Vrms
  - FD: 1 Vrms
- Gain steps supported: 0-24 dB in 0.5 dB increments

- Set input common-mode for active and sleep mode operation
- Implicit 2/3 attenuation to fit 1.2 V ADC full scale

Key features of the AUDADC include:

- Always-on operation
- Reconfigurable Successive Approximation Register (SAR) ADC
- 2 dedicated single-ended input channels (D0N/SE0, D0P/SE1) from two PGA sources
- Input Range: 0 V to 1.2 V
- Configurable automatic low power control between scans
- Configurable for 12-bit, 10-bit and 8-bit ADC Precision Modes
- Sampling rate up to 2.0 MS/s (12-bit Mode) & 2.8 MS/s (8-bit Mode)
- Configurable sampling time
- Uses 1.2 V external reference with internal buffer
- Single shot, repeating single shot, scan, and repeating scan modes
- Variable sample tracking time, configurable on per-slot basis
- User-selectable clock source for variable sampling rates
- Automatically accumulate and scale module for hardware averaging of samples
- 16-entry FIFO and DMA capability for storing measurement results and maximizing SoC sleep time
- Multiple Interrupt Support:
  - FIFO full
  - FIFO 75% full
  - Scan Complete
  - Conversion Complete
  - Window Incursion
  - Window Excursion
  - Various DMA-related notifications
- Window comparator for monitoring voltage excursions into or out of user-selectable thresholds
  - Unsigned mode support ONLY
- Supports signed data mode by way of AUDADC_ADCCFG_DATAFMT
- Settable sampling/tracking time per-slot
- ADC-internal trigger timer providing low-jitter periodic repeated triggers
- Additional delays configurable via AUDADC registers

Key features of MICBIAS include:

- MICBIAS provides user-programmable regulated (0.9 V to 1.5 V) supply to analog MEMS microphones
- Performance Summary:
  - 200 µA max load current with 2.2 µF capacitor
  - 560 nA quiescent current
  - Typical PSR (from VDDAUD)
    - 34 dB @ 1 kHz
    - 15 dB @ 20 kHz
    - Startup < 1 ms

25.2 Functional Overview

The always-on Audio ADC on the Apollo510B SoC is connected to 2 Programmable Gain Amplifier (PGA) channels. These gains are programmable gains and may be controlled by the ADC. Generally, the low-gain and high-gain path will maintain a fixed dB gain delta between them. The low gain parameter is adjusted depending on the amplitude of the incoming audio signal and this, in turn, also adjusts the high gain parameter in the same fashion.

When the Audio ADC takes samples, they can be analyzed for a specific number of saturation events wherein the amplitude of the signal exceeds a programmable threshold. This can notify the CPU via interrupts such that it may take action to reduce the PGA gain. Saturation may be monitored on either low gain or high gain path, but not a mix of the two.

Additionally, these samples can be monitored for zero-crossings (ZX) such that when the signal crosses this configurable sample region, gain parameters may be automatically updated. This is done in order to reduce the likelihood of pops or clicks as gains are adjusted. There is also an “immediate” gain update mode in which the gains will be updated immediately following the upcoming scan (a full set of conversions). As with saturation detection, ZX may be monitored on either both low gain or both high gain paths, but not a mix of the two. The ZX monitor may also provide per-channel interrupts. This can be useful to let the CPU know when a ZX gain update is about to occur.

To help avoid the potential of a varying gain making it difficult to process the sampled audio, the low-gain parameter which was used for the specific sample is encoded and packed along with high gain/low gain pairs of up to 12-bit samples in each 32-bit word. Initially, samples may be taken using only the low-gain path, reducing power consumption (“LP” mode). Then, once a keyword or voice is detected, the audio ADC may be switched into “MED” mode, which enables sampling on the high-gain paths as well.

Otherwise, the AUDADC is an instance of the general purpose ADC.

NOTE

The AUDADC can be configured for High Performance (Telco) mode or Low Power (Always On) mode. In High Performance mode, the PLL should be configured to provide a 48 MHz source clock by setting the MCUCTRL_PLLMUXCTL_AUDADCPLLCLKSEL register to PLL, with AUDADC_CFG_CLKSEL set to OFF.

In Low Power mode, the low power HFRC_48MHz clock source should be used by setting the AUDADC_CFG_CLKSEL to HFRC_48MHz.

The recommended sampling rate for both modes is 16 kHz for best performance.

ERRATUM NOTICE

If an AUDADC register access is attempted when the clock source connection has been removed, the MCU will hang. If the AUDADC is on and any loss-of-clock condition occurs, this can result in a CPU hang.

See “ERR001: AUDADC: MCU hangs when attempting to configure the AUDADC with disabled clock” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

25.3 Additional Information

Please refer to the AUDADC registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

26. Inter-IC Sound (I^2S)

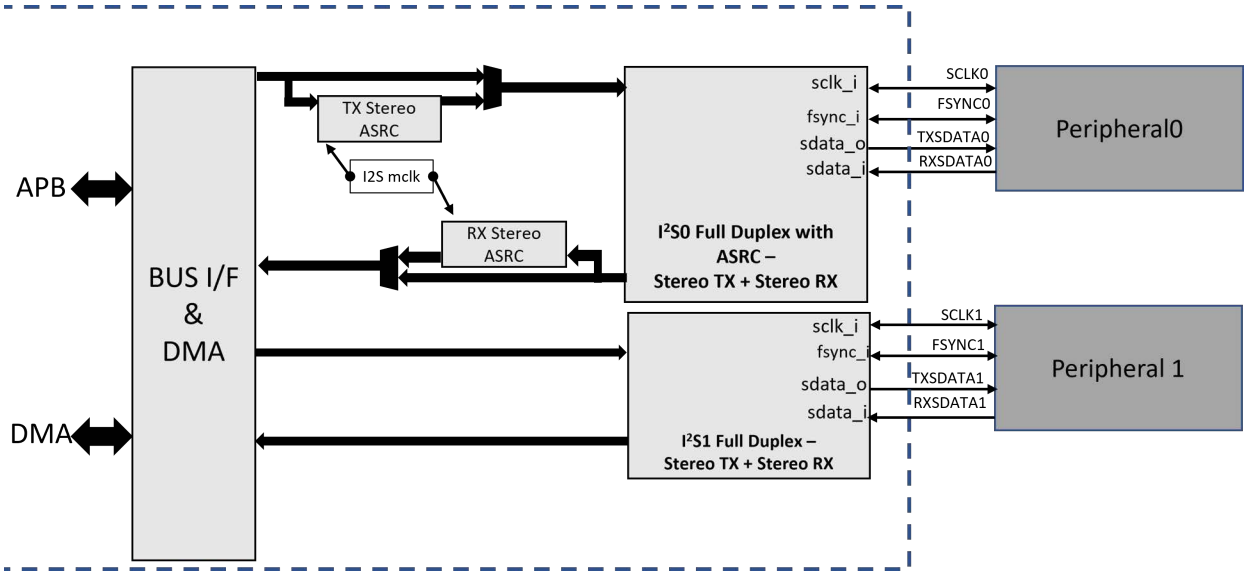

Figure 53. I^2S Block Diagram

26.1 Features

The Inter-IC Sound (I^2S) module includes features shown in Figure 53 and listed below.

- Inter-IC audio streaming interface
- Modes
  - I^2S Philips mode
  - I^2S right-justified and left-justified serial audio format modes
  - Time Division Multiplexing (TDM) mode
- Audio sample sizes of 8, 16, 24 and 32 bit
  - TDM has tremendous flexibility for framing and bit width
- 2x instances of full-duplex I^2S (stereo TX + stereo RX) using shared CLK & FS
- Manager and subordinate
- Supports ping-pong DMA jobs
- Optional Asynchronous Sample Rate Conversion (ASRC) on subordinate I^2S channels (I2S0 only)
  - Sample size: 24 bits (for internal processing, but accepts 8, 16, 24 or 32 bits)
  - Supported sampling rates: 8, 16, 24, 32, 44.1 and 48 kHz
  - Maximum down conversion of 1.95.1
  - Maximum up conversion of 1:7
  - Fixed FSYNC:SCLK ratio of 64:1 required
  - Lower than -130 dB THD+N for common conversion ratios (when using 24-bit samples)
- 1 to 8 Channel TDM interface

26.2 Functional Overview

The Apollo510B SoC supports two I^2S controllers. I2S0 supports manager or subordinate and I2S1 supports full duplex manager mode. Various modes and sample rates are supported to provide flexible audio data processing. DMA is supported to enable efficient transfer of data to/from SRAM. I2S0 also supports a configurable Asynchronous Sample Rate Converters (ASRC) capable of supporting stereo transmit and/or receive when configured as a subordinate device. DMA jobs can be ping-pong processed to allow software to pre-process and/or post-process one DMA job while the hardware is processing another DMA job.

ERRATUM NOTICE

The I2S does not set an error flag, TXDMASTAT_TXDMAERR or RXDMASTAT_RXDMAERR, or generate an error interrupt when a DMA error occurs. This error condition could cause the DMACPL logic to not work properly, and it may occur even when the DMACPL bit gets set.

See “ERR042: I2S: Error flag is not set when a DMA error occurs” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

26.3 Additional Information

Please refer to the I^2S registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

27. Voltage Regulator Module

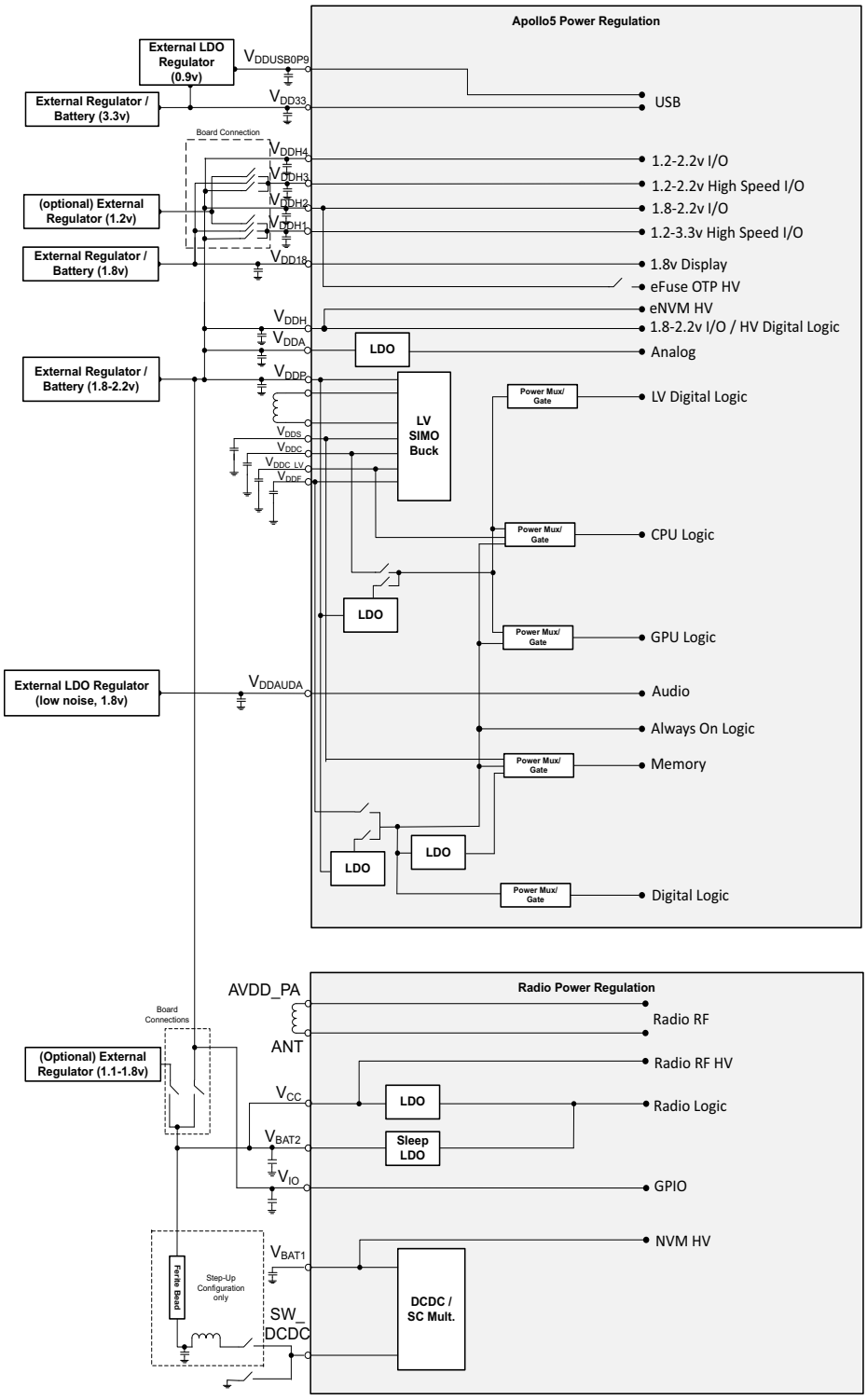

Figure 54. Block Diagram for Voltage Supplies and Regulation on Apollo510B SoC

27.1 Features

The voltage supplies and regulation subsystem includes features shown in Figure 54 and listed below.

- Down-converts and efficiently regulates the VDD supply voltage
- Optimized for low power environments
- Includes single-inductor/multiple-output SIMO Buck with ultra-low quiescent current
- SIMO Buck sources primary supplies for the core and memory domains
- Prevents drop out of regulated voltages from the SIMO Buck
- Enters efficient ultra-low power mode automatically based on active system load current
- Low-dropout (LDO) linear regulator available for very low-power modes
- LDO offers a lower cost system solution

27.2 Functional Overview

The Voltage Regulator Module on the Apollo510B SoC down-converts and regulates the supply voltage, VDD, with extremely high efficiency. The SIMO Buck, which is a single-inductor/multiple-output design enabled via software, sources the primary supplies for the core and memory domains. It enables down-conversion from the power supply input (e.g., a battery or external regulator) at more than 80% efficiency. With ultra-low quiescent current, the SIMO Buck Converter is optimized for low power environments.

Upon enabling the SIMO Buck, it will be powered up and stabilized through hardware control. The SIMO Buck has an efficient ultra-low power mode that is entered automatically via hardware control based on active load current of the system.

For cost/area constrained designs, the SIMO Buck can be disabled and a low-dropout (LDO) linear regulator can be used in very low-power modes. In this configuration, the SIMO Buck will remain powered down. There is also a zero-length detect circuit to ensure the regulated voltages from the SIMO Buck do not drop out.

The LDO regulator can also be utilized to provide a lower cost system solution by eliminating the need for the external inductor required in buck mode. The VDDC and VDDF capacitors are still required for the internal LDO.

The SIMO Buck Converter and LDO of the Voltage Regulator Module are tightly coupled to the various low power modes in the Apollo510B SoC. When the device enters deep sleep mode, the Buck Converter switches into a low power mode to provide very high efficiency at low quiescent current.

NOTE
The falling slew rate of a supply cannot exceed 2 kV/s. Doing so will cause indeterminate device behavior. In addition, I/O on rails should not exceed VDDHn+0.3V before the rail in question exceeds VDDHn_min, as it may cause indeterminate behavior.

ERRATUM NOTICE
The SIMO Buck cannot be enabled automatically via INFO0. See “ERR015: Memory: SIMO Buck cannot be enabled via INFO0 setting” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

ERRATUM NOTICE

An automatic SIMO Buck transition mode, which is enabled by setting both PWRCTRL_TONCNTRCTRL register fields LPMODESWOVR and ENABLELPOVR to 0x1, causes the SIMO Buck to transition to active mode if there is an increase in load current, but otherwise stays in Low Power (LP) Mode. Once the SIMO Buck transitions into Active Mode in deep sleep mode, it periodically retries to go into LP Mode. The SIMO Buck can transition from LP to Active if the temperature change and load change are gradual. However, it cannot handle the transition if there is a rapid change in temperature or load current. Because of this limitation, production trims do not make use of SIMO Buck automatic mode transitioning, and it is recommended that these PWRCTRL bits remain cleared.

See “ERR025: PWRCTRL: SIMO Buck fails to transition from Active Mode to LP Mode” in the *Apollo510 SoC / Apollo510B SoC Errata List*.

27.3 Additional Information

Please refer to the voltage regulation and control registers in the MCUCTRL and PWRCTRL registers of the Apollo510B SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

28. Apollo510B SoC Package Pins

28.1 Pin Configuration

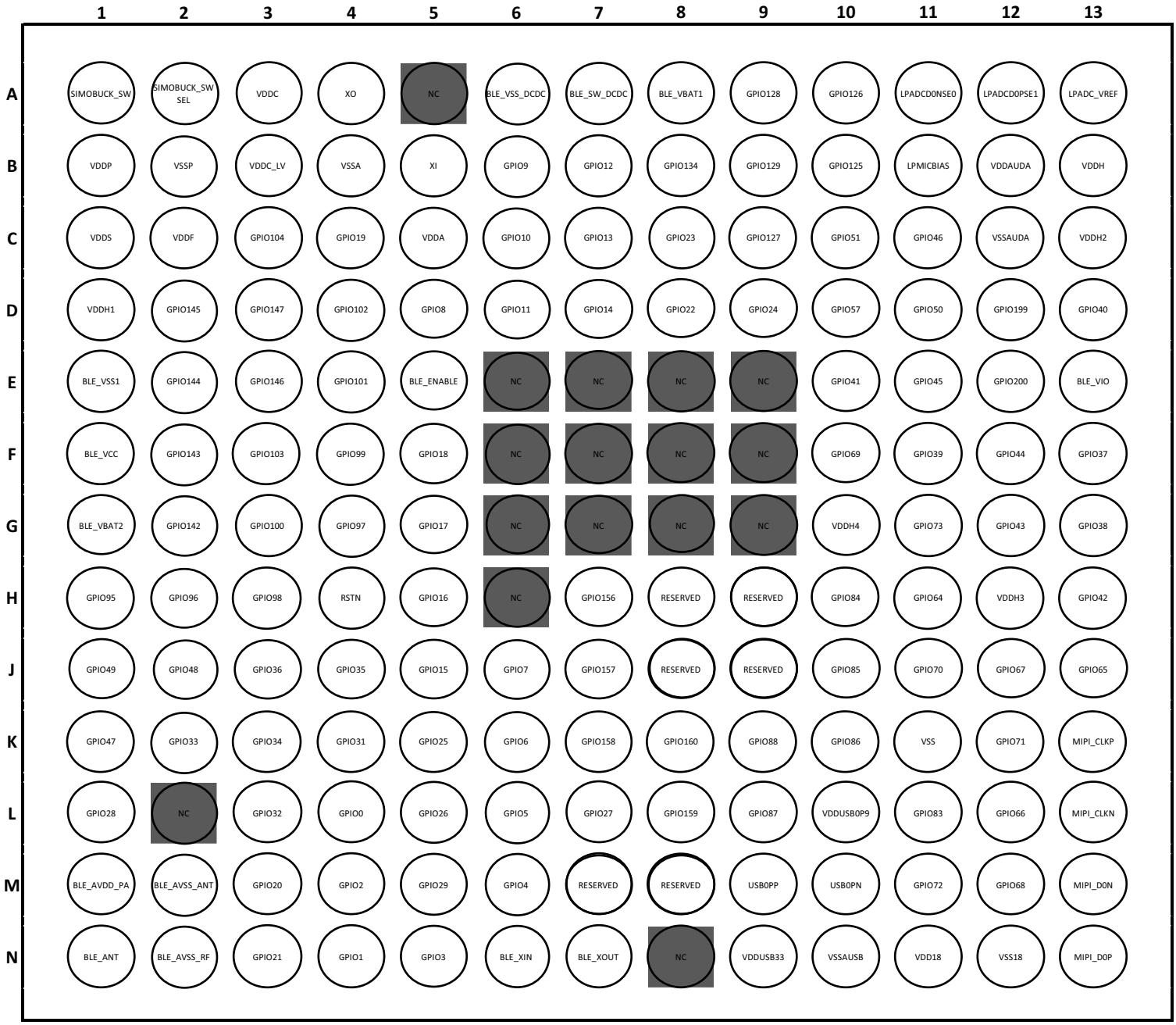

Figure 55. Apollo510B SoC BGA Pin Configuration Diagram - Top View

NOTE

All balls shaded gray are “no connects” and are not populated on the package.

NOTE

All balls labeled “RESERVED” must be unused and left unterminated.

NOTE

BLE_ENABLE on ball E5 must be terminated with a weak pull-down resistor.

NOTE

GPIO15 on ball J5 is used internally as a reference clock. It should be regarded as reserved and not be used. The ball must be left unterminated.

28.2 Pin Connections

The following table lists the external pins of the Apollo510B SoC and their available functions.

> NOTE
>
> The IOSFD module supports only the SPI interface. All function selection options in the below Pin List and Function Table related to IOSFD I2C interface should be ignored and not selected.

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
N11	-	-	VDD18	VDD supply for MIPI PHY	Power
C5	-	-	VDDA	Analog voltage supply	Power
B12	-	-	VDDAUDA	Analog Audio Voltage supply	Power
A3	-	-	VDDC	Core Buck converter VOUT	Power
B3	-	-	VDDC_LV	Core_LV Buck converter VOUT	Power
C2	-	-	VDDF	Mem Buck converter VOUT	Power
B13	-	-	VDDH	High voltage domain power supply	Power
D1	-	-	VDDH1	High voltage domain1 power supply	Power
C13	-	-	VDDH2	High voltage domain2 power supply	Power
H12	-	-	VDDH3	High voltage domain3 power supply	Power
G10	-	-	VDDH4	High voltage domain4 power supply	Power
B1	-	-	VDDP	VDD supply to I/O pads (Core)	Power
C1	-	-	VDDS	SRAM high voltage supply	Power
L10	-	-	VDDUSB0P9	USB 0.9v analog voltage supply	Power
N9	-	-	VDDUSB33	USB 3.3v voltage supply	Power
K11	-	-	VSS	Digital Ground for VDDF and PADS (Noisy) - (Previously called GNDD)	Ground
N12	-	-	VSS18	MIPI PHY Analog Ground	Ground
B4	-	-	VSSA	Analog Ground - Same as GNDA	Ground
C12	-	-	VSSAUDA	Analog Audio Ground	Ground
N10	-	-	VSSAUSB	USB PHY Analog Ground	Ground
B2	-	-	VSSP	Ground Connection for buck regs - Same as GNDP	Ground
A13	-	-	LPADC_VREF	LP ADC Reference Decap	Analog
A11	-	-	LPADCD0NSE0	LP Analog to Digital Converter SE0/DiffN IN0	Input
A12	-	-	LPADCD0PSE1	LP Analog to Digital Converter SE1/DiffP IN0	Input
B11	-	-	LPMICBIAS	LP Microphone Bias	Output
L13	-	-	MIPI_CLKN	MIPI DPHY Clock Lane N	I/O
K13	-	-	MIPI_CLKP	MIPI DPHY Clock Lane P	I/O
M13	-	-	MIPI_D0N	MIPI DPHY Data Lane 0N	I/O
N13	-	-	MIPI_D0P	MIPI DPHY Data Lane 0P	I/O

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
H4	-	-	RSTN	External reset input (aka nRST)	Input
A1	-	-	SIMOBUCK_SW	SIMO Buck converter inductor switch output	Power
A2	-	-	SIMOBUCK_SWSEL	SIMO Buck converter inductor switch input	Power
M10	-	-	USB0PN	The differential input/output signals of the PHY that support multiple modes. Depending on mode of operation they are either signaling 3.3V or 800mV differential.	Power
M9	-	-	USB0PP	The differential input/output signals of the PHY that support multiple modes. Depending on mode of operation they are either signaling 3.3V or 800mV differential.	Power
N1	-	-	BLE_ANT	BLE antenna	Analog
M1	-	-	BLE_AVDD_PA	BLE Analog PA VDD	Analog
M2	-	-	BLE_AVSS_ANT	BLE antenna analog ground	Analog
N2	-	-	BLE_AVSS_RF	BLE analog RF VSS	Analog
E5	-	-	BLE_ENABLE	BLE enable	Input
M8	-	-	Reserved	No Connect	I/O
M7	-	-	Reserved	No Connect	I/O
J9	-	-	Reserved	No Connect	I/O
J8	-	-	Reserved	No Connect	I/O
H9	-	-	Reserved	No Connect	I/O
H8	-	-	Reserved	No Connect	I/O
A7	-	-	BLE_SW_DCDC	BLE DCDC Switch	Analog
A8	-	-	BLE_VBAT1	BLE VBAT1	Analog
G1	-	-	BLE_VBAT2	BLE VBAT2	Analog
F1	-	-	BLE_VCC	BLE VCC	Analog
E13	-	-	BLE_VIO	BLE I/O Voltage	Analog
A6	-	-	BLE_VSS_DCDC	BLE DCDC VSS	Analog
E1	-	-	BLE_VSS1	BLE VSS	Analog
N6	-	-	BLE_XIN	BLE XTAL in	Analog
N7	-	-	BLE_XOUT	BLE XTAL out	Analog
B5	-	-	XI	32.768kHz crystal input	XT
A4	-	-	XO	32.768kHz crystal output	XT

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
L4	0	0	SWTRACECLK	Serial Wire Debug Trace Clock	Output
		1	SLFDSCK	SPI Subordinate Full Duplex clock	Input
		2	-	-	-
		3	GPIO0	General purpose I/O	I/O
		4	UART0TX	UART0 transmit output	Output
		5	UART1TX	UART1 transmit output	Output
		6	CT0	Timer/counter 0	Output
		7	NCE0	IOMSTR N Chip Select 0	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
N4	1	0	SWTRACE0	Serial Wire Debug Trace Output 0	Output
		1	SLFDMOSI	SPI Subordinate Full Duplex input data	Input
		2	SLFDWIR3	SPI Subordinate Full Duplex I/O pin for 3-wire	Bidirectional 3-state
		3	GPIO1	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART3TX	UART3 transmit output	Output
		6	CT1	Timer/counter 1	Output
		7	NCE1	IOMSTR N Chip Select 1	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	SLFD1WIR3	SPI Subordinate1 Full Duplex I/O pin for 3-wire	Output
		11	-	-	-
		12	-	-	-
		13	-	-	-
M4	2	0	SWTRACE1	Serial Wire Debug Trace Output 1	Output
		1	SLFDMISO	SPI Subordinate Full Duplex output data	Output
		2	TRIG1	ADC trigger input	Input
		3	GPIO2	General purpose I/O	I/O
		4	UART0RX	UART0 receive input	Input
		5	UART1RX	UART1 receive input	Input
		6	CT2	Timer/counter 2	Output
		7	NCE2	IOMSTR N Chip Select 2	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	SLFD1MISO	SPI Subordinate1 Full Duplex output data	Output
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
N5	3	0	SWTRACE2	Serial Wire Debug Trace Output 2	Output
		1	SLFDnCE	SPI Subordinate Full Duplex chip enable	Input
		2	SWO	Serial Wire Debug	Output
		3	GPIO3	General purpose I/O	I/O
		4	UART2RX	UART2 receive input	Input
		5	UART3RX	UART3 receive input	Input
		6	CT3	Timer/counter 3	Output
		7	NCE3	IOMSTR N Chip Select 3	Output
		9	-	-	-
		10	I2S1_SDIN	I2S1 Data input	Input
		11	-	-	-
		12	-	-	-
		13	-	-	-
M6	4	0	SWTRACE3	Serial Wire Debug Trace Output 3	Output
		1	SLFDINT	Configurable Subordinate Interrupt	Output
		2	32KHzXT	32kHZ from analog	Output
		3	GPIO4	General purpose I/O	I/O
		4	UART0RTS	UART0 Request to Send (RTS)	Output
		5	UART1RTS	UART1 Request to Send (RTS)	Output
		6	CT4	Timer/counter 4	Output
		7	NCE4	IOMSTR N Chip Select 4	Output
		9	I2S0_SDIN	I2S0 Data input	Input
		10	SLFD1INT	Configurable Subordinate Interrupt1	Output
		11	-	-	-
		12	-	-	-
		13	-	-	-
L6	5	0	M0SCL	I2C Manager 0 clock	Open Drain Output
		1	M0SCK	SPI Manager 0 clock	Output
		2	I2S0_CLK	I2S0 Bit clock	Bidirectional
		3	GPIO5	General purpose I/O	I/O
		4	UART2RTS	UART2 Request to Send (RTS)	Output
		5	UART3RTS	UART3 Request to Send (RTS)	Output
		6	CT5	Timer/counter 5	Output
		7	NCE5	IOMSTR N Chip Select 5	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K6	6	0	M0SDAWIR3	I2C Manager 0 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
		1	M0MOSI	SPI Manager 0 output data	Output
		2	I2S0_DATA	I2S0 Data	Bidirectional
		3	GPIO6	General purpose I/O	I/O
		4	UART0CTS	UART0 Clear to Send (CTS)	Input
		5	UART1CTS	UART1 Clear to Send (CTS) input	Input
		6	CT6	Timer/counter 6	Output
		7	NCE6	IOMSTR N Chip Select 6	Output
		9	I2S0_SDOUT	I2S0 Data output	Output
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
J6	7	0	M0MISO	SPI Manager 0 input data	Input
		1	TRIG0	ADC trigger input	Input
		2	I2S0_WS	I2S0 L/R clock	Bidirectional
		3	GPIO7	General purpose I/O	I/O
		4	UART2CTS	UART2 Clear to Send (CTS) input	Input
		5	UART3CTS	UART3 Clear to Send (CTS) input	Input
		6	CT7	Timer/counter 7	Output
		7	NCE7	IOMSTR N Chip Select 7	Output
		9	MNCE2_0	MSPI Manager 2 nCE 0 Signal	-
		10	MNCE3_1	MSPI Manager 3 nCE 1 Signal	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
D5	8	0	CMPRF1	Comparator reference 1	Input
		1	TRIG1	ADC trigger input	Input
		2	-	-	-
		3	GPIO8	General purpose I/O	I/O
		4	M1SCL	I2C Manager 1 clock	Open Drain Output
		5	M1SCK	SPI Manager 1 clock	Output
		6	CT8	Timer/counter 8	Output
		7	NCE8	IOMSTR N Chip Select 8	Output
		9	-	-	-
		10	I2S1_CLK	I2S1 Bit clock	Bidirectional
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
B6	9	0	CMPRF0	Comparator reference 0	Input
		1	TRIG2	ADC trigger input	Input
		2	-	-	-
		3	GPIO9	General purpose I/O	I/O
		4	M1SDAWIR3	I2C Manager 1 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
		5	M1MOSI	SPI Manager 1 output data	Output
		6	CT9	Timer/counter 9	Output
		7	NCE9	IOMSTR N Chip Select 9	Output
		9	I2S1_DATA	I2S1 Data	Bidirectional
		10	I2S1_SDOUT	I2S1 Data output	Output
		11	-	-	-
		12	-	-	-
		13	-	-	-
C6	10	0	CMPIN0	Voltage comparator input 0	Input
		1	TRIG3	ADC trigger input	Input
		2	MNCE0_0	MSPI Manager 0 nCE 0 Signal	-
		3	GPIO10	General purpose I/O	I/O
		4	M1MISO	SPI Manager 1 input data	Input
		5	MNCE2_0	MSPI Manager 2 nCE 0 Signal	-
		6	CT10	Timer/counter 10	Output
		7	NCE10	IOMSTR N Chip Select 10	Output
		9	DISP_TE	Display TE input	Input
		10	I2S1_WS	I2S1 L/R clock	Bidirectional
		11	-	-	-
		12	MNCE2_1	MSPI Manager 2 nCE 1 Signal	-
		13	-	-	-
D6	11	0	CMPIN1	Voltage comparator input 1	Input
		1	TRIG0	ADC trigger input	Input
		2	I2S0_CLK	I2S0 Bit clock	Bidirectional
		3	GPIO11	General purpose I/O	I/O
		4	UART2RX	UART2 receive input	Input
		5	UART3RX	UART3 receive input	Input
		6	CT11	Timer/counter 11	Output
		7	NCE11	IOMSTR N Chip Select 11	Output
		9	SLSCL	I2C Subordinate Half Duplex clock	Input
		10	SLSCK	SPI Subordinate Half Duplex clock	Input
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
B7	12	0	ADCSE7	Analog to Digital Converter SE IN7	Input
		1	TRIG1	ADC trigger input	Input
		2	I2S0_DATA	I2S0 Data	Bidirectional
		3	GPIO12	General purpose I/O	I/O
		4	UART0TX	UART0 transmit output	Output
		5	UART1TX	UART1 transmit output	Output
		6	CT12	Timer/counter 12	Output
		7	NCE12	IOMSTR N Chip Select 12	Output
		9	CMPRF2	Comparator reference 2	Input
		10	I2S0_SDOUT	I2S0 Data output	Output
		11	-	-	-
		12	-	-	-
		13	-	-	-
C7	13	0	ADCSE6	Analog to Digital Converter SE IN6	Input
		1	TRIG2	ADC trigger input	Input
		2	I2S0_WS	I2S0 L/R clock	Bidirectional
		3	GPIO13	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART3TX	UART3 transmit output	Output
		6	CT13	Timer/counter 13	Output
		7	NCE13	IOMSTR N Chip Select 13	Output
		9	SLnCE	SPI Subordinate Half Duplex chip enable	Input
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
D7	14	0	ADCSE5	Analog to Digital Converter SE IN5	Input
		1	TRIG3	ADC trigger input	Input
		2	-	-	-
		3	GPIO14	General purpose I/O	I/O
		4	-	-	-
		5	UART1RX	UART1 receive input	Input
		6	CT14	Timer/counter 14	Output
		7	NCE14	IOMSTR N Chip Select 14	Output
		9	-	-	-
		10	I2S0_SDIN	I2S0 Data input	Input
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
H5	16	0	ADCSE3	Analog to Digital Converter SE IN3	Input
		1	TRIG1	ADC trigger input	Input
		2	I2S1_CLK	I2S1 Bit clock	Bidirectional
		3	GPIO16	General purpose I/O	I/O
		4	-	-	-
		5	UART1RTS	UART1 Request to Send (RTS)	Output
		6	CT16	Timer/counter 16	Output
		7	NCE16	IOMSTR N Chip Select 16	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
G5	17	0	ADCSE2	Analog to Digital Converter SE IN2	Input
		1	TRIG2	ADC trigger input	Input
		2	I2S1_DATA	I2S1 Data	Bidirectional
		3	GPIO17	General purpose I/O	I/O
		4	-	-	-
		5	UART3RTS	UART3 Request to Send (RTS)	Output
		6	CT17	Timer/counter 17	Output
		7	NCE17	IOMSTR N Chip Select 17	Output
		9	I2S1_SDOUT	I2S1 Data output	Output
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
F5	18	0	ADCSE1	Analog to Digital Converter SE IN1	Input
		1	-	-	-
		2	I2S1_WS	I2S1 L/R clock	Bidirectional
		3	GPIO18	General purpose I/O	I/O
		4	UART0CTS	UART0 Clear to Send (CTS)	Input
		5	UART1CTS	UART1 Clear to Send (CTS) input	Input
		6	CT18	Timer/counter 18	Output
		7	NCE18	IOMSTR N Chip Select 18	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
C4	19	0	ADCSE0	Analog to Digital Converter SE IN0	Input
		1	-	-	-
		2	-	-	-
		3	GPIO19	General purpose I/O	I/O
		4	UART2CTS	UART2 Clear to Send (CTS) input	Input
		5	UART3CTS	UART3 Clear to Send (CTS) input	Input
		6	CT19	Timer/counter 19	Output
		7	NCE19	IOMSTR N Chip Select 19	Output
		9	I2S1_SDIN	I2S1 Data input	Input
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
M3	20	0	SWDCK	Software debug clock Input	Input
		1	TRIG1	ADC trigger input	Input
		2	-	-	-
		3	GPIO20	General purpose I/O	I/O
		4	UART0TX	UART0 transmit output	Output
		5	UART1TX	UART1 transmit output	Output
		6	CT20	Timer/counter 20	Output
		7	NCE20	IOMSTR N Chip Select 20	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
N3	21	0	SWDIO	Software data I/O	Bidirectional 3-state
		1	TRIG2	ADC trigger input	Input
		2	-	-	-
		3	GPIO21	General purpose I/O	I/O
		4	UART0RX	UART0 receive input	Input
		5	UART1RX	UART1 receive input	Input
		6	CT21	Timer/counter 21	Output
		7	NCE21	IOMSTR N Chip Select 21	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
D8	22	0	M7SCL	I2C Manager 7 Clk	Bidirectional Open Drain
		1	M7SCK	SPI Manager 7 Clk	Output
		2	SWO	Serial Wire Debug	Output
		3	GPIO22	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART3TX	UART3 transmit output	Output
		6	CT22	Timer/counter 22	Output
		7	NCE22	IOMSTR N Chip Select 22	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
C8	23	0	M7SDAWIR3	I2C Manager 7 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
		1	M7MOSI	SPI Manager 7 data out	Output
		2	SWO	Serial Wire Debug	Output
		3	GPIO23	General purpose I/O	I/O
		4	UART2RX	UART2 receive input	Input
		5	UART3RX	UART3 receive input	Input
		6	CT23	Timer/counter 23	Output
		7	NCE23	IOMSTR N Chip Select 23	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
D9	24	0	M7MISO	SPI Manager 7 data in	Input
		1	TRIG3	ADC trigger input	Input
		2	SWO	Serial Wire Debug	Output
		3	GPIO24	General purpose I/O	I/O
		4	UART0RTS	UART0 Request to Send (RTS)	Output
		5	UART1RTS	UART1 Request to Send (RTS)	Output
		6	CT24	Timer/counter 24	Output
		7	NCE24	IOMSTR N Chip Select 24	Output
		9	MNCE0_0	MSPI Manager 0 nCE 0 Signal	-
		10	MNCE0_1	MSPI Manager 0 nCE 1 Signal	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K5	25	0	M2SCL	I2C Manager 2 clock	Open Drain Output
		1	M2SCK	SPI Manager 2 clock	Output
		2	-	-	-
		3	GPIO25	General purpose I/O	I/O
		4	-	-	-
		5	UART1TX	UART1 transmit output	Output
		6	CT25	Timer/counter 25	Output
		7	NCE25	IOMSTR N Chip Select 25	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
L5	26	0	M2SDAWIR3	I2C Manager 2 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
		1	M2MOSI	SPI Manager 2 output data	Output
		2	-	-	-
		3	GPIO26	General purpose I/O	I/O
		4	-	-	-
		5	UART1RX	UART1 receive input	Input
		6	CT26	Timer/counter 26	Output
		7	NCE26	IOMSTR N Chip Select 26	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
L7	27	0	M2MISO	SPI Manager 2 input data	Input
		1	TRIG0	ADC trigger input	Input
		2	MNCE3_0	MSPI Manager 3 nCE 0 Signal	-
		3	GPIO27	General purpose I/O	I/O
		4	-	-	-
		5	UART1CTS	UART1 Clear to Send (CTS) input	Input
		6	CT27	Timer/counter 27	Output
		7	NCE27	IOMSTR N Chip Select 27	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
L1	28	0	SWO	Serial Wire Debug	Output
		1	VCMPO	Output of the voltage comparator signal	-
		2	-	-	-
		3	GPIO28	General purpose I/O	I/O
		4	UART2CTS	UART2 Clear to Send (CTS) input	Input
		5	-	-	-
		6	CT28	Timer/counter 28	Output
		7	NCE28	IOMSTR N Chip Select 28	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
M5	29	0	TRIG0	ADC trigger input	Input
		1	VCMPO	Output of the voltage comparator signal	-
		2	-	-	-
		3	GPIO29	General purpose I/O	I/O
		4	UART1CTS	UART1 Clear to Send (CTS) input	Input
		5	-	-	-
		6	CT29	Timer/counter 29	Output
		7	NCE29	IOMSTR N Chip Select 29	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
K4	31	0	M3SCL	I2C Manager 3 clock	Open Drain Output
		1	M3SCK	SPI Manager 3 clock	Output
		2	I2S0_CLK	I2S0 Bit clock	Bidirectional
		3	GPIO31	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART2CTS	UART2 Clear to Send (CTS) input	Input
		6	CT31	Timer/counter 31	Output
		7	NCE31	IOMSTR N Chip Select 31	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
L3	32	0	M3SDAWIR3	I2C Manager 3 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
		1	M3MOSI	SPI Manager 3 output data	Output
		2	I2S0_DATA	I2S0 Data	Bidirectional
		3	GPIO32	General purpose I/O	I/O
		4	UART0RX	UART0 receive input	Input
		5	UART3CTS	UART3 Clear to Send (CTS) input	Input
		6	CT32	Timer/counter 32	Output
		7	NCE32	IOMSTR N Chip Select 32	Output
		9	I2S0_SDOUT	I2S0 Data output	Output
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
K2	33	0	M3MISO	SPI Manager 3 input data	Input
		1	CLKOUT	Oscillator output clock	Output
		2	I2S0_WS	I2S0 L/R clock	Bidirectional
		3	GPIO33	General purpose I/O	I/O
		4	UART2RX	UART2 receive input	Input
		5	UART2RTS	UART2 Request to Send (RTS)	Output
		6	CT33	Timer/counter 33	Output
		7	NCE33	IOMSTR N Chip Select 33	Output
		9	DISP_TE	Display TE input	Input
		10	MNCE1_0	MSPI Manager 1 nCE 0 Signal	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
K3	34	0	M4SCL	I2C Manager 4 Clk	Output
		1	M4SCK	SPI Manager 4 Clk	Output
		2	SWO	Serial Wire Debug	Output
		3	GPIO34	General purpose I/O	I/O
		4	UART0TX	UART0 transmit output	Output
		5	UART2RX	UART2 receive input	Input
		6	CT34	Timer/counter 34	Output
		7	NCE34	IOMSTR N Chip Select 34	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	I2S1_CLK	I2S1 Bit clock	Bidirectional
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J4	35	0	M4SDAWIR3	I2C Manager 4 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
		1	M4MOSI	SPI Manager 4 data out	Input
		2	SWO	Serial Wire Debug	Output
		3	GPIO35	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART3TX	UART3 transmit output	Output
		6	CT35	Timer/counter 35	Output
		7	NCE35	IOMSTR N Chip Select 35	Output
		9	I2S1_SDOUT	I2S1 Data output	Output
		10	I2S1_DATA	I2S1 Data	Bidirectional
		11	-	-	-
		12	-	-	-
		13	-	-	-
J3	36	0	M4MISO	SPI Manager 4 data in	Input
		1	TRIG0	ADC trigger input	Input
		2	MNCE3_0	MSPI Manager 3 nCE 0 Signal	-
		3	GPIO36	General purpose I/O	I/O
		4	UART0RX	UART0 receive input	Input
		5	UART1RX	UART1 receive input	Input
		6	CT36	Timer/counter 36	Output
		7	NCE36	IOMSTR N Chip Select 36	Output
		9	MNCE1_0	MSPI Manager 1 nCE 0 Signal	-
		10	I2S1_WS	I2S1 L/R clock	Bidirectional
		11	-	-	-
		12	-	-	-
		13	-	-	-
F13	37	0	MSPI0_10	MSPI Manager 0 Interface Signal	I/O
		1	TRIG1	ADC trigger input	Input
		2	32KHzXT	32kHZ from analog	Output
		3	GPIO37	General purpose I/O	I/O
		4	UART2RX	UART2 receive input	Input
		5	UART3RX	UART3 receive input	Input
		6	CT37	Timer/counter 37	Output
		7	NCE37	IOMSTR N Chip Select 37	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G13	38	0	MSPI0_11	MSPI Manager 0 Interface Signal	I/O
		1	TRIG2	ADC trigger input	Input
		2	SWTRACECLK	Serial Wire Debug Trace Clock	Output
		3	GPIO38	General purpose I/O	I/O
		4	UART0RTS	UART0 Request to Send (RTS)	Output
		5	UART2RTS	UART2 Request to Send (RTS)	Output
		6	CT38	Timer/counter 38	Output
		7	NCE38	IOMSTR N Chip Select 38	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
F11	39	0	MSPI0_12	MSPI Manager 0 Interface Signal	I/O
		1	TRIG3	ADC trigger input	Input
		2	SWTRACE0	Serial Wire Debug Trace Output 0	Output
		3	GPIO39	General purpose I/O	I/O
		4	UART2RTS	UART2 Request to Send (RTS)	Output
		5	UART3RTS	UART3 Request to Send (RTS)	Output
		6	CT39	Timer/counter 39	Output
		7	NCE39	IOMSTR N Chip Select 39	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
D13	40	0	MSPI0_13	MSPI Manager 0 Interface Signal	I/O
		1	TRIG1	ADC trigger input	Input
		2	SWTRACE1	Serial Wire Debug Trace Output 1	Output
		3	GPIO40	General purpose I/O	I/O
		4	UART0CTS	UART0 Clear to Send (CTS)	Input
		5	UART1CTS	UART1 Clear to Send (CTS) input	Input
		6	CT40	Timer/counter 40	Output
		7	NCE40	IOMSTR N Chip Select 40	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
E10	41	0	MSPI0_14	MSPI Manager 0 Interface Signal	I/O
		1	TRIG0	ADC trigger input	Input
		2	SWTRACE2	Serial Wire Debug Trace Output 2	Output
		3	GPIO41	General purpose I/O	I/O
		4	UART0TX	UART0 transmit output	Output
		5	UART1TX	UART1 transmit output	Output
		6	CT41	Timer/counter 41	Output
		7	NCE41	IOMSTR N Chip Select 41	Output
		9	SWO	Serial Wire Debug	Output
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
H13	42	0	MSPI0_15	MSPI Manager 0 Interface Signal	I/O
		1	TRIG2	ADC trigger input	Input
		2	SWTRACE3	Serial Wire Debug Trace Output 3	Output
		3	GPIO42	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART3TX	UART3 transmit output	Output
		6	CT42	Timer/counter 42	Output
		7	NCE42	IOMSTR N Chip Select 42	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
G12	43	0	MSPI0_16	MSPI Manager 0 Interface Signal	I/O
		1	TRIG3	ADC trigger input	Input
		2	SWTRACECTL	Serial Wire Debug Trace Control	Output
		3	GPIO43	General purpose I/O	I/O
		4	UART0RX	UART0 receive input	Input
		5	UART1RX	UART1 receive input	Input
		6	CT43	Timer/counter 43	Output
		7	NCE43	IOMSTR N Chip Select 43	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
F12	44	0	MSPI0_17	MSPI Manager 0 Interface Signal	I/O
		1	TRIG1	ADC trigger input	Input
		2	SWO	Serial Wire Debug	Output
		3	GPIO44	General purpose I/O	I/O
		4	UART2RX	UART2 receive input	Input
		5	UART3RX	UART3 receive input	Input
		6	CT44	Timer/counter 44	Output
		7	NCE44	IOMSTR N Chip Select 44	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
E11	45	0	MSPI0_18	MSPI Manager 0 Interface Signal	I/O
		1	TRIG2	ADC trigger input	Input
		2	32KHzXT	32kHZ from analog	Output
		3	GPIO45	General purpose I/O	I/O
		4	UART0TX	UART0 transmit output	Output
		5	UART1TX	UART1 transmit output	Output
		6	CT45	Timer/counter 45	Output
		7	NCE45	IOMSTR N Chip Select 45	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
C11	46	0	-	-	-
		1	TRIG3	ADC trigger input	Input
		2	CLKOUT_32M	32MHz Oscillator output clock	Output
		3	GPIO46	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART3TX	UART3 transmit output	Output
		6	CT46	Timer/counter 46	Output
		7	NCE46	IOMSTR/MSPI N Chip Select 46	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K1	47	0	M5SCL	I2C Manager 5 Clk	Bidirectional Open Drain
		1	M5SCK	SPI Manager 5 Clk	Output
		2	-	-	-
		3	GPIO47	General purpose I/O	I/O
		4	UART0RX	UART0 receive input	Input
		5	UART1RX	UART1 receive input	Input
		6	CT47	Timer/counter 47	Output
		7	NCE47	IOMSTR N Chip Select 47	Output
		9	-	-	-
		10	I2S0_CLK	I2S0 Bit clock	Bidirectional
		11	-	-	-
		12	-	-	-
		13	-	-	-
J2	48	0	M5SDAWIR3	I2C Manager 5 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
		1	M5MOSI	SPI Manager 5 data out	Output
		2	-	-	-
		3	GPIO48	General purpose I/O	I/O
		4	UART2RX	UART2 receive input	Input
		5	UART3RX	UART3 receive input	Input
		6	CT48	Timer/counter 48	Output
		7	NCE48	IOMSTR N Chip Select 48	Output
		9	-	-	-
		10	I2S0_WS	I2S0 L/R clock	Bidirectional
		11	-	-	-
		12	-	-	-
		13	-	-	-
J1	49	0	M5MISO	SPI Manager 5 data in	Input
		1	TRIG0	ADC trigger input	Input
		2	MNCE1_0	MSPI Manager 1 nCE 0 Signal	-
		3	GPIO49	General purpose I/O	I/O
		4	UART0RTS	UART0 Request to Send (RTS)	Output
		5	UART1RTS	UART1 Request to Send (RTS)	Output
		6	CT49	Timer/counter 49	Output
		7	NCE49	IOMSTR N Chip Select 49	Output
		9	I2S0_DATA	I2S0 Data	Bidirectional
		10	I2S0_SDOUT	I2S0 Data output	Output
		11	-	-	-
		12	MNCE1_1	MSPI Manager 1 nCE 1 Signal	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
D11	50	0	PDM0_CLK	PDM0 Clock output	Output
		1	TRIG0	ADC trigger input	Input
		2	SWTRACECLK	Serial Wire Debug Trace Clock	Output
		3	GPIO50	General purpose I/O	I/O
		4	UART2RTS	UART2 Request to Send (RTS)	Output
		5	UART3RTS	UART3 Request to Send (RTS)	Output
		6	CT50	Timer/counter 50	Output
		7	NCE50	IOMSTR N Chip Select 50	Output
		9	DISP_TE	Display TE input	Input
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
C10	51	0	PDM0_DATA	PDM0 audio data input to chip	Input
		1	TRIG1	ADC trigger input	Input
		2	SWTRACE0	Serial Wire Debug Trace Output 0	Output
		3	GPIO51	General purpose I/O	I/O
		4	UART0CTS	UART0 Clear to Send (CTS)	Input
		5	UART1CTS	UART1 Clear to Send (CTS) input	Input
		6	CT51	Timer/counter 51	Output
		7	NCE51	IOMSTR N Chip Select 51	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
D10	57	0	MNCE0_1	MSPI Manager 0 nCE 1 Signal	-
		1	TRIG3	ADC trigger input	Input
		2	SWO	Serial Wire Debug	Output
		3	GPIO57	General purpose I/O	I/O
		4	UART0RTS	UART0 Request to Send (RTS)	Output
		5	UART1RTS	UART1 Request to Send (RTS)	Output
		6	CT57	Timer/counter 57	Output
		7	NCE57	IOMSTR/MSPI N Chip Select 57	Output
		9	I2S1_DATA	I2S1 Data	Bidirectional
		10	I2S1_SDOUT	I2S1 Data output	Output
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
H11	64	0	MSPI0_0	MSPI Manager 0 Interface Signal	I/O
		1	32KHzXT	32kHZ from analog	Output
		2	SWO	Serial Wire Debug	Output
		3	GPIO64	General purpose I/O	I/O
		4	UART0RTS	UART0 Request to Send (RTS)	Output
		5	UART2CTS	UART2 Clear to Send (CTS) input	Input
		6	CT64	Timer/counter 64	Output
		7	NCE64	IOMSTR N Chip Select 64	Output
		9	I2S1_SDIN	I2S1 Data input	Input
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
J13	65	0	MSPI0_1	MSPI Manager 0 Interface Signal	I/O
		1	32KHzXT	32kHZ from analog	Output
		2	SWO	Serial Wire Debug	Output
		3	GPIO65	General purpose I/O	I/O
		4	UART0CTS	UART0 Clear to Send (CTS)	Input
		5	UART1CTS	UART1 Clear to Send (CTS) input	Input
		6	CT65	Timer/counter 65	Output
		7	NCE65	IOMSTR N Chip Select 65	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
L12	66	0	MSPI0_2	MSPI Manager 0 Interface Signal	I/O
		1	CLKOUT	Oscillator output clock	Output
		2	SWO	Serial Wire Debug	Output
		3	GPIO66	General purpose I/O	I/O
		4	UART0TX	UART0 transmit output	Output
		5	UART1TX	UART1 transmit output	Output
		6	CT66	Timer/counter 66	Output
		7	NCE66	IOMSTR N Chip Select 66	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J12	67	0	MSPI0_3	MSPI Manager 0 Interface Signal	I/O
		1	CLKOUT	Oscillator output clock	Output
		2	SWO	Serial Wire Debug	Output
		3	GPIO67	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART3TX	UART3 transmit output	Output
		6	CT67	Timer/counter 67	Output
		7	NCE67	IOMSTR N Chip Select 67	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
M12	68	0	MSPI0_4	MSPI Manager 0 Interface Signal	I/O
		1	SWO	Serial Wire Debug	Output
		2	-	-	-
		3	GPIO68	General purpose I/O	I/O
		4	UART0RX	UART0 receive input	Input
		5	UART1RX	UART1 receive input	Input
		6	CT68	Timer/counter 68	Output
		7	NCE68	IOMSTR N Chip Select 68	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
F10	69	0	MSPI0_5	MSPI Manager 0 Interface Signal	I/O
		1	32KHzXT	32kHZ from analog	Output
		2	SWO	Serial Wire Debug	Output
		3	GPIO69	General purpose I/O	I/O
		4	UART2RX	UART2 receive input	Input
		5	UART3RX	UART3 receive input	Input
		6	CT69	Timer/counter 69	Output
		7	NCE69	IOMSTR N Chip Select 69	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J11	70	0	MSPI0_6	MSPI Manager 0 Interface Signal	I/O
		1	32KHzXT	32kHZ from analog	Output
		2	SWTRACE0	Serial Wire Debug Trace Output 0	Output
		3	GPIO70	General purpose I/O	I/O
		4	UART0RTS	UART0 Request to Send (RTS)	Output
		5	UART1RTS	UART1 Request to Send (RTS)	Output
		6	CT70	Timer/counter 70	Output
		7	NCE70	IOMSTR N Chip Select 70	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
K12	71	0	MSPI0_7	MSPI Manager 0 Interface Signal	I/O
		1	CLKOUT	Oscillator output clock	Output
		2	SWTRACE1	Serial Wire Debug Trace Output 1	Output
		3	GPIO71	General purpose I/O	I/O
		4	UART0CTS	UART0 Clear to Send (CTS)	Input
		5	UART3RTS	UART3 Request to Send (RTS)	Output
		6	CT71	Timer/counter 71	Output
		7	NCE71	IOMSTR N Chip Select 71	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
M11	72	0	MSPI0_8	MSPI Manager 0 Interface Signal	I/O
		1	CLKOUT	Oscillator output clock	Output
		2	SWTRACE2	Serial Wire Debug Trace Output 2	Output
		3	GPIO72	General purpose I/O	I/O
		4	UART0TX	UART0 transmit output	Output
		5	UART1TX	UART1 transmit output	Output
		6	CT72	Timer/counter 72	Output
		7	NCE72	IOMSTR N Chip Select 72	Output
		9	VCMPO	Output of the voltage comparator signal	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G11	73	0	MSPI0_9	MSPI Manager 0 Interface Signal	I/O
		1	-	-	-
		2	SWTRACE3	Serial Wire Debug Trace Output 3	Output
		3	GPIO73	General purpose I/O	I/O
		4	UART2TX	UART2 transmit output	Output
		5	UART3TX	UART3 transmit output	Output
		6	CT73	Timer/counter 73	Output
		7	NCE73	IOMSTR/MSPI N Chip Select 73	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
L11	83	0	MSPI2_9	MSPI Manager 2 Interface Signal	I/O
		1	32KHzXT	32kHZ from analog	Output
		2	DISP_QSPI_D3	Display SPI Data3	Output
		3	GPIO83	General purpose I/O	I/O
		4	SWTRACE3	Serial Wire Debug Trace Output 3	Output
		5	UART3RTS	UART3 Request to Send (RTS)	Output
		6	CT83	Timer/counter 83	Output
		7	NCE83	IOMSTR/MSPI N Chip Select 83	Output
		9	DISP_SPI_RST	Display SPI Reset	Output
		10	SLMISO	SPI Subordinate Half Duplex output data	Output
		11	-	-	-
		12	-	-	-
		13	-	-	-
H10	84	0	-	-	-
		1	-	-	-
		2	SDIF0_DAT0	SD/SDIO/MMC Data0 pin	I/O
		3	GPIO84	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT84	Timer/counter 84	Output
		7	NCE84	IOMSTR/MSPI N Chip Select 84	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J10	85	0	-	-	-
		1	-	-	-
		2	SDIF0_DAT1	SD/SDIO/MMC Data1 pin	I/O
		3	GPIO85	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT85	Timer/counter 85	Output
		7	NCE85	IOMSTR/MSPI N Chip Select 85	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
K10	86	0	-	-	-
		1	-	-	-
		2	SDIF0_DAT2	SD/SDIO/MMC Data2 pin	I/O
		3	GPIO86	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT86	Timer/counter 86	Output
		7	NCE86	IOMSTR/MSPI N Chip Select 86	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
L9	87	0	-	-	-
		1	-	-	-
		2	SDIF0_DAT3	SD/SDIO/MMC Data3 pin	I/O
		3	GPIO87	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT87	Timer/counter 87	Output
		7	NCE87	IOMSTR N Chip Select 87	Output
		9	DISP_TE	Display TE input	Input
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K9	88	0	-	-	-
		1	-	-	-
		2	SDIF0_CLKOUT	SD/SDIO/MMC Clock to Card (CLK)	Output
		3	GPIO88	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT88	Timer/counter 88	Output
		7	NCE88	IOMSTR N Chip Select 88	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
H1	95	0	MSPI1_0	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO95	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT95	Timer/counter 89	Output
		7	NCE95	IOMSTR N Chip Select 95	Output
		9	I2S0_SDIN	I2S0 Data input	Input
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
H2	96	0	MSPI1_1	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO96	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT96	Timer/counter 89	Output
		7	NCE96	IOMSTR N Chip Select 96	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G4	97	0	MSPI1_2	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO97	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT97	Timer/counter 89	Output
		7	NCE97	IOMSTR N Chip Select 97	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
H3	98	0	MSPI1_3	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO98	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT98	Timer/counter 89	Output
		7	NCE98	IOMSTR N Chip Select 98	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
F4	99	0	MSPI1_4	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO99	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT99	Timer/counter 89	Output
		7	NCE99	IOMSTR N Chip Select 99	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G3	100	0	MSPI1_5	MSPI Manager 1 Interface Signal	I/O
		1	DISP_QSPI_D0_OUT	Display SPI Data0	Output
		2	DISP_QSPI_D0	Display SPI Data0	Bidirectional
		3	GPIO100	General purpose I/O	I/O
		4	DISP_SPI_SD	Display SPI Data Out	Bidirectional
		5	DISP_SPI_SDO	Display SPI Data Out	Output
		6	CT100	Timer/counter 100	Output
		7	NCE100	IOMSTR N Chip Select 100	Output
		9	I2S0_CLK	I2S0 Bit clock	Bidirectional
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
E4	101	0	MSPI1_6	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	DISP_QSPI_D1	Display SPI Data1	Output
		3	GPIO101	General purpose I/O	I/O
		4	DISP_SPI_DCX	Display SPI DCx	Output
		5	-	-	-
		6	CT101	Timer/counter 101	Output
		7	NCE101	IOMSTR N Chip Select 101	Output
		9	I2S0_DATA	I2S0 Data	Bidirectional
		10	I2S0_SDOUT	I2S0 Data output	Output
		11	-	-	-
		12	-	-	-
		13	-	-	-
D4	102	0	MSPI1_7	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	DISP_QSPI_SCK	Display SPI CLK	Output
		3	GPIO102	General purpose I/O	I/O
		4	DISP_SPI_SCK	Display SPI Clock	Output
		5	-	-	-
		6	CT102	Timer/counter 102	Output
		7	NCE102	IOMSTR N Chip Select 102	Output
		9	I2S0_WS	I2S0 L/R clock	Bidirectional
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
F3	103	0	MSPI1_8	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	DISP_QSPI_D2	Display SPI Data2	Output
		3	GPIO103	General purpose I/O	I/O
		4	DISP_SPI_SDI	Display SPI Data IN	input
		5	-	-	-
		6	CT103	Timer/counter 103	Output
		7	NCE103	IOMSTR N Chip Select 103	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
C3	104	0	MSPI1_9	MSPI Manager 1 Interface Signal	I/O
		1	-	-	-
		2	DISP_QSPI_D3	Display SPI Data3	Output
		3	GPIO104	General purpose I/O	I/O
		4	DISP_SPI_RST	Display SPI Reset	Output
		5	-	-	-
		6	CT104	Timer/counter 104	Output
		7	NCE104	IOMSTR N Chip Select 104	Output
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
B10	125	0	SDIF1_DAT0	SD/SDIO/MMC Data0 pin	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO125	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT125	Timer/counter 125	Output
		7	NCE125	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
A10	126	0	SDIF1_DAT1	SD/SDIO/MMC Data1 pin	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO126	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT126	Timer/counter 126	Output
		7	NCE126	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
C9	127	0	SDIF1_DAT2	SD/SDIO/MMC Data2 pin	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO127	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT127	Timer/counter 127	Output
		7	NCE127	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
A9	128	0	SDIF1_DAT3	SD/SDIO/MMC Data3 pin	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO128	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT128	Timer/counter 128	Output
		7	NCE128	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
B9	129	0	SDIF1_CLKOUT	SD/SDIO/MMC Clock to Card (CLK)	Output
		1	-	-	-
		2	-	-	-
		3	GPIO129	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT129	Timer/counter 129	Output
		7	NCE129	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
B8	134	0	SDIF1_CMD	SD1/SD4/MMC Command pin	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO134	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT134	Timer/counter 134	Output
		7	NCE134	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
G2	142	0	SWTRACECLK	Serial Wire Debug Trace Clock	Output
		1	-	-	-
		2	-	-	-
		3	GPIO142	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT142	Timer/counter 142	Output
		7	NCE142	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
F2	143	0	SWTRACE0	Serial Wire Debug Trace Output 0	Output
		1	-	-	-
		2	-	-	-
		3	GPIO143	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT143	Timer/counter 143	Output
		7	NCE143	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
E2	144	0	SWTRACE1	Serial Wire Debug Trace Output 1	Output
		1	-	-	-
		2	-	-	-
		3	GPIO144	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT144	Timer/counter 144	Output
		7	NCE144	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
D2	145	0	SWTRACE2	Serial Wire Debug Trace Output 2	Output
		1	-	-	-
		2	-	-	-
		3	GPIO145	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT145	Timer/counter 145	Output
		7	NCE145	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
E3	146	0	SWTRACE3	Serial Wire Debug Trace Output 3	Output
		1	-	-	-
		2	-	-	-
		3	GPIO146	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT146	Timer/counter 146	Output
		7	NCE146	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
D3	147	0	SWTRACECTL	Serial Wire Debug Trace Control	Output
		1	-	-	-
		2	-	-	-
		3	GPIO147	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT147	Timer/counter 147	Output
		7	NCE147	-	-
		9	MNCE0_0	MSPI Manager 0 nCE 0 Signal	-
		10	MNCE3_0	MSPI Manager 3 nCE 0 Signal	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
H7	156	0	SDIF0_DAT4	SD/SDIO/MMC Data4 pin	I/O
		1	MNCE2_1	MSPI Manager 2 nCE 1 Signal	-
		2	-	-	-
		3	GPIO156	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT156	Timer/counter 156	Output
		7	NCE156	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J7	157	0	SDIF0_DAT5	SD/SDIO/MMC Data5 pin	I/O
		1	MNCE2_0	MSPI Manager 2 nCE 0 Signal	-
		2	-	-	-
		3	GPIO157	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT157	Timer/counter 157	Output
		7	NCE157	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
K7	158	0	SDIF0_DAT6	SD/SDIO/MMC Data6 pin	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO158	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT158	Timer/counter 158	Output
		7	NCE158	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
L8	159	0	SDIF0_DAT7	SD/SDIO/MMC Data7 pin	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO159	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT159	Timer/counter 159	Output
		7	NCE159	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

Table 24: Apollo510B SoC Pin List and Function Table

510B Ball No.	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K8	160	0	SDIF0_CMD	SD1/SD4/MMC Command pin	I/O
		1	-	-	-
		2	-	-	-
		3	GPIO160	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT160	Timer/counter 160	Output
		7	NCE160	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
D12	199	0	-	-	-
		1	MNCE0_0	MSPI Manager 0 nCE 0 Signal	-
		2	-	-	-
		3	GPIO199	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT199	Timer/counter 199	Output
		7	NCE199	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-
E12	200	0	-	-	-
		1	MNCE0_1	MSPI Manager 0 nCE 1 Signal	-
		2	MNCE0_0	MSPI Manager 0 nCE 0 Signal	-
		3	GPIO200	General purpose I/O	I/O
		4	-	-	-
		5	-	-	-
		6	CT200	Timer/counter 200	Output
		7	NCE200	-	-
		9	-	-	-
		10	-	-	-
		11	-	-	-
		12	-	-	-
		13	-	-	-

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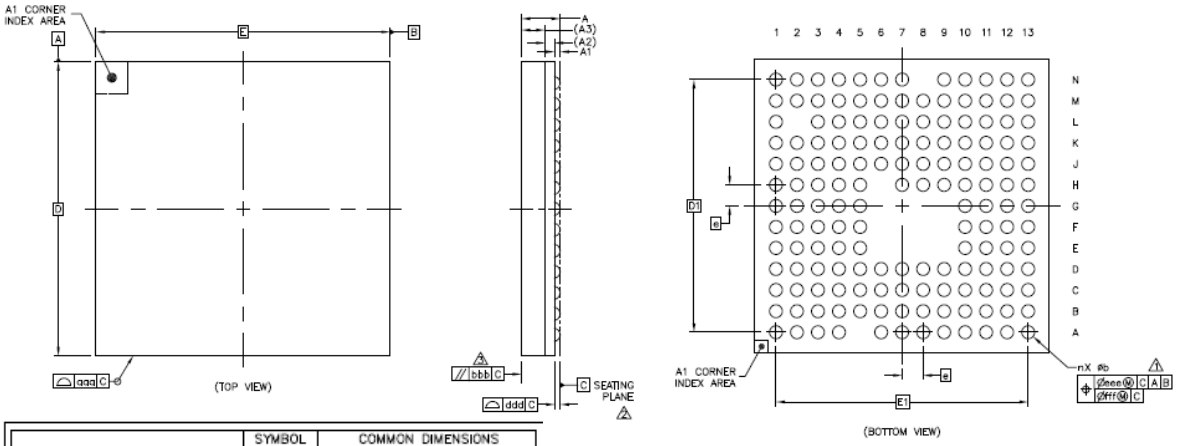
29. Package Mechanical Information[1]

29.1 Apollo510B BGA Package



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	---	---	0.8
STAND OFF	A1	0.07	---	0.15
SUBSTRATE THICKNESS	A2		0.18	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		5.6	BSC
	E		5.6	BSC
BALL DIAMETER			0.2	
BALL OPENING			0.25	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.4	BSC
BALL COUNT	n		153	
EDGE BALL CENTER TO CENTER	D1		4.8	BSC
	E1		4.8	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.1	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.05	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 56. BGA Package Drawing for Apollo510B SoC

1. All dimensions in mm unless otherwise noted.

29.1.1 Top Side Marking

Package type: 5.6 x 5.6 mm, 153-pin BGA

Part Number: AP510BFA-CBR

Memory Size: 4 MB

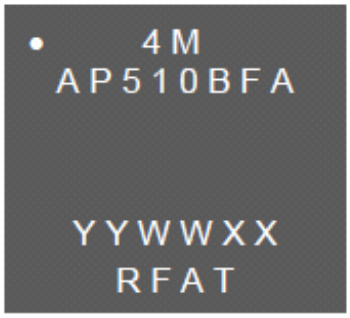


Figure 57. Apollo510B BGA Package Top Side Marking

Table 25: Apollo510 BGA Marking Description

Line	Field	Description
1	Part Description	4M
2	Part Name	AP510BFA
3	YY = Year WW = Work Week XX = Sequential Lot Number	YY corresponds to the year. WW is the release week of assembly lot. XX is the sequential lot number assigned by the assembly house
4	R = Production Revision F = Foundry Site A = Assembly Site T = Test Site	RFAT designates the product revision and the supply chain.

29.1.2 Tape & Reel Data

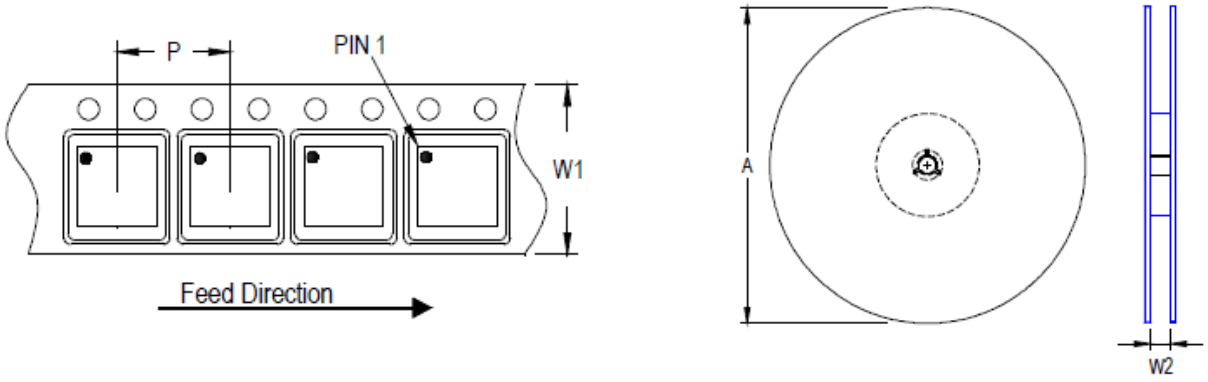


Figure 58. Tape Feed Direction and Reel Dimension Drawing

Table 26: Tape & Reel Dimension Table

Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Reel Width (W2) Min/Max (mm)
		(mm)	(in)	
12	8	330	13	12.4/13.4

29.1.3 Tape & Reel Packaging

Table 27: Tape & Reel Packaging Dimensions

Reel		Inner Box			Outer Carton		
Size (mm)	Units	Size (mm)	Reels	Units	Size (mm)	Boxes	Units
330	5,000	355 x 338 x 50	1	5,000	375 x 284 x 362	5	25,000

29.1.4 Label Format

Table 28: Label Location and Format

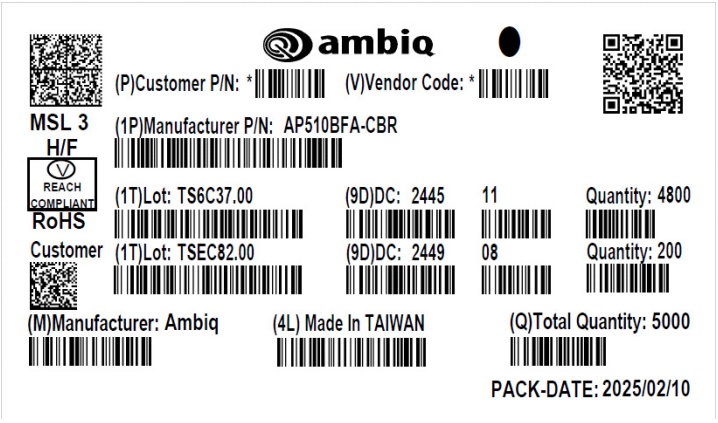
Step	Label Location	Label Format
Reel		One Lot: 
MBB (HIC & Desiccant inside)		Two lots in one reel: *For combined lot, allows at most two 4-digits of date codes to be packed in the one reel.
Inner Box		

Table 28: Label Location and Format

Step	Label Location	Label Format
Outer Carton		

29.2 Reflow Profile

Table 29 lists the reflow conditions for the lead-free package. Reference IR Reflow Profile for Moisture Sensitivity Test (J-STD-020).

Reflow times: 3 cycles

Table 29: Reflow Condition (260 °C) for Pb-free Package

Profile Features	Pb-Free Assembly
Average ramp-up rate (include 217°C to Peak)	3°C/second max.
Temperature maintained above 217°C	60 to 150 seconds
Time within 5°C of actual peak temperature	20 - 40 seconds
Peak temperature (minimum)	260 +0/-5°C
Ramp-down rate	6°C /second max.
Time 25°C to peak temperature	8 minutes max.

Figure 59 illustrates the temperature profile for reflow soldering requirements.

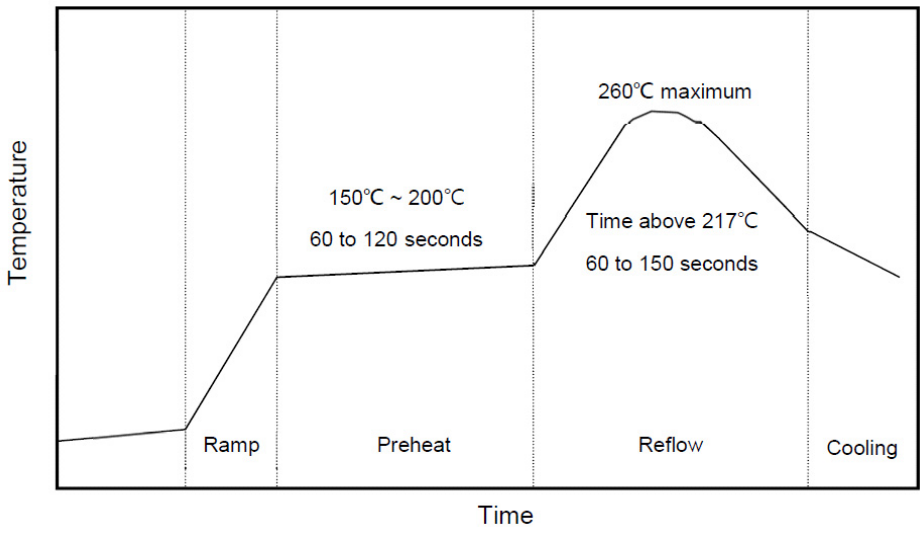


Figure 59. Reflow Profile

30. Electrical Characteristics

IMPORTANT NOTICE

Timing characteristics for the various communication/data interfaces have been determined by either measurements on chip or through simulations. It is noted in each timing set how its characteristics were derived. Characteristics derived through simulation are subject to change, and cover the worst-case fastest and slowest corners.

Contact Ambiq sales with questions about specifications.

30.1 Absolute Maximum Ratings

The absolute maximum ratings are the limits to which the device can be subjected without permanently damaging the device and are stress ratings only. Device reliability may be adversely affected by exposure to absolute-maximum ratings for extended periods. Functional operation of the device at the absolute maximum ratings or any other conditions beyond the recommended operating conditions is not implied.

Table 30: Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
VDDP	SIMO/LDO Buck Supply voltage		-0.2	3.63	V
VDDA	Analog Supply voltage				
VDDH	High voltage domain supply voltage				
VDDH1	High voltage domain 1 IO Supply voltage		-0.2	3.63	V
VDDH2	High voltage domain 2 IO Supply voltage		-0.2	3.63	V
VDDH3	High voltage domain 3 IO Supply voltage		-0.2	3.63	V
VDDH4	High voltage domain 4 IO Supply voltage		-0.2	3.63	V
VDD18	MIPI, DSI, DISPPLL Supply voltage		-0.2	1.98	V
VDDAUDA	Analog Audio Supply voltage		-0.2	1.98	V
VDDUSB33	USB Analog 3.3 V Supply voltage		-0.2	3.63	V
VDDUSB0P9	USB Analog 0.9 V Supply voltage		-0.2	0.99	V
V_{IO}	Voltage on all input and output pins		-0.30	VDDHn[1] + 0.30	V
BLE_VCC	BLE Controller VCC analog supply voltage		-0.2	2.7	V
BLE_VIO	BLE Controller I/O supply voltage		-0.2	VDDH+ 0.3	V
BLE_VBAT1	BLE Controller VBAT1 internally-generated supply voltage		-0.2	3.9	V
BLE_VBAT2	BLE Controller VBAT2 supply voltage		-0.2	3.9	V
$VDDX_{FSLEW}$	Falling slew rate for VDDP, VDDA, VDDH and VDDHn power supplies		-	2	kV/s
T_{OPEC}	Extended commercial operating temperature range	Specific to extended commercial temperature range SKUs	-20	70	ºC
T_{OPI}	Industrial operating temperature range	Specific to industrial temperature range SKUs	-40	85	ºC
T_{REFLOW}	Reflow temperature	Reflow Profile per JEDEC J-STD-020D.1	-	260	ºC
I_{LU}	Latch-up current	EIA/JESD78, 25°C, ±100 mA trigger current and Over voltage at 1.5 Vmax	-	100	mA
V_{ESDHBM}	ESD Human Body Model (HBM)	JS-001-2017	-	2000	V
V_{ESDCDM}	ESD Charged Device Model (CDM)	JS-002-2014	-	250	V

1. The designation “n” corresponds to the voltage source for the pin, e.g., VDDH1. This specification is for all VDDH supplies powering GPIO.

30.2 Recommended Operating Conditions

30.2.1 External Voltage Supplies

Table 31: External Voltage Supplies

Supply	Description	Source	Min	Typ	Max	Units	Notes
VDDA	Analog Supply	Battery / External Regulator	1.71	1.8 - 2.0	2.20	V	VDDA, VDDP and VDDH must be connected to the same supply.
VDDP	SIMO/LDO Buck Supply						
VDDH	High voltage domain supply voltage						
VDDH1	Secondary I/O Supply (Primary Interface: HWTRACE)	Battery / External Regulator	1.14	1.8 - 2.0	2.20	V	
VDDH2	Secondary I/O Supply	Battery / External Regulator	1.71	1.8 - 2.0	2.20	V	VDDH2 must be the same as VDDH.
VDDH3	Secondary I/O Supply (Primary Interface: MSPI0)	Battery / External Regulator	1.14	1.8 - 2.0	2.20	V	
VDDH4	Secondary I/O Supply	Battery / External Regulator	1.71	1.8 - 2.0	2.20	V	VDDH4 must be the same as VDDH.
VDDAUDA	Analog Audio	External LDO, Low quiescent current, low noise preferred	1.62	1.75 - 1.85	1.98	V	Quiescent current: < 1 µA PSRR: > 40 dB in the range 1 kHz to 10 kHz
VDD18	MIPI DPHY LP LDO and transceivers	Battery / External Regulator	1.62	1.8	1.98	V	Noise/ripple: ± 2% (72mVpk-pk) Frequency range: 10 MHz - 3 GHz Leakage current: 2-3 µA (typ)[1]
VDDUSB33	USB Analog 3.3 V Supply	Battery / External Regulator	3.0	3.3	3.63	V	
VDDUSB0P9	USB Analog 0.9 V Supply	External Regulator	0.84	0.9	0.99	V	Noise/ripple: < 3% (pk-pk).
BLE_VBAT2	BLE Controller VBAT2 (PM/analog supply voltage)	Battery / External Regulator	1.1	1.8 (1.9 max)	BLE_VIO	V	Must be connected to BLE_VCC and optionally to BLE_VIO provided the voltage level is within the specified range of all three voltage supplies. Cannot exceed lower of BLE_VIO or 1.9 V in Step-up mode or 2.2 V in Voltage Multiplier mode.
BLE_VCC	BLE Controller VCC (RF supply voltage)	Battery / External Regulator	1.1	1.8 (1.9 max)	1.9/2.2	V	Must be connected to BLE_VBAT2 and optionally to BLE_VIO provided the voltage level is within the specified range of all three voltage supplies. Cannot exceed lower of BLE_VIO or 1.9 V in Step-up mode or 2.2 V in Voltage Multiplier mode.
BLE_VIO	BLE Controller VIO (I/O supply voltage)	Battery / External Regulator	VDDH	-	VDDH	V	BLE_VIO must be connected to VDDH and be equal to or higher than BLE_VBAT2
$VBAT2_{4dBm\_TX}$	Min VBAT2 voltage for +4dBm TX output	BLE_VBAT2	1.35	-	-	V	

Table 31: External Voltage Supplies

Supply	Description	Source	Min	Typ	Max	Units	Notes
$VBAT2_{6dBm\_TX}$	Min VBAT2 voltage for +6dBm TX output	BLE_VBAT2	1.73	-	-	V	

1. A load switch could be used for this rail to decrease current if the stated leakage current is too high for the targeted use case. It is recommended to use a low-leakage external switch controlled by the MCU, such as:.
   - TI TPS22916xx, I_q = 10 nA typ
   - Toshiba TCK106AG/107AG/108AG, I_q = 14 nA typ.
   - Microchip MIC94080/1/4/5, I_q = 20 nA typ.

30.2.2 Recommended External Components for Voltage Supplies

30.2.2.1 Components for External Voltage Supplies

Table 32: Recommended Bypass Capacitors for External Supplies

External Supply	Bypass Capacitor
VDDH, VDDH1, VDDH2	2.2 µF to ground
VDDH3	4.7 µF to ground
VDDH4	0.1 µF to ground
VDDA	1 µF to ground
VDDP	10 µF to ground (SIMO Buck converter output capacitance (4) (VDDC, VDDC_LV, VDDF, VDDS))
VDDAUDA	2.2 µF to ground (Typ); follow recommendations of LDO supplier. See notes below.
VDDUSB33	2.2 µF to ground
VDDUSB0P9	2.2 µF to ground
VDD18	2.2 µF to ground

Additional Notes:

1. For VDDH3, it might be possible to use a bypass capacitor smaller than 4.7 µF (possibly 2.2 µF) depending on the speed of the external LDO and how close the LDO is placed to the Apollo510B device and external PSRAM power pins, and the interface speed being used. It is also recommended that the same size bypass capacitor be used for the I/O supply of the external (PSRAM) device.
2. For VDDP 10 µF: Recommend 0402 package, 10 V. No more than 40% reduction in capacitance (6.0 µF) with a DC bias of 1.8 V. Suitable component: CL05A106MP8NUB8.
3. Recommend use of 5 V or greater capacitors for 1.9 V rails
4. Recommend use of 10 V capacitors for 3.3 V rails
5. Do not float any supply input. If a supply is not used, it should be tied to a supply within its operating range.
6. Suitable standalone small form factor LDOs:
   - Microchip MCP1811A in 1.0 x 1.0 x 0.50 mm UDFN package
   - TI TPS7A02 in 1.0 x 1.0 x 0.40 mm X2SON package

30.2.2.2 Components for SIMO Buck Converter

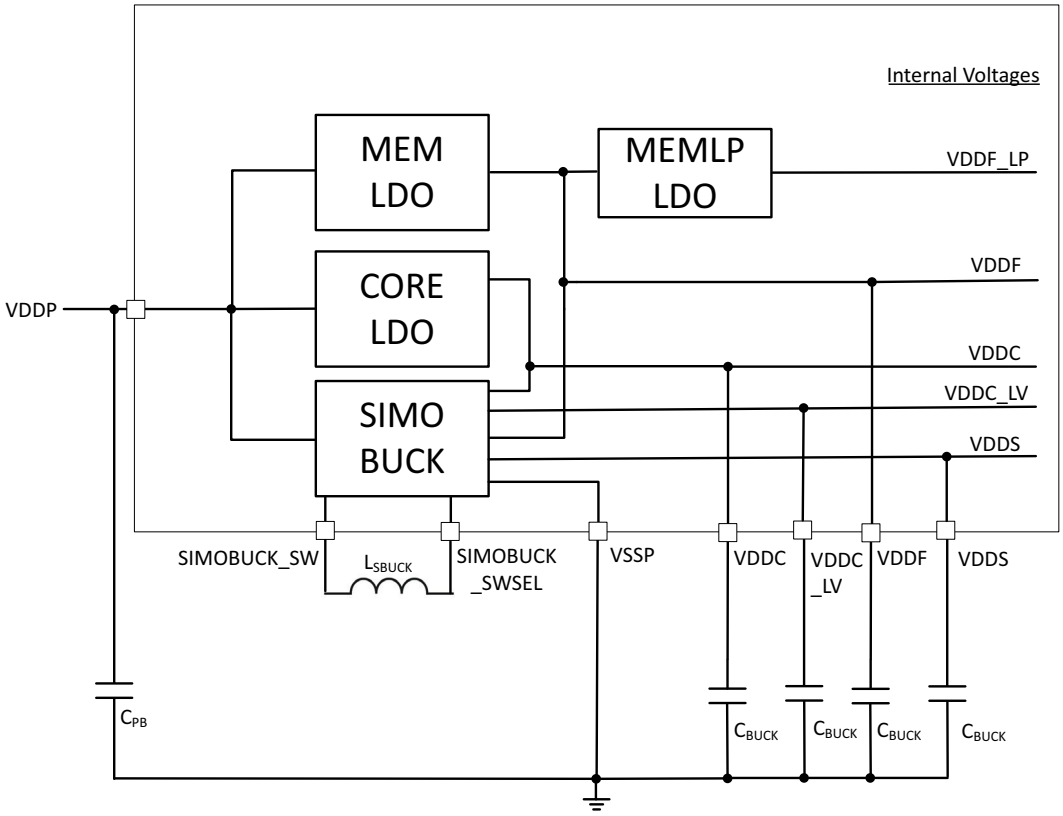


Figure 60. External Components for SIMO Buck

Table 33: SIMO Buck Converter External Components

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
L_{SBUCK}	SIMO Buck converter inductance (V_{SIMO})		-	2.2	-	µH
C_{BUCK}	SIMO Buck converter output capacitance (4) (VDDC, VDDC_LV, VDDF, VDDS)		-	4.7/10	-	µF

NOTES:

1) For operation across the full voltage and temperature range, the SIMO Buck Inductor (L_{SBUCK} connected between SIMOBUCK_SW and SIMOBUCK_SWSEL) with the following characteristics is required:

- 2.2 µH
- Saturation current >= 1 A
- Maximum DC resistance < 550 mΩ
- Operating frequency range > 20 MHz
- Recommended[1] parts:
  - Murata DFE201210U-2R2M=P2 (0805 size)
  - Taiyo Yuden LSCND1608HKT2R2MF (0603 size)
- Other options (all 2.2 µH):

Table 34: SIMO Buck Converter Inductor Options

Part Number	Manufacturer	DCR (mOhm)	Current Rating (Amps)	Saturation Current (Amps)	Footprint	L x W x H (in)
DFE201210U-2R2M=P2	Murata	228	1.2	2	0805	0.079 x 0.047 x 0.039
LSCND1608HKT2R2MF	Taiyo Yuden	250	1.4	1.3	0603	0.063 x 0.031 x 0.031
DFE252012F-2R2M=P2	Murata	82	2.3	3.3	1008	0.098 x 0.079 x 0.047
74479276222C	Wurth Elektronik	135	1.6	2.5	0806	0.079 x 0.063 x 0.039
CIGT201610EH2R2MNE	Samsung	87	2.5	2.9	0806	0.079 x 0.063 x 0.039
DFE21CCN2R2MELL	Murata	138	1.8	2.1	0805	0.079 x 0.047 x 0.031
AOTA-B201610S2R2MT	Abracon	74	2.0	2.6	0806	0.079 x 0.063 x 0.039

2) For C_{BUCK} the following specifications should be followed

- Smaller package option: 4.7 µF, ±20%,6.3 V, X5R, -55°C ~ 85°C, ceramic
- 0201 package to be placed as close to the MCU pins as possible
- No more than 20% reduction in capacitance with a DC bias of 0.9 V
- Recommended parts:
  - Murata GRM035R60J475ME15 or equivalent

Larger package option for up to 2% reduction in total power over smaller package:

- 10 µF, ±20%, 10 V, X5R, -55°C ~ 85°C, ceramic
- 0402 package to be placed as close to the MCU pins as possible
- No more than 20% reduction in capacitance with a DC bias of 0.9 V
- Recommended parts:
  - Murata GRT155R61A106ME13J or equivalent

1. Inductors with higher Q rating (Q > 20 between 2 MHz and 10 MHz) are recommended. Inductors with lower Q may be used, but will result in power consumption increase of a few percent.

30.2.2.3 Components for the BLE Controller

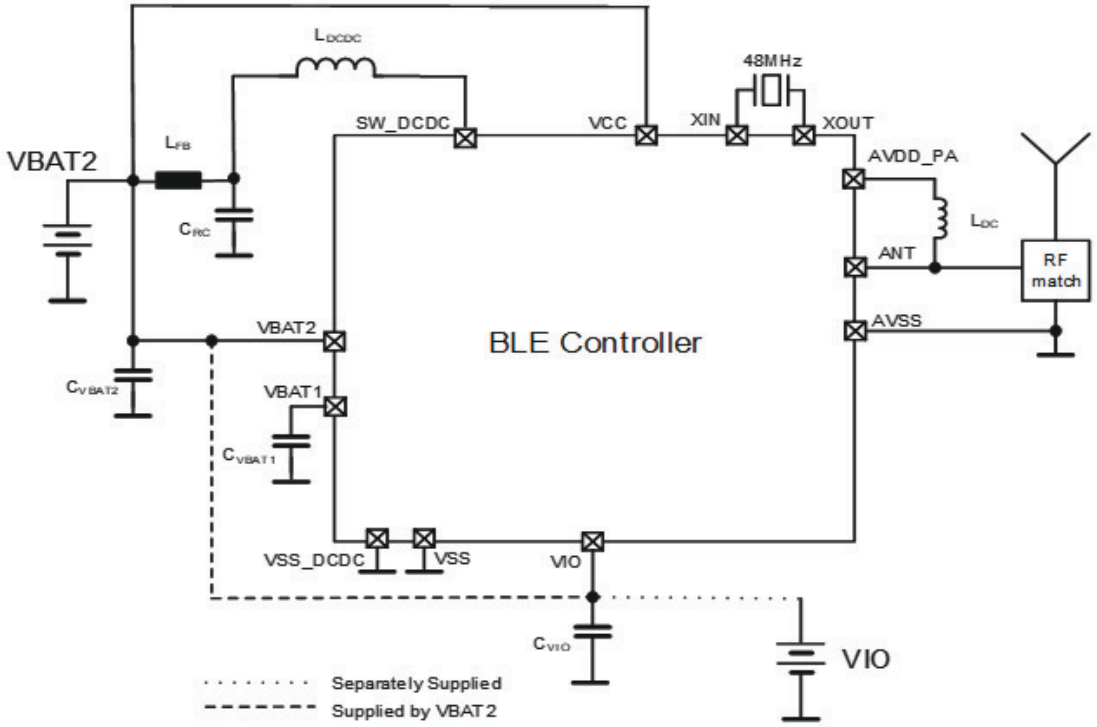


Figure 61. External Components for BLEC - Step-up Power Mode

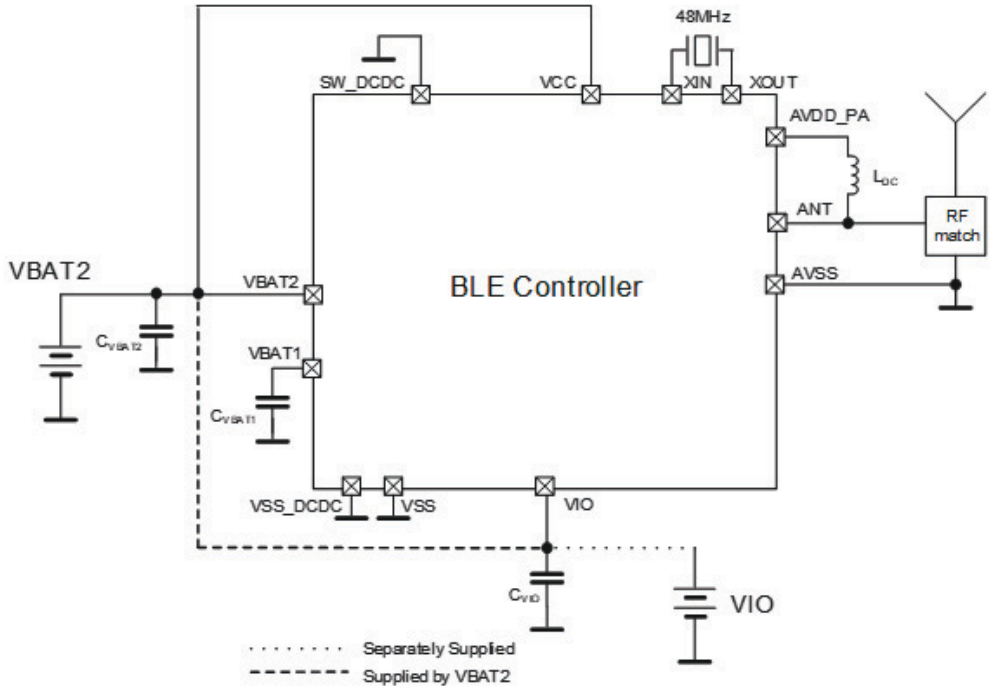


Figure 62. External Components for BLEC - Voltage Multiplier Power Mode

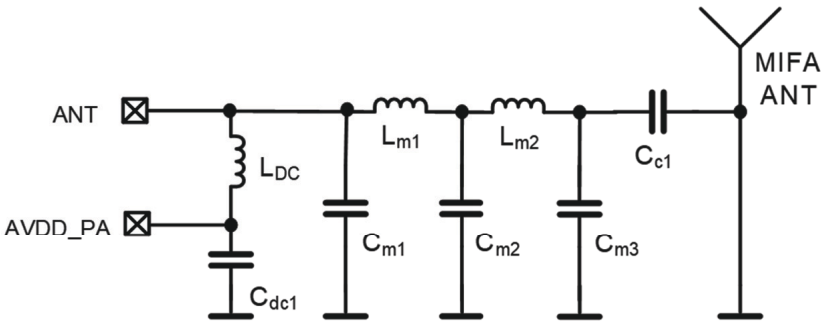


Figure 63. BLEC RF Matching Circuit

Table 35: BLEC Components

Symbol	Parameter	Min	Typ	Used on EVB[1]	Max	Unit
L_{DCDC}	SW_DCDC inductance	-	4.7/2.2		-	µH
C_{VIO}	VIO capacitance	-	100		-	nF
C_{VBAT1}	VBAT1 capacitance[2]	-	2.2		-	µF
C_{VBAT2}	VBAT2 capacitance	-	1		-	µF
C_{RC}	Ferrite bead capacitance	-	1		-	µF
L_{FB}	Ferrite bead inductance	-	3		-	µH
L_{DC}	Antenna matching network DC inductor	-	1.5	1.5	-	nH
C_{dc1}	Antenna matching network DC1 capacitance	-	18	18	-	pF
C_{m1}	Antenna matching network M1 capacitance	-	2.0	2.8	-	pF
C_{m2}	Antenna matching network M2 capacitance	-	2.0	3.2	-	pF
C_{m3}	Antenna matching network M3 capacitance	-	DNP	DNP	-	pF
C_{c1}	Antenna matching network C1 capacitance[3]	-	220	220	-	pF
L_{m1}	Antenna matching network m1 inductance	-	2.4	1.8	-	nH
L_{m2}	Antenna matching network m2 inductance (optional)	-	DNP (shorted)	DNP (shorted)	-	nH

1. EVB component values should only be used as a reference point for a customer's initial matching network; customer's design may require different values. [DNP = do not populate]
2. VBAT1 is the output of an internally generated voltage in the two supported modes of operation of the BLEC. C_{VBAT1} is required.
3. Needed if antenna is referenced to ground rather than the supply.

Table 36: Recommended Parts for BLE Components

Symbol	Part Number	Manufacturer	Component Value	Units	Footprint
L_{DCDC}	LQM18PN4R7MFRL	Murata	4.7	µH	0603
	MLZ1005M2R2WT000	TDK	2.2	µH	0402
C_{VIO}	GRM155R62A104KE14D	Murata	100	nF	0402
C_{VBAT1}[1]	GRM155R61C225KE11D	Murata	2.2	µF	0402
C_{VBAT2}[2]	GRM155R61C105MA12D	Murata	1.0	µF	0402
C_{RC}	GRM155R61C105MA12D	Murata	1.0	µF	0402
L_{FB}	BLM15HG601SN1D	Murata	3.0	µH	0402
L_{DC}	LQG15HS1N5B02D	Murata	1.5	nH	0402
C_{dc1}	Type GRM0335C	Murata	18	pF	0201
C_{m1}	Type GRM0335C	Murata	2.0	pF	0201
C_{m2}	Type GRM0335C	Murata	2.0	pF	0201
C_{m3}	Type GRM0335C	Murata	1.0	pF	0201
C_{c1}	GRM0335C1H221JA01D	Murata	220	pF	0201
L_{m1}	Type LQP03TN	Murata	2.4	nH	0201
L_{m2}	Type LQP03TN	Murata	2.2	nH	0201

1. Smaller (0201) capacitors may be used at the expense of power efficiency. In this case a 0201 capacitor with the best voltage rating specification available should be selected. However, the recommended capacitors are as listed.

NOTE: In situations where an alternate for the SW_DCDC inductor (L_{DCDC}) of the Step-Up Power Mode is required, the parameters listed in Table 37 must be prioritized to ensure compatibility and performance. By default, the SDK assumes an inductor configuration of 4.7 µH. If the system uses an inductor of 2.2 µH, this configuration must be set in the NVM_ConfigModules function of the application. When selecting an alternate L_{DCDC} inductor for the BLEC, ensure the part meets or exceeds the following specifications for inductance, tolerance, rated current, DCR, SRF, and shielding. These parameters directly impact converter efficiency, thermal behavior, and RF integrity.

Table 37: Required Specifications for L_{DCDC} Alternative Sources

Parameter	Why It Matters	Target Specification
Inductance Value	Determines converter stability and performance. Only 2.2 µH and 4.7 µH are supported.	2.2 or 4.7 µH
Tolerance	Lower values reduce production part-to-part variation and protect from problematic corner conditions.	≤ ±20%
Rated Current	Must exceed peak inductor current to avoid core saturation. The higher the current rating, the greater the protection.	≥ 350 mA
DC Resistance (DCR)	Lower DCR improves efficiency by reducing conduction losses.	≤ 550 mΩ
Self-Resonant Frequency (SRF)	Must exceed DCDC switching frequency for correct DCDC operation.	≥ 30 MHz
Magnetic Shielding	Suppresses EMI and protects nearby RF circuitry.	Ferrite-based multi-layer shield

30.2.2.4 Other External Components

- LPADC_VREF
  - 100 nF capacitor from the LPADC_VREF pin to ground
- LPMICBIAS
  - LPMICBIAS can source up to 400 µA at 1.3 V, with a minimum VDDAUDA supply of 1.62 V.
  - 2.2 µF capacitor from the LPMICBIAS pin to ground. A smaller value is acceptable if current is less than 400 µA.

30.2.3 Power Sequencing

Table 38: Power Supply Sequencing

External Supply[1]	Conditions/Notes
VDDP/VDDH/VDDA[2]	1. Power up concurrently from same source to the same voltage (i.e., VDDP = VDDH = VDDA). 2. Should generally be supplied at nearly the same time as other rails. 3. Some skew is acceptable.
VDDH1-VDDH4[2]	1. May be powered up before, or at the same time as, VDDP/VDDH/VDDA are powered[3]. 2. May be a separate supply from VDDP/VDDH/VDDA, but it may be tied to VDDP/VDDH/VDDA if not requiring a different voltage.
BLE_VBAT2, BLE_VCC, BLE_VIO	1. All BLEC power supply rails must be stabilized before the BLE Enable pin (BLE_ENBLE) is asserted. 2. All supplies must be powered up at the same time, and at the same time as or after VDDP/VDDH/VDDA.
VDDAUDA[4]	1. Must be powered before or at the same time as VDDP/VDDH/VDDA. 2. If not using audio, then should be tied to VDDP/VDDH/VDDA if they are within the specified VDDAUDA range. 3. Must be a very clean supply when used to power the Low Power Analog Audio Interface. 4. Primarily needed for internal clocking circuitry as well as the AUDADC.
VDD18	1. Should be tied to ground if not using MIPI DSI interface[5]. 2. If using MIPI, then may be powered at the same time as VDDP/VDDH/VDDA but not before. 3. Preferably only enabled/powered up when the display is being used.
VDDUSB33/ VDDUSB0P9	1. May be powered before, at the same time as, or after VDDP/VDDH/VDDA. 2. For USB power details, see USB chapter and USB PHY specifications later in this chapter. 3. Only required when using USB (i.e., when USB cable is plugged in). 4. Powering both supplies at the same time from VBUS source is recommended, with 0.9 V generated by LDO from the 3.3 V.[6]

1. Recommended termination of unused interface:
   - USB data pads (USB0PP and USB0PN) left open
   - Both USB PHY power rails VDDUSB33 and VDDUSB0P9 connected to ground
   - DSI TX data and clock pads left open
2. Falling slew rate for these supplies cannot exceed 2 kV/s.
3. Grounding any of these supplies while VDDP/VDDH/VDDA are powered will result in excess current draw and can have long term reliability implications. It is acceptable to have one VDDHn rail ramp up *after* VDDP/VDDH/VDDA as long as that rail ramps up while the CPU is still in reset (nRST pin is low).
4. To reduce power consumption and supply noise, VDDAUDA should be tied to a supply within the specified VDDAUDA operating range when not using the Low Power Analog Audio Interface which is powered by the VDDAUDA supply. In this specific scenario, the VDDAUDA supply does not need to meet the Audio Interface's required noise/PSRR conditions.
5. Note that VDD18 leakage current is 2-3 µA (typ).
6. Although it is recommended to power-up VDDUSB33 and VDDUSB0P9 together only when USB is to be used, it is possible to keep VDDUSB33 powered at all times. In which case it is required that a 2 MΩ pull-down resistor be included on each of the USB data lines to prevent leakage current. Note that in all cases, to minimize leakage current, the USB internal power rail must be enabled by software before external power is applied to VDDUSB0P9.

30.3 Current Consumption

Table 39: Current Consumption in Active Mode and Sleep Modes

Symbol	Parameter	Test Conditions[1,2]	VDD (V)	Min	Typ	Max	Unit
$I_{RUNLPFB}$	Coremark run current in low power mode	Executed from internal MRAM, cache enabled, buck enabled, core clock/HFRC=96 MHz	1.8	-	35.3	-	µW/ MHz
$I_{RUNHPFB}$	Coremark run current in high performance mode	Executed from internal MRAM, cache enabled, buck enabled, core clock/HFRC=250 MHz	1.8	-	46.8	-	µW/ MHz
I_{SS1}	System Sleep mode 1 current - 160 kB TCM retained	WFI instruction with SLEEP=1, all core & peripheral clocks gated, HFRC on, XTAL off, SIMO buck enabled, NVM in standby, no System SRAM bank enabled/retained, cache retained, 160 kB TCM enabled/retained	1.8	-	750	-	µW
$I_{SDS2-160RET}$	System Deep Sleep mode 2 current - 160 kB TCM retained	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM powered down, cache off (no retention), 160 kB TCM retained	1.8	-	23.8	-	µW
$I_{SDS2-768RET}$	System Deep Sleep mode 2 current - 768 kB TCM retained	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM powered down, cache off (no retention), 768 kB TCM retained	1.8	-	36.0	-	µW
$I_{SDS2-3840RET}$	System Deep Sleep mode 2 current - all SSRAM/TCM retained	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM powered down, cache off (no retention), 3072 kB SSRAM + 768 kB TCM retained	1.8	-	57.0	-	µW
I_{SDS3}	System Deep Sleep mode 3 current	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM powered down, all SSRAM/TCM/cache off (no retention).	1.8	-	23.1	-	µW

30.3.1 Bluetooth Low Energy Controller Current Consumption

Table 40 lists current consumption to the single-sourced BLE_VBAT2 / BLE_VCC / BLE_VIO supply (V_{BLE}) in TX mode in the Step-up power configuration. Nearly all of the current being drawn is to the BLE_VCC supply input.

Table 40: BLEC Power Consumption in TX Mode

Symbol	Parameter	V_{BLE} (V)	Min	Typ	Max	Units
$I_{TX\_0dBm\_CONT\_OP}$	Radio transmit current measured on single BLE_VBAT2 / BLE_VCC / BLE_VIO supply at 0 dBm continuous output at fixed 2440 kHz	1.8	-	7.3	-	mA
$I_{TX\_6dBm\_CONT\_OP}$	Radio transmit current measured on single BLE_VBAT2 / BLE_VCC / BLE_VIO supply at 6 dBm continuous output at fixed 2440 kHz	1.8	-	12.5	-	mA

Table 41 lists current draw when powering the BLEC at 1.9 V at 48 MHz in Voltage Multiplier mode (CPU in Halt).

Table 41: BLEC Power Consumption in Voltage Multiplier Mode

Symbol	Parameter	BLE_VBAT2 / BLE_VCC (V)	Min	Typ	Max	Units
I_{ACTIVE_RC}	Active mode current - clocked by RC	1.9	-	510	-	µA

Table 42 lists the BLEC's sleep mode current when powering the module at 1.9 V in either the Voltage Multiplier or Step-up configuration.

Table 42: BLEC Sleep Mode Power Consumption

Symbol	Parameter	BLE_VBAT2 / BLE_VCC (V)	Min	Typ	Max	Units
$I_{SLEEP\_60K\_RET}$	Sleep mode, 60kB SRAM retention, 25C	1.9	-	1.14	-	µA
$I_{BATT\_INRUSH\_BOOT}$	Battery in-rush current at boot	1.9	-	11.5	-	mA
$I_{CHIP\_DISABLE}$	Chip disable	1.9	-	7.5	-	nA

30.4 Power-On Reset (POR) and Brown-Out Detector (BOD)

Table 43: Power-On Reset (POR) and Brown-Out Detector (BOD)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR_RISING}	POR rising threshold voltage	-	1.635 - 1.675	-	V
$V_{BODL\_FALLING}$	Brownout detection low falling threshold voltage	-	1.63 - 1.70	-	V
$V_{BLE\_VBAT1\_FALLING}$	Brownout detection low falling BLE_VBAT1 voltage	-	1.62	-	V

30.5 Resets

Table 44: Resets

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PU_{RST}	Internal nRST pull-up resistor		-	24	-	kΩ

30.6 General Purpose Input/Output (GPIO)

The GPIO specifications in this section are applicable to the various types of GPIO pad on the device. Table 45 lists each pad type and the GPIOs which use each pad type. The tables below list the specifications for each pad type.

Table 45: GPIO Pad Types

GPIO Pad Type	Description	GPIO Numbers
GPIO_TOP_LP_V	Standard	0-2, 5-10, 22-27, 52-57, 61-63, 74-88, 125-134, 156-160, 192
GPIO_TOP_LP_H	Standard	31-36, 46-49, 95-104, 114, 147, 195, 199, 200
Skinny_GPIO_TOP_LP_V	Skinny	3-4, 11-21, 28-30, 50-51, 58-60, 89-92, 94, 148-149, 152-155, 161, 165, 173, 175, 208-223
Skinny_GPIO_TOP_LP_H	Skinny	33, 136, 138-141, 150-151, 162, 186-189, 191, 201
HS_GPIO_TOP_H	High speed	37-45, 64-73, 105-113, 115-124, 142-146

Table 47 lists the actual internal pull-up and pull-down resistance for each PULLCFG setting, as well as the source and sink current and general characteristics for standard, skinny and high-speed GPIO pads.

Table 46: General Purpose Input/Output (GPIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All Standard/Skinny GPIOs[1]						
V_{OH}	High-level output voltage		0.8 x V_{DDHn}[2]	-	-	V
V_{OL}	Low-level output voltage		-	-	0.2 x V_{DDHn}	V
V_{IH}	Positive going input threshold voltage		0.7 x V_{DDHn}	-	-	V
V_{IL}	Negative going input threshold voltage		-	-	0.3 x V_{DDHn}	V
C_{GPI}	Input capacitance		-	5	-	pF
I_{IN}	Input pin leakage current		-	1	20	nA
I_{INOD}	Open drain output leakage current		-	1	20	nA
R_{PD50K}	50 kΩ pull-down resistance, PULLCFG = 1	PULLCFG = 1	42.4	51.0	59.4	kΩ
R_{PU15K}	1.5 kΩ pull-up resistance, PULLCFG = 2	PULLCFG = 2	1.3	1.6	1.9	kΩ
R_{PU6K}	6 kΩ pull-up resistance, PULLCFG = 3	PULLCFG = 3	5.2	6.2	7.3	kΩ
R_{PU12K}	12 kΩ pull-up resistance, PULLCFG = 4	PULLCFG = 4	10.4	12.5	14.6	kΩ
R_{PU24K}	24 kΩ pull-up resistance, PULLCFG = 5	PULLCFG = 5	20.6	24.9	29.0	kΩ

Table 46: General Purpose Input/Output (GPIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU50K}	50 kΩ pull-up resistance, PULLCFG = 6	PULLCFG = 6	42.2	50.7	58.8	kΩ
R_{PU100K}	100 kΩ pull-up resistance, PULLCFG = 7	PULLCFG = 7	84.0	100.5	116.6	kΩ
Standard GPIOs						
I_{SRC_0p1DS}	Output source current, 0.1x drive strength	VDDHn = 1.8 V	3.1	3.8	4.8	mA
I_{SNK_0p1DS}	Output sink current, 0.1x drive strength	VDDHn = 1.8 V	3.5	4.5	6.0	mA
I_{SRC_0p5DS}	Output source current, 0.5x drive strength	VDDHn = 1.8 V	15.6	18.9	23.9	mA
I_{SNK_0p5DS}	Output sink current, 0.5x drive strength	VDDHn = 1.8 V	13.9	18.0	24.0	mA
I_{SRC_0p75DS}	Output source current, 0.75x drive strength	VDDHn = 1.8 V	25.0	30.3	38.3	mA
I_{SNK_0p75DS}	Output sink current, 0.75x drive strength	VDDHn = 1.8 V	20.8	27.0	35.9	mA
I_{SRC_1p0DS}	Output source current, 1.0x drive strength	VDDHn = 1.8 V	31.2	37.8	47.8	mA
I_{SNK_1p0DS}	Output sink current, 1.0x drive strength	VDDHn = 1.8 V	27.8	36.0	47.9	mA
Skinny GPIOs						
I_{SRC_0p1DS}	Output source current, 0.1x drive strength	VDDHn = 1.8 V	3.1	3.8	4.8	mA
I_{SNK_0p1DS}	Output sink current, 0.1x drive strength	VDDHn = 1.8 V	3.5	4.5	6.0	mA
I_{SRC_0p5DS}	Output source current, 0.5x drive strength	VDDHn = 1.8 V	15.6	18.9	23.9	mA
I_{SNK_0p5DS}	Output sink current, 0.5x drive strength	VDDHn = 1.8 V	13.9	18.0	24.0	mA
High-speed GPIOs: VDDHn = 1.8 V						
V_{OH}	High-Level output Voltage	VDDHn = 1.8 V	0.8 x VDDHn	-		V
V_{OL}	Low-Level output Voltage	VDDHn = 1.8 V		-	0.2 x VDDHn	V
V_{IH}	Positive going input threshold voltage	VDDHn = 1.8 V	0.7 x VDDHn	-	-	V
V_{IL}	Negative going input threshold voltage	VDDHn = 1.8 V	-	-	0.3 x VDDHn	V
V_{HYS}	Input Hysteresis	VDDHn = 1.8 V	0.12	0.14	0.16	V
R_{PD}	PULL DOWN resistance	VDDHn = 1.8 V	42.6	51.5	60.1	kΩ
R_{PU}	PULL UP resistance	VDDHn = 1.8 V	42.7	51.4	60.0	kΩ
C_{GPI}	Input capacitance	VDDHn = 1.8 V	-	5		pF
I_{IN}	Input pin leakage current	VDDHn = 1.8 V	-	1	20	nA

Table 46: General Purpose Input/Output (GPIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{INOD}	Open drain output leakage current	VDDHn = 1.8 V	-	1	20	nA
$I_{SRC\_HS\_0p125DS}$	Output source current, 0.12x drive strength	VDDHn = 1.8V, 0.8 x VDDH	8.2	9.7	11.8	mA
$I_{SNK\_HS\_0p125DS}$	Output sink current, 0.12x drive strength	VDDHn = 1.8V, 0.2 x VDDH	8.1	9.9	12.5	mA
$I_{SRC\_HS\_0p25DS}$	Output source current, 0.25x drive strength	VDDHn = 1.8V, 0.8 x VDDH	16.5	19.4	23.5	mA
$I_{SNK\_HS\_0p25DS}$	Output sink current, 0.25x drive strength	VDDHn = 1.8V, 0.2 x VDDH	16.1	19.7	25.0	mA
$I_{SRC\_HS\_0p375DS}$	Output source current, 0.37x drive strength	VDDHn = 1.8V, 0.8 x VDDH	24.7	29.1	35.3	mA
$I_{SNK\_HS\_0p375DS}$	Output sink current, 0.37x drive strength	VDDHn = 1.8V, 0.2 x VDDH	24.2	29.6	37.6	mA
$I_{SRC\_HS\_0p5DS}$	Output source current, 0.5x drive strength	VDDHn = 1.8V, 0.8 x VDDH	33.0	38.9	47.0	mA
$I_{SNK\_HS\_0p5DS}$	Output sink current, 0.5x drive strength	VDDHn = 1.8V, 0.2 x VDDH	32.2	39.5	50.0	mA
$I_{SRC\_HS\_0p625DS}$	Output source current, 0.63x drive strength	VDDHn = 1.8V, 0.8 x VDDH	41.2	48.6	58.8	mA
$I_{SNK\_HS\_0p62DS}$	Output sink current, 0.63x drive strength	VDDHn = 1.8V, 0.2 x VDDH	40.3	49.3	62.6	mA
$I_{SRC\_HS\_0p75DS}$	Output source current, 0.75x drive strength	VDDHn = 1.8V, 0.8 x VDDH	49.5	58.3	70.6	mA
$I_{SNK\_HS\_0p75DS}$	Output sink current, 0.75x drive strength	VDDHn = 1.8V, 0.2 x VDDH	48.4	59.2	75.0	mA
$I_{SRC\_HS\_0p875DS}$	Output source current, 0.88x drive strength	VDDHn = 1.8V, 0.8 x VDDH	57.8	68.0	82.3	mA
$I_{SNK\_HS\_0p875DS}$	Output sink current, 0.88x drive strength	VDDHn = 1.8V, 0.2 x VDDH	56.4	69.0	87.6	mA
$I_{SRC\_HS\_1p0DS}$	Output source current, 1.0x drive strength	VDDHn = 1.8V, 0.8 x VDDH	66.0	77.7	94.1	mA
$I_{SNK\_HS\_1p0DS}$	Output sink current, 1.0x drive strength	VDDHn = 1.8V, 0.2 x VDDH	64.5	78.9	100.0	mA
High-speed GPIOs: VDDHn = 1.2 V						
V_{OH}	High-Level output Voltage	VDDHn = 1.2 V	0.8 x VDDHn	-	-	V
V_{OL}	Low-Level output Voltage	VDDHn = 1.2 V	-	-	0.2 x VDDHn	V
V_{IH}	Positive going input threshold voltage	VDDHn = 1.2 V	0.7 x VDDHn	-	-	V
V_{IL}	Negative going input threshold voltage	VDDHn = 1.2 V	-	-	0.3 x VDDHn	V
V_{HYS}	Input Hysteresis	VDDHn = 1.2 V	0.07	0.09	0.11	V
R_{PD}	PULL DOWN resistance	VDDHn = 1.2 V	43.1	52.1	60.9	kΩ
R_{PU}	PULL UP resistance	VDDHn = 1.2 V	43.8	52.8	61.5	kΩ

Table 46: General Purpose Input/Output (GPIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{GPI}	Input capacitance	VDDHn = 1.2 V	-	5	-	pF
I_{IN}	Input pin leakage current	VDDHn = 1.2 V	-	1	20	nA
I_{INOD}	Open drain output leakage current	VDDHn = 1.2 V	-	1	20	nA
$I_{SRC\_HS\_0p125DS}$	Output source current, 0.12x drive strength	VDDHn = 1.2V, 0.8 x VDDH	2.9	3.6	4.5	mA
$I_{SNK\_HS\_0p125DS}$	Output sink current, 0.12x drive strength	VDDHn = 1.2V, 0.2 x VDDH	2.7	3.7	5.1	mA
$I_{SRC\_HS\_0p25DS}$	Output source current, 0.25x drive strength	VDDHn = 1.2V, 0.8 x VDDH	5.9	7.2	9.1	mA
$I_{SNK\_HS\_0p25DS}$	Output sink current, 0.25x drive strength	VDDHn = 1.2V, 0.2 x VDDH	5.5	7.5	10.2	mA
$I_{SRC\_HS\_0p375DS}$	Output source current, 0.37x drive strength	VDDHn = 1.2V, 0.8 x VDDH	8.9	10.8	13.6	mA
$I_{SNK\_HS\_0p375DS}$	Output sink current, 0.37x drive strength	VDDHn = 1.2V, 0.2 x VDDH	8.3	11.2	15.3	mA
$I_{SRC\_HS\_0p5DS}$	Output source current, 0.5x drive strength	VDDHn = 1.2V, 0.8 x VDDH	11.9	14.4	18.1	mA
$I_{SNK\_HS\_0p5DS}$	Output sink current, 0.5x drive strength	VDDHn = 1.2V, 0.2 x VDDH	11.1	15.0	20.4	mA
$I_{SRC\_HS\_0p625DS}$	Output source current, 0.63x drive strength	VDDHn = 1.2V, 0.8 x VDDH	14.8	18.0	22.6	mA
$I_{SNK\_HS\_0p62DS}$	Output sink current, 0.63x drive strength	VDDHn = 1.2V, 0.2 x VDDH	13.9	18.7	25.5	mA
$I_{SRC\_HS\_0p75DS}$	Output source current, 0.75x drive strength	VDDHn = 1.2V, 0.8 x VDDH	17.8	21.6	27.2	mA
$I_{SNK\_HS\_0p75DS}$	Output sink current, 0.75x drive strength	VDDHn = 1.2V, 0.2 x VDDH	16.7	22.4	30.6	mA
$I_{SRC\_HS\_0p875DS}$	Output source current, 0.88x drive strength	VDDHn = 1.2V, 0.8 x VDDH	20.8	25.3	31.7	mA
$I_{SNK\_HS\_0p875DS}$	Output sink current, 0.88x drive strength	VDDHn = 1.2V, 0.2 x VDDH	19.5	26.2	35.7	mA
$I_{SRC\_HS\_1p0DS}$	Output source current, 1.0x drive strength	VDDHn = 1.2V, 0.8 x VDDH	23.8	28.9	36.2	mA
$I_{SNK\_HS\_1p0DS}$	Output sink current, 1.0x drive strength	VDDHn = 1.2V, 0.2 x VDDH	22.3	29.9	40.8	mA

1. All GPIOs have Schmitt trigger inputs.
2. The designation “n” corresponds to the voltage source for the pin, e.g., VDDH1.

Table 47 lists the rise and fall times based on drive strengths and slew rate (SR) settings for each of the GPIO pad types.

Table 47: General Purpose Input/Output (GPIO) - Rise/Fall Times

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Standard (GPIO_TOP_LP_V, GPIO_TOP_LP_H) or Skinny (Skinny_GPIO_TOP_LP_V, Skinny_GPIO_TOP_LP_H) GPIOs[1]						
- GPIO_TOP_LP_V						
$T_{RISE\_STD\_0P1X}$	Rise time, 35 pF load, 0.1x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	33.56	-	ns
$T_{FALL\_STD\_0P1X}$	Fall time, 35 pF load, 0.1x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	31.00	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 35 pF load, 0.5x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	4.81	-	ns
$T_{FALL\_STD\_0P5X}$	Fall time, 35 pF load, 0.5x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	6.26	-	ns
$T_{RISE\_STD\_0P75X}$	Rise time, 35 pF load, 0.75x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	3.31	-	ns
$T_{FALL\_STD\_0P75X}$	Fall time, 35 pF load, 0.75x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	3.80	-	ns
$T_{RISE\_STD\_1P0X}$	Rise time, 35 pF load, 1.0x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	3.04	-	ns
$T_{FALL\_STD\_1P0X}$	Fall time, 35 pF load, 1.0x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	3.08	-	ns
$T_{RISE\_STD\_0P1X}$	Rise time, 35 pF load, 0.1x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	35.96	-	ns
$T_{FALL\_STD\_0P1X}$	Fall time, 35 pF load, 0.1x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	34.28	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 35 pF load, 0.5x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	7.03	-	ns
$T_{FALL\_STD\_0P5X}$	Fall time, 35 pF load, 0.5x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	9.05	-	ns
$T_{RISE\_STD\_0P75X}$	Rise time, 35 pF load, 0.75x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	4.48	-	ns
$T_{FALL\_STD\_0P75X}$	Fall time, 35 pF load, 0.75x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	6.09	-	ns
$T_{RISE\_STD\_1P0X}$	Rise time, 35 pF load, 1.0x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	4.12	-	ns
$T_{FALL\_STD\_1P0X}$	Fall time, 35 pF load, 1.0x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	4.89	-	ns
- GPIO_TOP_LP_H						
$T_{RISE\_STD\_0P1X}$	Rise time, 35 pF load, 0.1x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	26.97	-	ns
$T_{FALL\_STD\_0P1X}$	Fall time, 35 pF load, 0.1x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	23.85	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 35 pF load, 0.5x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	4.17	-	ns

Table 47: General Purpose Input/Output (GPIO) - Rise/Fall Times

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{FALL\_STD\_0P5X}$	Fall time, 35 pF load, 0.5x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	4.98	-	ns
$T_{RISE\_STD\_0P75X}$	Rise time, 35 pF load, 0.75x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	2.92	-	ns
$T_{FALL\_STD\_0P75X}$	Fall time, 35 pF load, 0.75x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	3.19	-	ns
$T_{RISE\_STD\_1P0X}$	Rise time, 35 pF load, 1.0x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	2.55	-	ns
$T_{FALL\_STD\_1P0X}$	Fall time, 35 pF load, 1.0x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	2.61	-	ns
$T_{RISE\_STD\_0P1X}$	Rise time, 35 pF load, 0.1x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	29.51	-	ns
$T_{FALL\_STD\_0P1X}$	Fall time, 35 pF load, 0.1x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	27.25	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 35 pF load, 0.5x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	5.62	-	ns
$T_{FALL\_STD\_0P5X}$	Fall time, 35 pF load, 0.5x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	7.13	-	ns
$T_{RISE\_STD\_0P75X}$	Rise time, 35 pF load, 0.75x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	3.99	-	ns
$T_{FALL\_STD\_0P75X}$	Fall time, 35 pF load, 0.75x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	5.00	-	ns
$T_{RISE\_STD\_1P0X}$	Rise time, 35 pF load, 1.0x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	3.61	-	ns
$T_{FALL\_STD\_1P0X}$	Fall time, 35 pF load, 1.0x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	4.28	-	ns
- Skinny_GPIO_TOP_LP_V						
$T_{RISE\_STD\_0P1X}$	Rise time, 40 pF load, 0.1x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	5.32	-	ns
$T_{FALL\_STD\_0P1X}$	Fall time, 40 pF load, 0.1x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	6.80	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 40 pF load, 0.5x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	5.24	-	ns
$T_{FALL\_STD\_0P5X}$	Fall time, 40 pF load, 0.5x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	6.76	-	ns
$T_{RISE\_STD\_0P1X}$	Rise time, 40 pF load, 0.1x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	6.34	-	ns
$T_{FALL\_STD\_0P1X}$	Fall time, 40 pF load, 0.1x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	9.10	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 40 pF load, 0.5x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	6.38	-	ns
$T_{FALL\_STD\_0P5X}$	Fall time, 40 pF load, 0.5x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	9.08	-	ns
- Skinny_GPIO_TOP_LP_H						
$T_{RISE\_STD\_0P1X}$	Rise time, 40 pF load, 0.1x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	1.98	-	ns

Table 47: General Purpose Input/Output (GPIO) - Rise/Fall Times

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{FALL\_STD\_0P1X}$	Fall time, 40 pF load, 0.1x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	2.32	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 40 pF load, 0.5x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	1.96	-	ns
$T_{FALL\_STD\_0P5X}$	Fall time, 40 pF load, 0.5x drive strength, SR = 0, GPIOx	VDDHn = 1.8 V	-	2.27	-	ns
$T_{RISE\_STD\_0P1X}$	Rise time, 40 pF load, 0.1x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	2.65	-	ns
$T_{FALL\_STD\_0P1X}$	Fall time, 40 pF load, 0.1x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	3.43	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 40 pF load, 0.5x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	2.65	-	ns
$T_{FALL\_STD\_0P5X}$	Fall time, 40 pF load, 0.5x drive strength, SR = 1, GPIOx	VDDHn = 1.8 V	-	3.45	-	ns
High-speed GPIOs[2]: VDDHn = 1.8 V						
$T_{RISE\_HS\_0P13X}$	Rise time, 30pF load, 0P12X_0P63X drive strength, SR=0, GPIOx	VDDHn = 1.8V	-	7.50	-	ns
$T_{FALL\_HS\_0P13X}$	Fall time, 30pF load, 0P12X_0P63X drive strength, SR=0, GPIOx	VDDHn = 1.8V	-	7.70	-	ns
$T_{RISE\_HS\_0P25X}$	Rise time, 30pF load, 0P25X_0P75X drive strength, SR=0, GPIOx	VDDHn = 1.8V	-	3.45	-	ns
$T_{FALL\_HS\_0P25X}$	Fall time, 30pF load, 0P25X_0P75X drive strength, SR=0, GPIOx	VDDHn = 1.8V	-	3.40	-	ns
$T_{RISE\_HS\_0P37X}$	Rise time, 30pF load, 0P37X_0P88X drive strength, SR=0, GPIOx	VDDHn = 1.8V	-	2.69	-	ns
$T_{FALL\_HS\_0P37X}$	Fall time, 30pF load, 0P37X_0P88X drive strength, SR=0, GPIOx	VDDHn = 1.8V	-	2.72	-	ns
$T_{RISE\_HS\_0P5X}$	Rise time, 30pF load, 0P5X_1P0X drive strength, SR=0, GPIOx	VDDHn = 1.8V	-	2.56	-	ns
$T_{FALL\_HS\_0P5X}$	Fall time, 30pF load, 0P5X_1P0X drive strength, SR=0, GPIOx	VDDHn = 1.8V	-	2.28	-	ns
$T_{RISE\_HS\_0P63X}$	Rise time, 30pF load, 0P12X_0P63X drive strength, SR=1, GPIOx	VDDHn = 1.8V	-	2.31	-	ns
$T_{FALL\_HS\_0P63X}$	Fall time, 30pF load, 0P12X_0P63X drive strength, SR=1, GPIOx	VDDHn = 1.8V	-	2.04	-	ns
$T_{RISE\_HS\_0P75X}$	Rise time, 30pF load, 0P25X_0P75X drive strength, SR=1, GPIOx	VDDHn = 1.8V	-	2.15	-	ns

Table 47: General Purpose Input/Output (GPIO) - Rise/Fall Times

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{FALL\_HS\_0P75X}$	Fall time, 30pF load, 0P25X_0P75X drive strength, SR=1, GPIOx	VDDHn = 1.8V	-	1.99	-	ns
$T_{RISE\_HS\_0P88X}$	Rise time, 30pF load, 0P37X_0P88X drive strength, SR=1, GPIOx	VDDHn = 1.8V	-	2.06	-	ns
$T_{FALL\_HS\_0P88X}$	Fall time, 30pF load, 0P37X_0P88X drive strength, SR=1, GPIOx	VDDHn = 1.8V	-	1.98	-	ns
$T_{RISE\_HS\_1P0X}$	Rise time, 30pF load, 0P5X_1P0X drive strength, SR=1, GPIOx	VDDHn = 1.8V	-	2.03	-	ns
$T_{FALL\_HS\_1P0X}$	Fall time, 30pF load, 0P5X_1P0X drive strength, SR=1, GPIOx	VDDHn = 1.8V	-	1.84	-	ns
High-speed GPIOs[3]: VDDHn = 1.2 V						
$T_{RISE\_HS\_0P13X}$	Rise time, 30pF load, 0P12X_0P63X drive strength, SR=0, GPIOx	VDDHn = 1.2V	-	12.92	-	ns
$T_{FALL\_HS\_0P13X}$	Fall time, 30pF load, 0P12X_0P63X drive strength, SR=0, GPIOx	VDDHn = 1.2V	-	13.85	-	ns
$T_{RISE\_HS\_0P25X}$	Rise time, 30pF load, 0P25X_0P75X drive strength, SR=0, GPIOx	VDDHn = 1.2V	-	5.38	-	ns
$T_{FALL\_HS\_0P25X}$	Fall time, 30pF load, 0P25X_0P75X drive strength, SR=0, GPIOx	VDDHn = 1.2V	-	5.86	-	ns
$T_{RISE\_HS\_0P37X}$	Rise time, 30pF load, 0P37X_0P88X drive strength, SR=0, GPIOx	VDDHn = 1.2V	-	3.75	-	ns
$T_{FALL\_HS\_0P37X}$	Fall time, 30pF load, 0P37X_0P88X drive strength, SR=0, GPIOx	VDDHn = 1.2V	-	3.70	-	ns
$T_{RISE\_HS\_0P5X}$	Rise time, 30pF load, 0P5X_1P0X drive strength, SR=0, GPIOx	VDDHn = 1.2V	-	2.93	-	ns
$T_{FALL\_HS\_0P5X}$	Fall time, 30pF load, 0P5X_1P0X drive strength, SR=0, GPIOx	VDDHn = 1.2V	-	3.04	-	ns
$T_{RISE\_HS\_0P63X}$	Rise time, 30pF load, 0P12X_0P63X drive strength, SR=1, GPIOx	VDDHn = 1.2V	-	2.77	-	ns
$T_{FALL\_HS\_0P63X}$	Fall time, 30pF load, 0P12X_0P63X drive strength, SR=1, GPIOx	VDDHn = 1.2V	-	2.76	-	ns
$T_{RISE\_HS\_0P75X}$	Rise time, 30pF load, 0P25X_0P75X drive strength, SR=1, GPIOx	VDDHn = 1.2V	-	2.60	-	ns

Table 47: General Purpose Input/Output (GPIO) - Rise/Fall Times

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{FALL\_HS\_0P75X}$	Fall time, 30pF load, 0P25X_0P75X drive strength, SR=1, GPIOx	VDDHn = 1.2V	-	2.35	-	ns
$T_{RISE\_HS\_0P88X}$	Rise time, 30pF load, 0P37X_0P88X drive strength, SR=1, GPIOx	VDDHn = 1.2V	-	2.41	-	ns
$T_{FALL\_HS\_0P88X}$	Fall time, 30pF load, 0P37X_0P88X drive strength, SR=1, GPIOx	VDDHn = 1.2V	-	2.31	-	ns
$T_{RISE\_HS\_1P0X}$	Rise time, 30pF load, 0P5X_1P0X drive strength, SR=1, GPIOx	VDDHn = 1.2V	-	2.22	-	ns
$T_{FALL\_HS\_1P0X}$	Fall time, 30pF load, 0P5X_1P0X drive strength, SR=1, GPIOx	VDDHn = 1.2V	-	2.09	-	ns

1. All GPIOs have Schmitt trigger inputs.
2. For High-speed GPIO pads, if SR is set to 0 then the DS is the first value, e.g., 0P12X_0P63X means DS = 0.12x full strength. If SR is set to 1 then the DS is the second value, e.g., 0P12X_0P63X means DS = 0.63 x full strength.
3. For High-speed GPIO pads, if SR is set to 0 then the DS is the first value, e.g., 0P12X_0P63X means DS = 0.12x full strength. If SR is set to 1 then the DS is the second value, e.g., 0P12X_0P63X means DS = 0.63 x full strength.

30.7 Clocks/Oscillators

Table 48: Primary Internal Clocks

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{HFRC_LP}	HFRC frequency - Low Power		-	96	-	MHz
F_{HFRC_HP}	HFRC frequency - High Performance Burst Mode		-	192[1]	-	MHz
DC_{HFRC}	HFRC duty cycle		-	50	-	%
F_{HFRC2_LP}	HFRC2 frequency - Low Power		-	125	-	MHz
F_{HFRC2_HP}	HFRC2 frequency - High Performance Burst Mode		-	250[2]	-	MHz
F_{LFRC}	LFRC frequency		-	887	-	Hz
DC_{LFRC}	LFRC duty cycle	CLKGEN_CLKOUT_CKSEL = LFRC_DIV2	-	50	-	%
F_{PLL_OUT}	System PLL output frequency		1.22	-	48	MHz
$F_{PLL\_IN\_INT}$	System PLL input frequency - Integer Mode		1	-	48	MHz
$F_{PLL\_IN\_FRAC}$	System PLL input frequency - Fractional Mode		10	-	48	MHz
$ACC_{PLL\_OUT\_FRAC}$	System PLL output accuracy - Fractional Mode		-	24	-	bit
$Jitter_{PLL\_OUT\_INT}$	Maximum integrated jitter (10 kHz to Nyquist) - Integer Mode[3]		-	-	15	ps
$Jitter_{PLL\_OUT\_FRAC}$	Maximum integrated jitter (10 kHz to Nyquist) - Fractional Mode[1]		-	-	30	ps

1. The HFRC oscillator frequency is used to supply the 192 MHz HFRC_HP clock and is divided by 2 to provide the 96 MHz HFRC_LP clock.
2. The HFRC2 oscillator frequency is used to supply the 250 MHz HFRC2_HP clock and is further divided by 2 to provide the 125 MHz HFRC2_LP clock.
3. This is PLL jitter only and actual jitter seen on clock sinks, either internal or external, will be higher as it includes the jitter added by clocks routings.

Table 49: Low-Frequency Crystal Oscillator

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{XT}	XT frequency		-	32.768	-	kHz
DC_{XT}	XT duty cycle		50	56	60	%
ΔFXTAL	Frequency tolerance[1]	Untrimmed; include initial tolerance/aging/ temperature drift	-50	-	50	PPM
ESR	Equivalent serial resistance		-	-	90	KΩ
$C_{EXT\_XT\_LOAD}$	Allowed external XI/XO load capacitance per pin[2]		-	-	10	pF

1. Recommended to achieve target internal clock frequencies which use the XTAL as reference clock

2. If oscillator allowance (≥ 4x) is insufficient after adding the load caps, the XTALGENCTRL_XTALBIASTRIM field value in MCUCTRL can be increased to help increase the allowance. Default value for this field is 0x38 and can be increased as high as 0x3F (about a 12% increase in bias current).

Table 50: High-Speed Crystal Oscillator

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{XTAL}	Crystal frequency		-	48	-	MHz
ΔFXTAL	Frequency deviation	Including frequency tolerance, stability over temperature, aging, and total tolerances of external capacitances	-	-	±50	PPM
ESR	Equivalent serial resistance		-	-	60	Ω
CL_{XTAL}	Differential equivalent load capacitance		8	10	11	pF

Tuning capacitance range for the high-frequency XTAL is from 5 pF to 13.5 pF. There are six trimming bits for the on-chip capacitance with 64 steps.

30.8 Counter/Timer (TIMER)

Table 51: Timer (TIMER)

Symbol	Parameter	Min	Typ	Max	Unit
F_{TIMER}	Input frequency	-	-	48	MHz

30.9 Bluetooth Low Energy Controller

Table 52: Supply Voltage Specifications

Symbol	Setting	Min	Typ	Max	Unit
T_{CS}	Cold Start Duration[1] (VBAT2 >= 1.5V, ramp=0.3 V/µs, LF RC, 1 ms precharge)	-	3.9	-	ms

1. Cold Start time is defined as the time from ENABLE pin high until RDY SPI pin high, when the device is ready to receive an HCI command. Assumes a SPI transport layer is used; power configuration is either Step Up or Voltage Multiplier.

Table 53: Supported Data Rates

Symbol	Setting	Min	Typ	Max	Unit
R_{1MBPS}	BLE 1 Mbps PHY		1000		kbps
R_{2MBPS}	BLE 2 Mbps PHY		2000		kbps
$R_{LR125KBPS}$	BLE Coded LR at 125 kbps (S=8)		125		kbps
$R_{LR500KBPS}$	BLE Coded LR at 500 kbps (S=2)		500		kbps

Table 54: General Transmitter Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Unit
$P_{OUT(MIN)}$	Minimum output power		-	-20	-	dBm
$P_{OUT(MAX)}$	Maximum output power	Power setting = 6	-	6	-	dBm
P_0 P_3 P_4 P_5 P_6	Output power[1]	Power setting = 0, $V_{BAT2} \geq 1.1$ V Power setting = 3, $V_{BAT2} \geq 1.25$ V Power setting = 4, $V_{BAT2} \geq 1.35$ V Power setting = 5, $V_{BAT2} \geq 1.5$ V Power setting = 6, $V_{BAT2} \geq 1.73$ V	-	0 3 4 5 6	-	dBm dBm dBm dBm dBm
P_{TX_H2}	Out-of-band emission in 2nd harmonic	Power setting = 6, step-up configuration	-	-45	-	dBm
P_{TX_H3}	Out-of-band emission in 3rd harmonic	Power setting = 6, step-up configuration	-	-48	-	dBm
P_{TX_H4}	Out-of-band emission in 4th harmonic	Power setting = 6, step-up configuration	-	-51	-	dBm
$P_{out(fc+foff)}$	In-band spurious emission	1 Mbps, $\lvert f_{off} \rvert$ = 2 MHz 1 Mbps, $\lvert f_{off} \rvert$ = 3 MHz 2 Mbps, $\lvert f_{off} \rvert$ = 4 MHz 2 Mbps, $\lvert f_{off} \rvert$ = 5 MHz	-	-50 -60 -55 -60	-	dBm dBm dBm dBm
	Spurious emissions	f = 30 MHz – 88 MHz f = 88 MHz – 1 GHz f = 1 GHz – 12.75 GHz	-	-70 -68 -45	-	dBm dBm dBm
f_{RF}	Carrier frequency		2402	-	2480	MHz
Δf_c	Deviation from the channel center frequency		-150	-	150	kHz
Δf_{c_pkt}	Frequency drift for any packet length		-50	-	50	kHz
$\Delta f_c/\Delta T$	Drift rate		-	-	400	Hz/µs
Δf_{mod}	Modulated frequency deviation	2 Mbps 1 Mbps and lower	-	±500 ±250	-	kHz

1. Power level P_6 (6dBm transmit power) is the highest power level supported.

Table 55: General Receiver Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Unit
$RCVR_{SENS}$	Sensitivity	2 Mbps, 37 byte payload, BER = 1^{e-3} 2 Mbps, 255 byte payload, BER = 1^{e-3} 1 Mbps, 37 byte payload, BER = 1^{e-3} 1 Mbps, 255 byte payload, BER = 1^{e-3} 500 kbps, 37 byte payload, BER = 1^{e-3} 500 kbps, 255 byte payload, BER = 1^{e-3} 125 kbps, 37 byte payload, BER = 1^{e-3} 125 kbps, 255 byte payload, BER = 1^{e-3}	-	-94 -93 -97 -96 -100 -99 -103 -102	-	dBm dBm dBm dBm dBm dBm dBm dBm
$P_{IN(MAX)}$	Maximum input power		-	-	6.5	dBm
C/I_0 $C/I_{\pm1}$ C/I_{+2} C/I_{-2} C/I_{+3} C/I_{-3} C/I_{4-10} $C/I_{\geq10}$	In-band blocking (-67 dBm desired signal)	Co-channel interference (i.e., 0 MHz) Adjacent ±1 MHz interference Adjacent +2 MHz interference Adjacent -2 MHz interference (image) Adjacent +3 MHz interference Adjacent -3 MHz interference (next to image) Adjacent ≥ ±4 MHz and ≤ ±10 MHz interference Adjacent ≥ ±10 MHz interference	-	9 -2 -45 -25 -48 -40 -45 -50	-	dB dB dB dB dB dB dB dB
$BLOCKING_{30\_2000MHz}$ $BLOCKING_{2003\_2399MHz}$ $BLOCKING_{2484\_2997MHz}$ $BLOCKING_{3000\_12750MHz}$	Out-of-band blocking (-67 dBm desired signal)	30 MHz – 2000 MHz 2003 MHz – 2399 MHz (excepted for f_{RF} - 96 MHz) 2484 MHz – 2997 MHz (excepted for f_{RF} + 96 MHz) 3000 MHz – 12.75 GHz	-24 -29 -29 -24	-3 -15 -10 -3	-	dBm dBm dBm dBm
$INTERMOD_{1Mbps}$	Intermodulation @1 Mbps	f_{RX}=2 x (f_1-f_2) and f_2-f_1=±3 MHz / ±4 MHz /±6 MHz	-	-27	-	dBm
$INTERMOD_{2Mbps}$	Intermodulation @2 Mbps	f_{RX}=2 x (f_1-f_2) and f_2-f_1=±6 MHz / ±8 MHz /±10 MHz	-	-28	-	dBm

30.10 General Purpose Analog-to-Digital Converter (ADC)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{ADCCLK}	ADC Clock Frequency		-	24/48	-	MHz
ANALOG INPUT						
V_{ADCINN}	Maximum safe Input voltage range		0	-	VDDH	V
V_{ADCREF}	Internal reference voltage range		-	1.2	-	V
C_{ADCIN}	Input source capacitance		-	2	-	pF
SAMPLING DYNAMICS						
RES	Resolution		8	-	12	bit
F_{ADCONV}	Conversion rate[1]		-	2.0 (12 b) 2.4 (10 b) 2.8 (8 b)	-	MS/s
TTRIG_W-START_LP1_REF0	Delay from warm start trigger to start of scan, LPMODE1	LPMODE1	-	57	-	µs
TTRIG_W-START_LP0_REF0	Delay from warm start trigger to start of scan, LPMODE0	LPMODE0	-	0	-	µs
TSNGLSLOT_SCNC-MP_PM12	Delay from scan start to scan complete, precision mode 12	Precision Mode 12	-	24	-	cycles
TSNGLSLOT_SCNC-MP_PM10	Delay from scan start to scan complete, precision mode 10	Precision Mode 10	-	20	-	cycles
TSNGLSLOT_SCNC-MP_PM8	Delay from scan start to scan complete, precision mode 8	Precision Mode 8	-	17	-	cycles
DYNAMIC CHARACTERISTICS, Internal 2.0 V Reference (Buck Mode, Single Ended Input, 1 kHz Input, ADC Running in 12-bit Mode)						
ENOB	Effective number of bits	1.8V	-	9.02	-	ENOB
THD_{ADC}	Total harmonic distortion (THD) - 1st 7 harmonics	1.8V	-	-78	-	dB
SNR_{ADC}	Signal-to-noise ratio (SNR)	1.8V	-	57.8	-	dB
$SFDR_{ADC}$	Spurious-free dynamic range (SFDR)	1.8V	-	TBD	-	dB
$SINAD_{ADC}$	Signal-to-noise and distortion ratio (SINAD)	1.8V	-	56.1	-	dB
PERFORMANCE						
NMC_{ADC}	Number of missing codes		-	0	-	Codes
INL_{ADC}	Integral nonlinearity	Full input range	-	± 3.5	-	LSB
DNL_{ADC}	Differential nonlinearity	Full input range	-	[-0.97, 2.3]	-	LSB
E_{ADC_OFFSET}	Offset error		-1	-	1	%FS
E_{ADC_GAIN}	Gain error		-2	-	2	%FS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
INTERNAL TEMPERATURE SENSOR						
E_{TEMP}	Temperature sensor accuracy	10-bit resolution	-	± 3.5	-	°C
S_{TEMP}	Temperature sensor slope		-	3.3	-	mV/°C
BATTERY VOLTAGE MEASUREMENT						
$V_{BATTDIV}$	Battery divider voltage		0.324 * VDDH	0.338 * VDDH	0.342 * VDDH	V

1. Refer to Errata List for any known device issues which may impact the achievable conversion rate.

30.11 Display Controller (DC)

30.11.1 DC QSPI/SPI Interface

Timing characteristics have been determined by measurements on chip.

Table 56: DC QSPI/SPI Timing[1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$F_{SCLK(OUT)}$	SCLK OUT frequency		-	-	48[2]	MHz
$T_{LOW(SCLK)}$	Clock low time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	DS = 1.0x, 30 pF load	-	1.4	-	ns
$T_{FALL(SCLK)}$	Clock fall time	DS = 1.0x, 30 pF load	-	1.6	-	ns
$T_{SETUP(IN)}$	Data input data setup time		40	-	-	ns
$T_{HOLD(in)}$	Data input data hold time		1	-	-	ns
$T_{HOLD(OUT)}$	Data output data hold time		-1	-	-	ns
$T_{VALID(OUT)}$	Data output data valid time	DS = 1.0x, 30 pF load	-	-	5	ns

1. The CE pin is assumed to be controlled by SW.
2. Max clock frequency setting using HFRC clock source. Note that the specified $T_{VALID(OUT)}$ time of 5 ns exceeds a half cycle of 96 MHz clock. If the external SPI peripheral supports full-cycle data capture, then a 96 MHz clock is supported provided it can meet the hold time requirement with the $T_{HOLD(OUT)}$ of -1ns. It is recommended that customers perform compliance testing in their systems to ensure reliable operation.

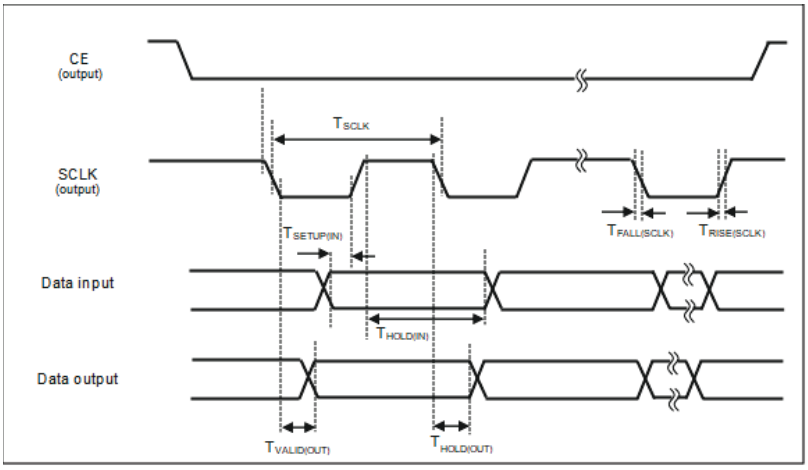


Figure 64. DC QSPI/SPI Timing Diagram

30.12 Multi-bit Serial Peripheral Interface (MSPI)

The following sections provide timing specifications for the MSPI modules.

For MSPI0 timings, the specifications cover nominal 1.2 V and 1.8 V operation. For MSPI1 timings, the specifications cover nominal 1.8 V operation.

Timing characteristics for have been derived through simulations.

Table 57: MSPI General Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{DLY\_STEP\_SIZE}$	DDR Delay Step Size		80	-	200	ps

30.12.1 Standard 4-Wire Serial and SDR Non-DQS SPI Modes - Both MSPIs

For Standard 4-Wire Serial SPI Manager Mode, the following timing specifications assume that the MSPI is configured to use the same SCLK edge to launch MOSI and to capture MISO. This allows maximum speed to be achieved in serial SPI mode. If the MSPI is configured to follow the standard SPI timing mode, using a different SCLK edge to launch MOSI and to capture MISO, the setup and hold times of MISO is the same, but now with respect to the configured SCLK capture edge.

For SDR Non-DQS Mode, the following specifications cover QuadSPI (x4) data width. To use on-chip RX delay lines, the external data skew needs to be less than or equal to 4.0 ns. Timing parameters are applicable for the MSPI's voltage rail as defined above.

Timing characteristics have been determined by measurements on chip.

Table 58: 4-Wire Serial and SDR Non-DQS Mode Timing (Both MSPIs)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	96	MHz
T_{SCLK_LO}	Clock low time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
T_{SCLK_HI}	Clock high time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load, GPIO Drive Strength=0.5x	-	1.0	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load, GPIO Drive Strength=0.5x	-	1.4	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$3.0/F_{SCLK}$	s
$T_{SETUP(IN)}$	MISO/Data input setup time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	3.4	-	-	ns

Table 58: 4-Wire Serial and SDR Non-DQS Mode Timing (Both MSPIs)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
$T_{HOLD(IN)}$	MISO/Data input hold time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	0	-	-	ns
$T_{HOLD(OUT)}$	MOSI/Data output hold time	15 pF Load, GPIO Drive Strength=0.5x	-2.3	-	-	ns
$T_{VALID(OUT)}$	MOSI/Data output valid time	15 pF Load, GPIO Drive Strength=0.5x	-	-	2.0	ns

1. Turnaround set per memory target specification.

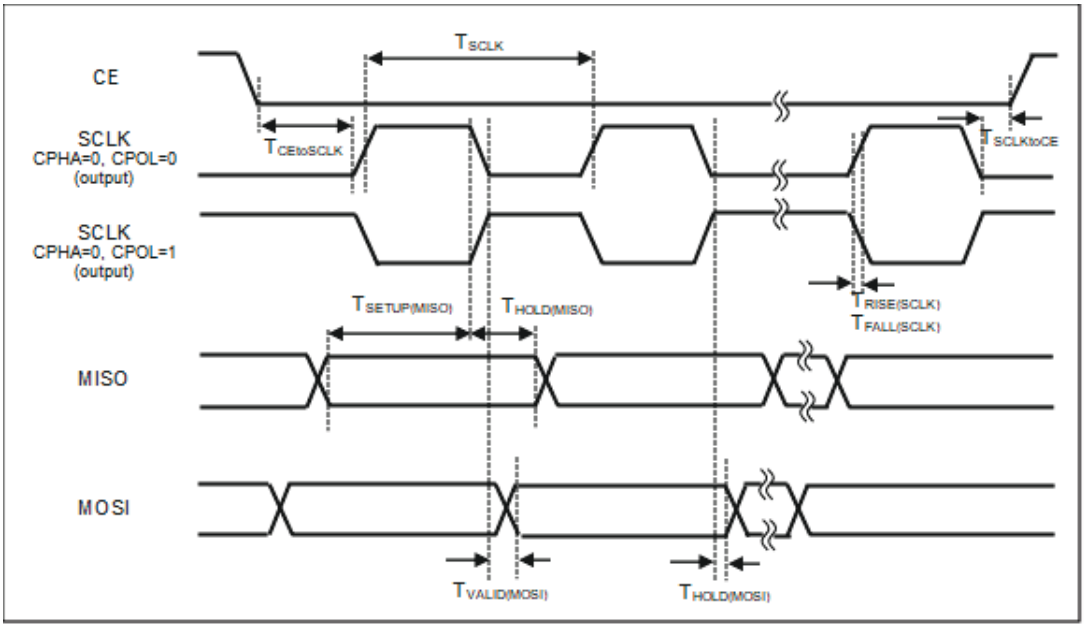


Figure 65. Standard 4-Wire Mode Timing Diagram - SPI Manager, CPHA=0 (Both MSPIs)

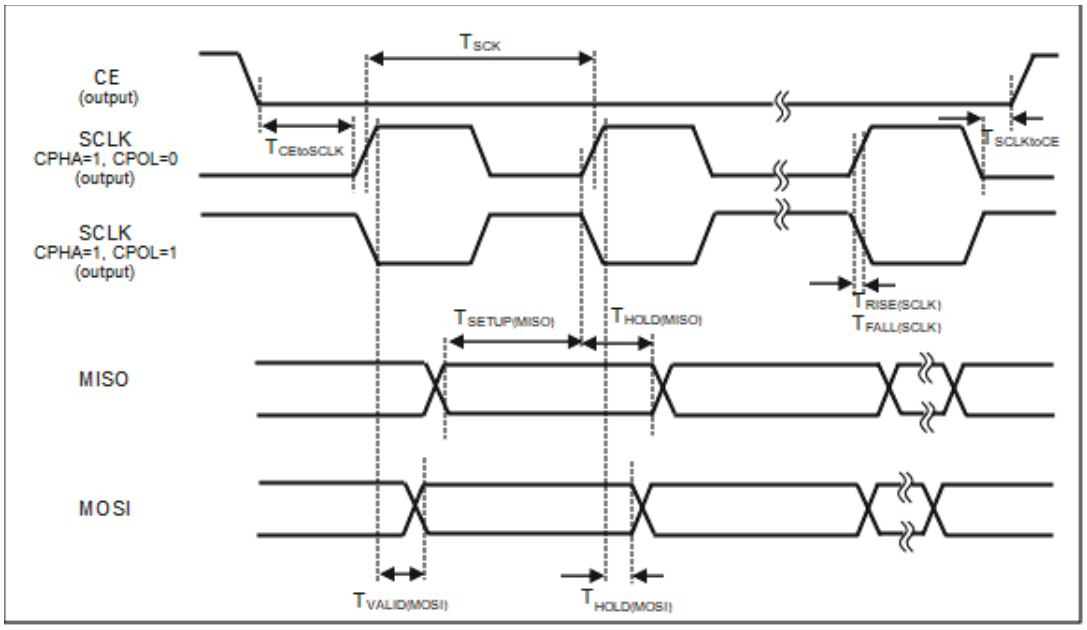


Figure 66. Standard 4-Wire Mode Timing Diagram - SPI Manager, CPHA=1 (Both MSPIs)

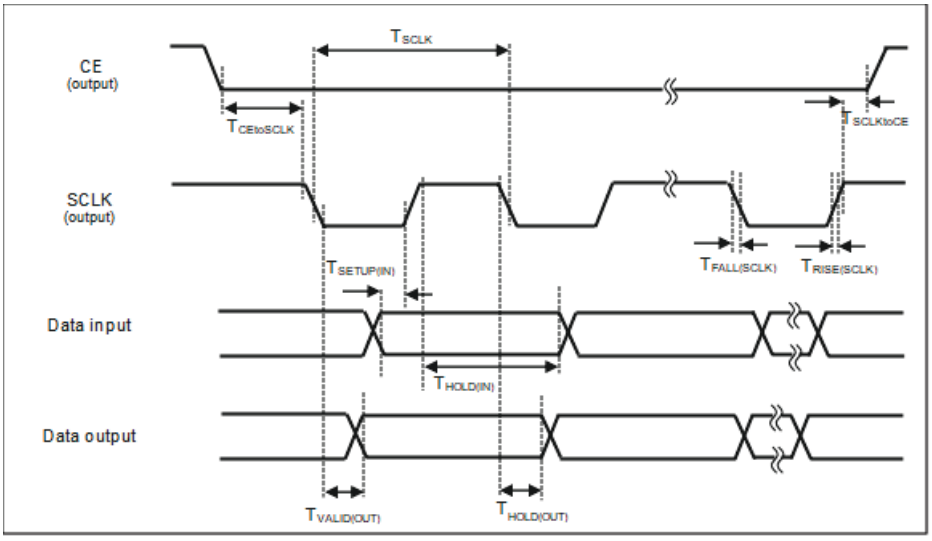


Figure 67. SDR Non-DQS Mode Timing Diagram (Both MSPIs)

30.12.2 MSPI0 DDR with DQS Mode (All Supported Data Widths)

The following specifications for MSPI0 cover all supported data widths from QuadSPI (x4) up to HexSPI (x16).

To use on-chip RX delay lines, the external data skew needs to be less than or equal to 1.6 ns.

Timing parameters are applicable to both 1.2V and 1.8V nominal I/O voltage.

Timing characteristics have been determined by measurements on chip.

Table 59: MSPI0 Timing - DDR with DQS Mode

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	125	MHz
T_{SCLK_LO}	Clock low time	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK)	$0.46/F_{SCLK}$	-	$0.54/F_{SCLK}$	s
T_{SCLK_HI}	Clock high time	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK)	$0.46/F_{SCLK}$	-	$0.54/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK)	-	1	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK)	-	1.6	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK)	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK)	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SETUP(IN)}$	Data input setup time	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK), TURNAROUND0=10, TXDQSDLY=0, RXDQSDLY=7	0.6	-	-	ns
$T_{HOLD(IN)}$	Data input hold time	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK), TURNAROUND0=10, TXDQSDLY=0, RXDQSDLY=7	2	-	-	ns
$T_{HOLD(OUT)}$	Data output hold time	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK)	$(0.225/F_{SCLK}) - 0.9(10)^{-9}$	-	-	s
$T_{VALID(OUT)}$	Data output valid time	15 pF Load, GPIO Drive Strength=1.0x (Data) / 0.75x (DQS/CE/CLK)	-	-	$(0.275/F_{SCLK}) + 0.9(10)^{-9}$	s

1. Turnaround set per memory target specification. RXDQS/TXDQS delay values determined by timing scan. See AmbiqSuite SDK for more details.

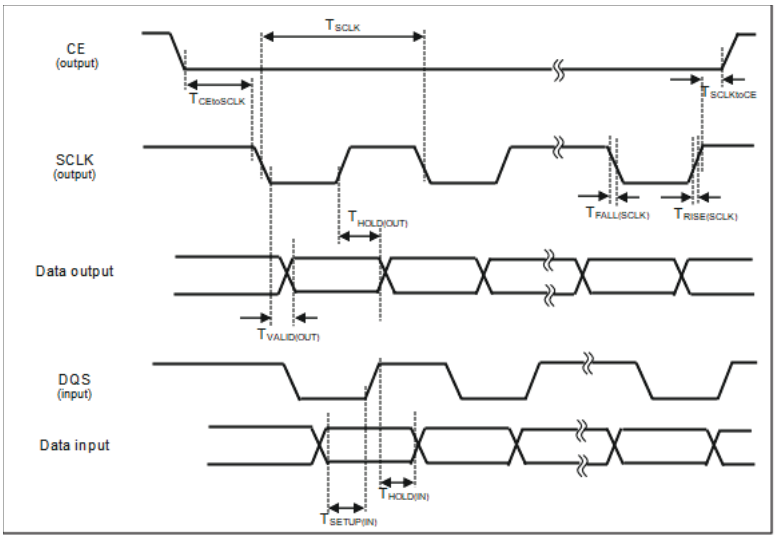


Figure 68. MSPI0 DDR with DQS Mode Timing Diagram

30.12.3 MSPI1 DDR with DQS Mode (All Supported Data Widths)

The following specifications for MSPI1 cover data widths QuadSPI (x4) and OctalSPI (x8).

To use on-chip RX delay lines, the external data skew needs to be less than or equal to 4.0 ns.

Timing parameters are applicable to 1.8 V nominal I/O voltage for MSPI1.

Timing characteristics have been determined by measurements on chip..

Table 60: MSPI1 Timing - DDR with DQS Mode

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	48	MHz
T_{SCLK_LO}	Clock low time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
T_{SCLK_HI}	Clock high time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load, GPIO Drive Strength=0.5x	-	1.5	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load, GPIO Drive Strength=0.5x	-	1.7	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SETUP(IN)}$	Data input setup time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=0, RXDQSDELAY=6	1.5	-	-	ns
$T_{HOLD(IN)}$	Data input hold time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=0, RXDQSDELAY=6	2.5	-	-	ns
$T_{HOLD(OUT)}$	Data output hold time	15 pF Load, GPIO Drive Strength=0.5x	$(0.225/F_{SCLK}) - 0.3(10)^{-9}$	-	-	s
$T_{VALID(OUT)}$	Data output valid time	15 pF Load, GPIO Drive Strength=0.5x	-	-	$(0.275/F_{SCLK}) + 2.9(10)^{-9}$	s

1. Turnaround set per memory target specification.

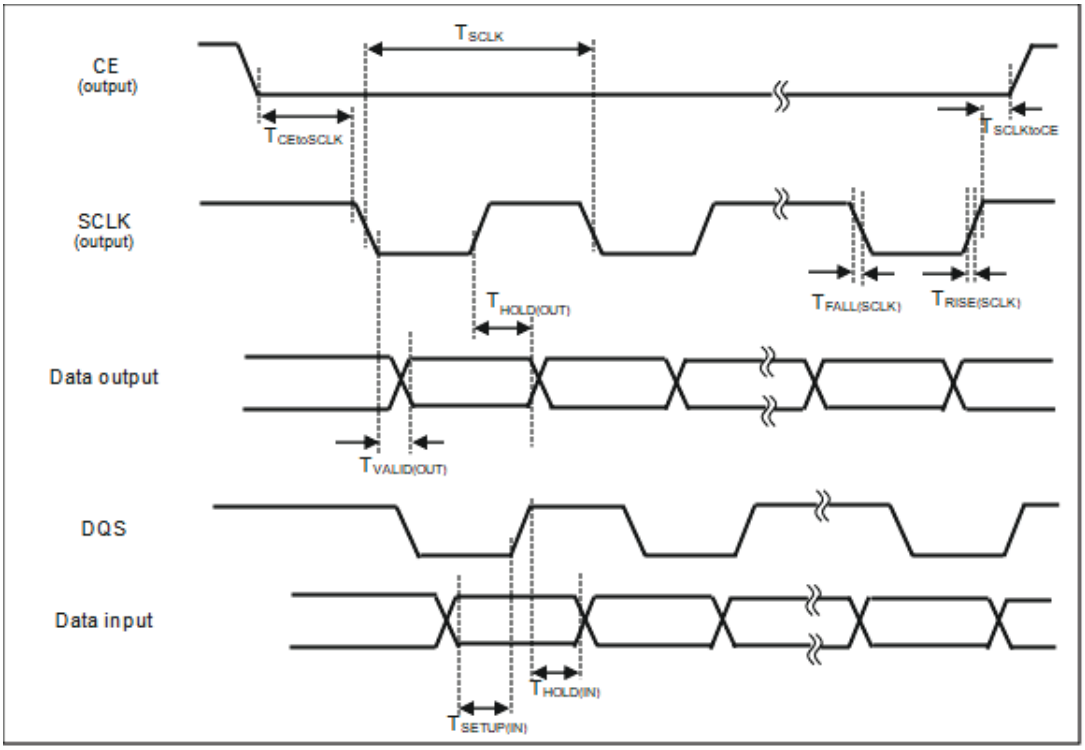


Figure 69. MSPI1 DDR with DQS Mode Timing Diagram

30.13 I²C/SPI Manager (IOM)

30.13.1 Inter-Integrated Circuit (I²C) Interface

Table 61: I²C Interface Timing

Symbol	Parameter	VCC	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	1.71 V - 2.2 V	10	-	1000	kHz
t_{LOW}	Low period of SCL clock	1.71 V - 2.2 V	1.3	-	-	µs
t_{HIGH}	High period of SCL clock	1.71 V - 2.2 V	600	-	-	ns
t_{RISE}	Rise time of SDA and SCL	1.71 V - 2.2 V	-	-	300	ns
t_{FALL}	Fall time of SDA and SCL	1.71 V - 2.2 V	-	-	300	ns
$t_{HD:STA}$	START condition hold time	1.71 V - 2.2 V	600	-	-	ns
$t_{SU:STA}$	START condition setup time	1.71 V - 2.2 V	600	-	-	ns
$t_{SU:DAT}$	SDA setup time	1.71 V - 2.2 V	100	-	-	ns
$t_{HD:DAT}$	SDA hold time	1.71 V - 2.2 V	0	-	-	ns
$t_{SU:STO}$	STOP condition setup time	1.71 V - 2.2 V	600	-	-	ns
t_{BUF}	Bus free time before a new transmission	1.71 V - 2.2 V	1.3	-	-	µs

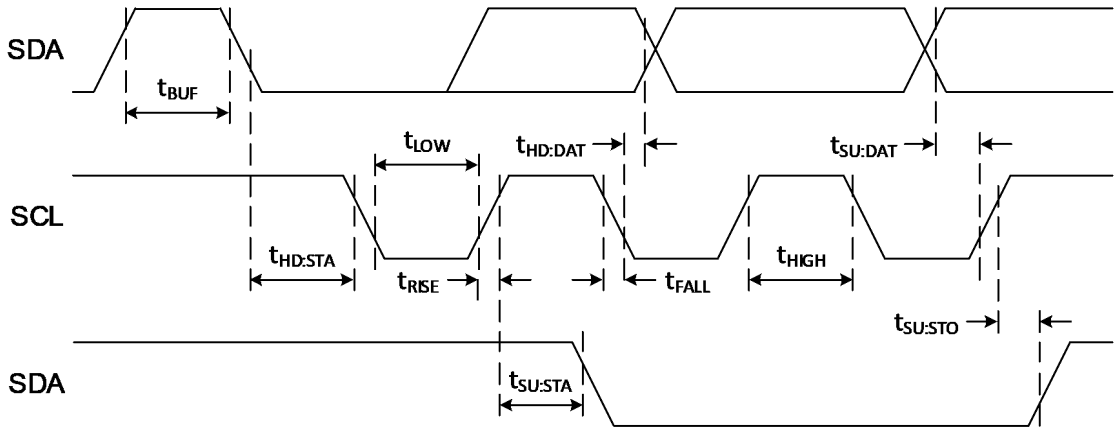


Figure 70. I²C Interface Timing Diagram

30.13.2 Serial Peripheral Interface (SPI) Manager Interface

Timing characteristics have been determined by measurements on chip.

Table 62: SPI Manager Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} ($1/T_{SCLK}$)	SCLK frequency range	DS=0.5x, 30pF load	-	-	48	MHz
$F_{SCLK-3WIRE}$	SCLK frequency range - 3-wire mode	DS=0.5x, 30pF load	-	-	12	MHz
$T_{LOW(SCLK)}$	Clock low time	DS=0.5x, 30pF load	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time	DS=0.5x, 30pF load	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	DS=0.5x, 30pF load	-	1.5	-	ns
$T_{FALL(SCLK)}$	Clock fall time	DS=0.5x, 30pF load	-	2.8	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	DS=0.5x, 30pF load	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	DS=0.5x, 30pF load	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SETUP (MISO)}$	MISO input data setup time	DS=0.5x, 30pF load	5.5	-	-	ns
$T_{HOLD (MISO)}$	MISO input data hold time	DS=0.5x, 30pF load	2	-	-	ns
$T_{SETUP\_3WIRE (MOSI\_IN)}$	MOSI input data setup time for 3-wire mode[1]	DS=0.5x, 30pF load	34	-	-	ns
$T_{HOLD\_3WIRE (MOSI\_IN)}$	MOSI input data hold time for 3-wire mode	DS=0.5x, 30pF load	2	-	-	ns
$T_{VALID\_HOLD (MOSI)}$	MOSI output data hold time	DS=0.5x, 30pF load	0	-	-	ns
$T_{VALID (MOSI)}$	MOSI output data valid time	DS=0.5x, 30pF load		-	6	ns
$T_{VALID\_HOLD\_3WIRE (MOSI)}$	MOSI output data hold time for 3-wire mode	DS=0.5x, 30pF load	-4	-	-	ns
$T_{VALID\_3WIRE (MOSI)}$	MOSI output data valid time for 3-wire mode	DS=0.5x, 30pF load	-	-	32	ns

1. For 3-wire mode, MOSI is a bidirectional pin. All 3-wire mode times are from simulation data.

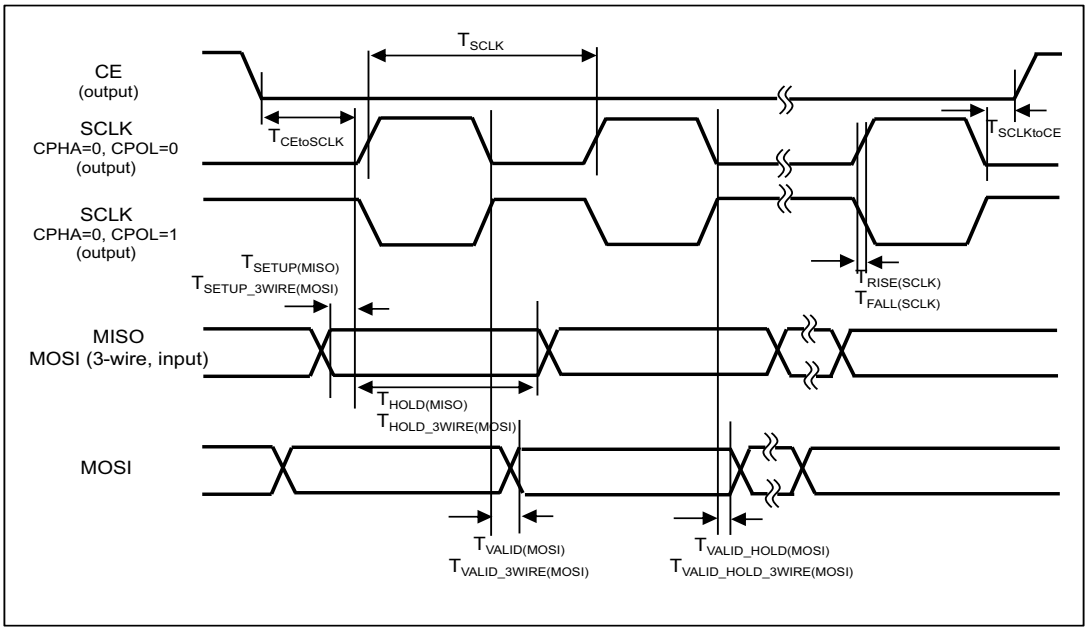


Figure 71. SPI Manager Interface Timing Diagram, CPHA = 0

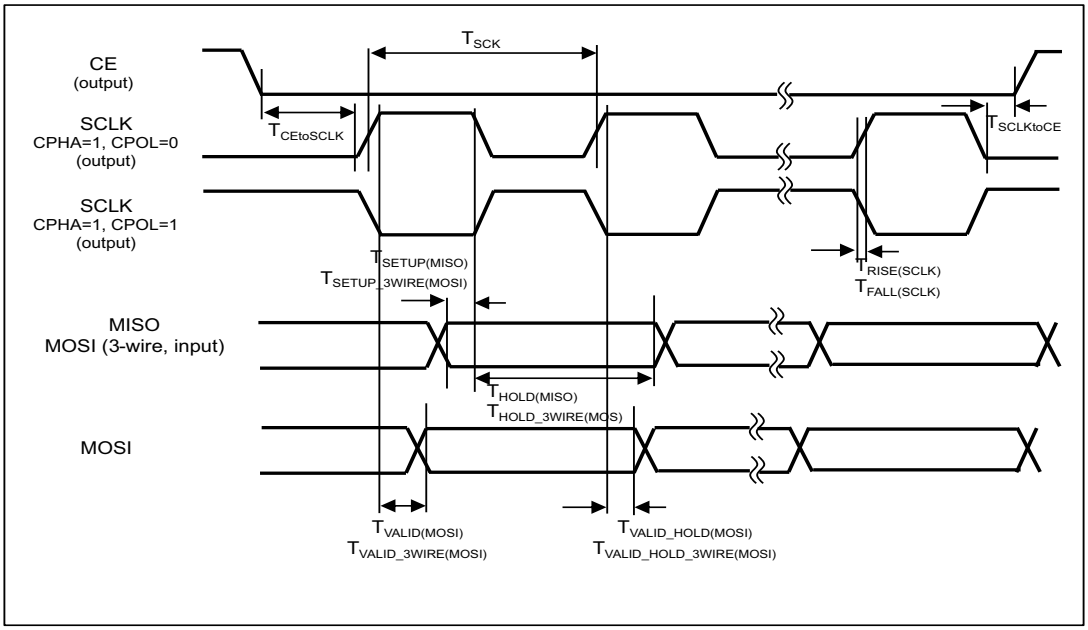


Figure 72. SPI Manager Interface Timing Diagram, CPHA = 1

30.14 SPI Subordinate (IOSFD)

30.14.1 Serial Peripheral Interface (SPI) Subordinate Interface (IOSFD)

Timing characteristics have been determined by measurements on chip except for 3-wire mode timings which have been derived through simulation.

Table 63: SPI Subordinate Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} ($1/T_{SCLK}$)	SCLK frequency range		-	8	24[1]	MHz
$F_{SCLK-3WIRE}$	SCLK frequency range - 3-wire mode		-	8	12	MHz
$T_{LOW(SCLK)}$	Clock low time		$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time		$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time		-	2	-	ns
$T_{FALL(SCLK)}$	Clock fall time		-	2	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge		18	-	-	ns
$T_{SCLKtoCE}$	Last SCLK to CE		18	-	-	ns
$T_{SETUP(MOSI)}$	MOSI input data setup time		3.9	-	-	ns
$T_{HOLD(MOSI)}$	MOSI input data hold time		3	-	-	ns
$T_{SETUP\_3WIRE(MOSI\_IN)}$[2]	MOSI input data setup time for 3-wire mode[3]		35	-	-	ns
$T_{HOLD\_3WIRE(MOSI\_IN)}$	MOSI input data hold time for 3-wire mode		3	-	-	ns
$T_{VALID\_HOLD(MISO)}$	MISO output data hold time	DS=0.5x, 15 pF Load	4	-	-	ns
$T_{VALID(MISO)}$	MISO output data valid time	DS=0.5x, 15 pF Load	-	-	15.5	ns
$T_{VALID\_HOLD\_3WIRE(MOSI)}$	MOSI output data hold time for 3-wire mode	DS=0.5x, 15 pF Load	4	-	-	ns
$T_{VALID\_3WIRE(MOSI)}$	MOSI output data valid time for 3-wire mode	DS=0.5x, 15 pF Load	-	-	32	ns

1. Due to the specified $T_{VALID(MISO)}$ time, max clock is restricted to 24 MHz. If the external SPI host supports full-cycle data capture, max clock is 48 MHz.
2. TSETUP_3WIRE(MOSI_IN), THOLD_3WIRE(MOSI_IN), TVALID_HOLD_3WIRE(MOSI), and TVALID_3WIRE(MOSI) specifications are from simulation data.
3. For 3-wire mode, MOSI is a bidirectional pin.

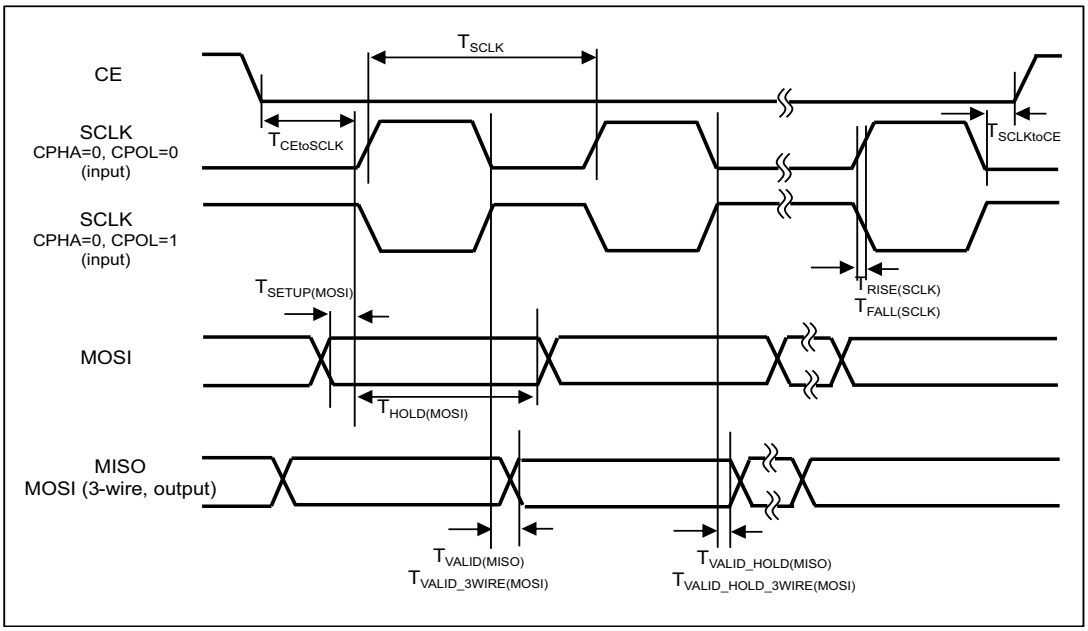


Figure 73. SPI Subordinate Interface Timing Diagram, CPHA = 0

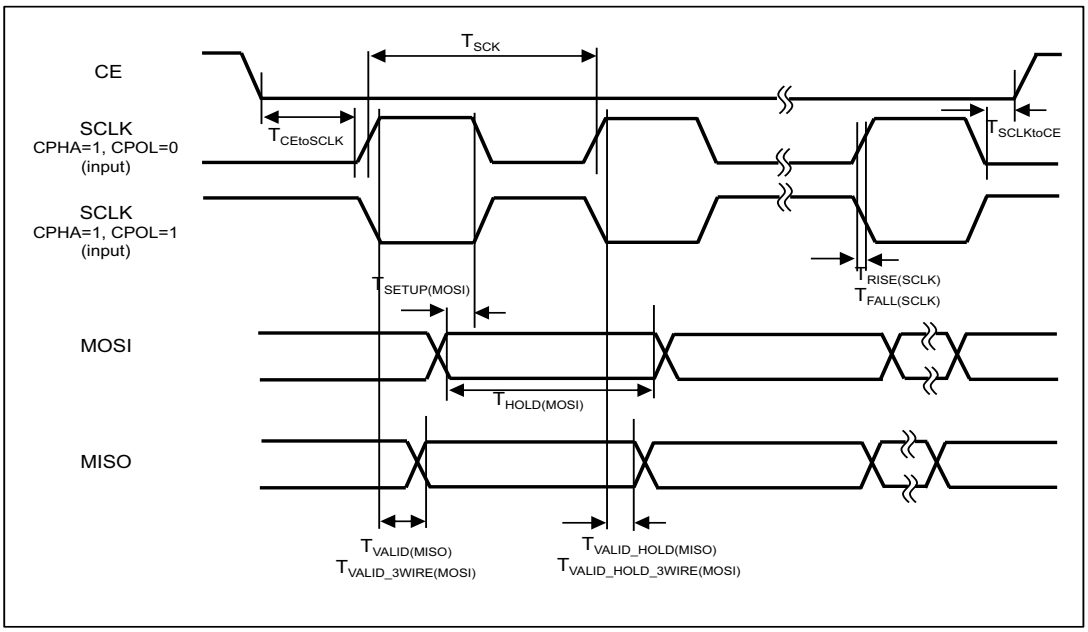


Figure 74. SPI Subordinate Interface Timing Diagram, CPHA = 1

30.15 Universal Asynchronous Receiver/Transmitter (UART)

Table 64: Universal Asynchronous Receiver/Transmitter (UART)

Symbol	Parameter	Min	Typ	Max	Unit
F_{BAUD}	UART baud rate	-	-	3.0	Mbps

30.16 Universal Serial Bus (USB)

30.16.1 USB Power Gating and Leakage Current

Table 65: USB Power Gating

VDDF_USB_SW	VDDUSB0P9	VDDUSB33	Requirements
OFF	ON	ON	This state may result in elevated leakage current (see USB Leakage Current table below) and is not recommended in a system where the 0.9 V rail is powered from the battery and not USB VBUS.
ON	OFF	ON	VDDUSB0P9 must be pulled to ground. A floating supply will cause leakage from VDDF_USB_SW.
ON	OFF	OFF	VDDUSB0P9 / VDDUSB33 must be pulled to ground. A floating supply will cause leakage from VDDF_USB_SW.
OFF	OFF	ON	VDDUSB0P9 must be pulled to ground. A floating supply will cause leakage from VDDUSB33.

NOTES:
1) The VDDF_USB_SW rail is internal, and the VDDUSB33 and VDDUSB0P9 rails are external on the Apollo510B SoC. External rails are controlled by the user's design/system on request by the MCU software (either via GPIO or I2C or even over inter-CPU communications bet ween the MCU and the main processor), while the internal rails are controlled through register settings.
2) Removal of VDDUSB33 while VDDUSB0P9 is still powered on is not supported as it will affect long term reliability of the PHY.

Table 66: USB Leakage Current

Operating Conditions	VDDF_USB_SW (0.8 V nominal)	VDDUSB0P9 (0.9 V nominal)	VDDUSB33 (3.3 V nominal)	Worst case leakage @ VDDF_USB_SW	Worst case leakage @ VDDUSB0P9	Worst case leakage @ VDDUSB33
USB comes out of reset; PHY is in suspend mode	0.8 V	0.9 V	3.3 V	0	4 µA	40 µA
PHY is not operational; All input signals are at their default values.	0.8 V	0	3.3 V	0	0	40 µA
PHY is not operational; All input signals are at their default values.	0	0	3.3 V	0	0	1.2 µA
PHY is not operational; All input signals are at their default values.	0	0.9 V	3.3 V	0	X	X

NOTES:
1) All numbers given are with the assumption PHY is brought to suspend state, and the USB controller is held in reset before any rails are powered off.
2) Both DP/DM are in the high-Z state if the PHY is powered off when in suspend or reset state. Otherwise, the DP/DM state depends on the state USB controller/SW is in at the moment when PHY power goes off.
3) Leakage via external ESD protection brings DP/DM voltage to zero when PHY puts them in the high-Z state.
4) If 3.3 V is always powered, the software must enable internal 0.8 V rail before the internal 0.9V. Otherwise, leakage can't be controlled (last two rows of the table).
5) "X" indicates that the leakage current is unpredictable and could be > 40 mA.
6) Assuming 3.3 V is always on, the power-on sequence depicted below is allowed with no limitations on the duration [t0...t1]. The leakage for the period from t0 to t1 is several microamps.

30.16.2 USB PHY Power and Interface Timing Requirements

Table 67: USB PHY Power Supply

Voltage Supply	Parameter	Condition	Min	Typ	Max	Units
VDDUSB33	Voltage		3.0	-	3.63	V
VDDUSB33	Current consumption	In functional FS/HS state	-	6.2	-	mA
VDDUSB0P9	Voltage		0.84	-	0.99	V
VDDUSB0P9	Ripple		-	-	5	%
VDDUSB0P9	Current consumption	In functional FS/HS state	-	23.2	40	mA
VDDUSB33	Current Consumption	In suspend state when both 3.3 V and 0.9 V are supplied.	-	-	4	µA
VDDUSB0P9	Current Consumption		-	-	5	µA

30.17 Secure Digital Input Output (SDIO)

Table 68: SDIO General Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{TX\_DLY\_STEP\_SIZE}$	TX Delay Step Size		0.12	-	0.40	ns
$T_{RX\_DLY\_STEP\_SIZE}$	RX Delay Step Size		0.09	-	0.35	ns

30.17.1 Default SD Interface

Timing characteristics have been determined through simulations.

1. Timing parameters are based on a nominal voltage of 3.3 V.
2. Data, CMD output hold time is based on FF/H/H/H/-40C corner.
3. The timing parameters are based on 0-tap TX and RX delay lines, with SDIO_HOSTCTRL1_HISPEEDEN bit = 0.
4. Default Speed Card specifications:

   Input setup/hold = 5 ns / 5 ns, with respect to clock rise

   Output min/max = 0 ns / 14 ns, with respect to clock fall
5. High Speed Card specifications with respect to clock rise:

   Input setup/hold = 6 ns / 2 ns

   Output min/max = 2.5 ns / 14 ns

Table 69: Default and High-Speed SD Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{CLK} ($1/T_{CLK}$)	SCLK frequency range		-	-	48	MHz
T_{CLK_LO}	Clock low time		$0.45/F_{CLK}$	-	$0.55/F_{CLK}$	s
T_{CLK_HI}	Clock high time		$0.45/F_{CLK}$	-	$0.55/F_{CLK}$	s
$T_{RISE(CLK)}$	Clock rise time	10 pF load	-	-	2	ns
$T_{FALL(CLK)}$	Clock fall time	10 pF load	-	-	1	ns
$T_{SETUP(IN)}$	Data/CMD input setup time		2.0	-	-	ns
$T_{HOLD(IN)}$	Data/CMD input hold time		1.5	-	-	ns
$T_{HOLD(OUT)}$	Data/CMD output hold time	10 pF load	-1	-	-	ns
$T_{VALID(OUT)}$	Data/CMD output valid time	10 pF load	-	-	3.2	ns

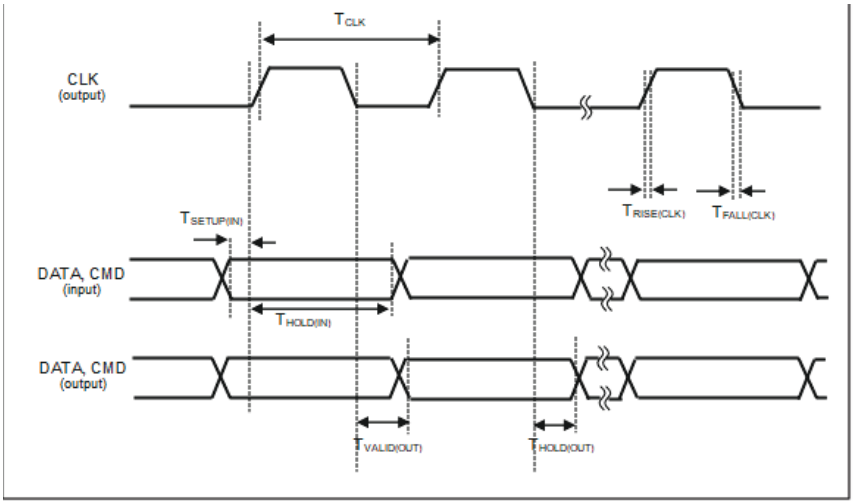


Figure 75. Default and High-Speed SD Interface Timing Diagram

30.17.2 SD SDR50 Mode Interface

Timing characteristics have been determined by measurements on chip.

The following specifications are with the settings MCUCTRL_SDIOnCTRL_SDIOnOTAPDLYSEL = 4 and MCUCTRL_SDIOnCTRL_SDIOnITAPDLYSEL = 8.

Table 70: SD SDR50 Mode Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{CLK} ($1/T_{CLK}$)	SCLK frequency range		-	-	96	MHz
T_{CLK_LO}	Clock low time	15 pF Load, DS=1.0x	$0.3/F_{CLK}$	-	$0.6/F_{CLK}$	s
T_{CLK_HI}	Clock high time	15 pF Load, DS=1.0x	$0.4/F_{CLK}$	-	$0.7/F_{CLK}$	s
$T_{RISE(CLK)}$	Clock rise time	15 pF Load, DS=1.0x	-	2.2	-	ns
$T_{FALL(CLK)}$	Clock fall time	15 pF Load, DS=1.0x	-	3.5	-	ns
$T_{SETUP(IN)}$	Data/CMD input setup time	15 pF Load, DS=1.0x	2	-	-	ns
$T_{HOLD(IN)}$	Data/CMD input hold time	15 pF Load, DS=1.0x	2	-	-	ns
$T_{HOLD(OUT)}$	Data/CMD output hold time	15 pF Load, DS=1.0x	2	-	-	ns
$T_{VALID(OUT)}$	Data/CMD output valid time	15 pF Load, DS=1.0x	-	-	7	ns

Note: Card specifications with respect to clock rise:

- Input setup/hold = 3 ns/0.8 ns
- Output min/max = 1.5 ns/7.5 ns

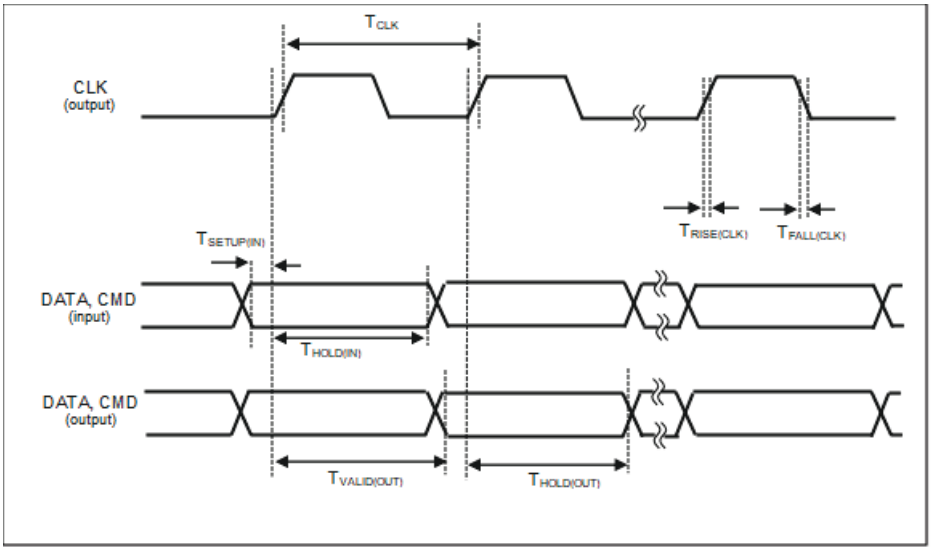


Figure 76. SD SDR50 Mode Interface Timing Diagram

30.17.3 SD DDR50 Mode Interface

Timing characteristics have been determined by measurements on chip.

The following specifications are with the settings MCUCTRL_SDIOnCTRL_SDIOnOTAPDLYSEL = 4 and MCUCTRL_SDIOnCTRL_SDIOnITAPDLYSEL = 8.

Table 71: SD DDR50 Mode Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{CLK} ($1/T_{CLK}$)	SCLK frequency range		-	-	48	MHz
T_{CLK_LO}	Clock low time	30 pF Load, DS=1.0x	$0.4/F_{CLK}$	-	$0.6/F_{CLK}$	s
T_{CLK_HI}	Clock high time	30 pF Load, DS=1.0x	$0.4/F_{CLK}$	-	$0.6/F_{CLK}$	s
$T_{RISE(CLK)}$	Clock rise time	30 pF Load, DS=1.0x	-	2.2	-	ns
$T_{FALL(CLK)}$	Clock fall time	30 pF Load, DS=1.0x	-	3.4	-	ns
$T_{SETUP(IN)}$	Data/CMD input setup time	30 pF Load, DS=1.0x	2	-	-	ns
$T_{HOLD(IN)}$	Data/CMD input hold time	30 pF Load, DS=1.0x	2	-	-	ns
$T_{HOLD(OUT)}$	Data/CMD output hold time	30 pF Load, DS=1.0x	1	-	-	ns
$T_{VALID(OUT)}$	Data/CMD output valid time	30 pF Load, DS=1.0x	-	-	6	ns

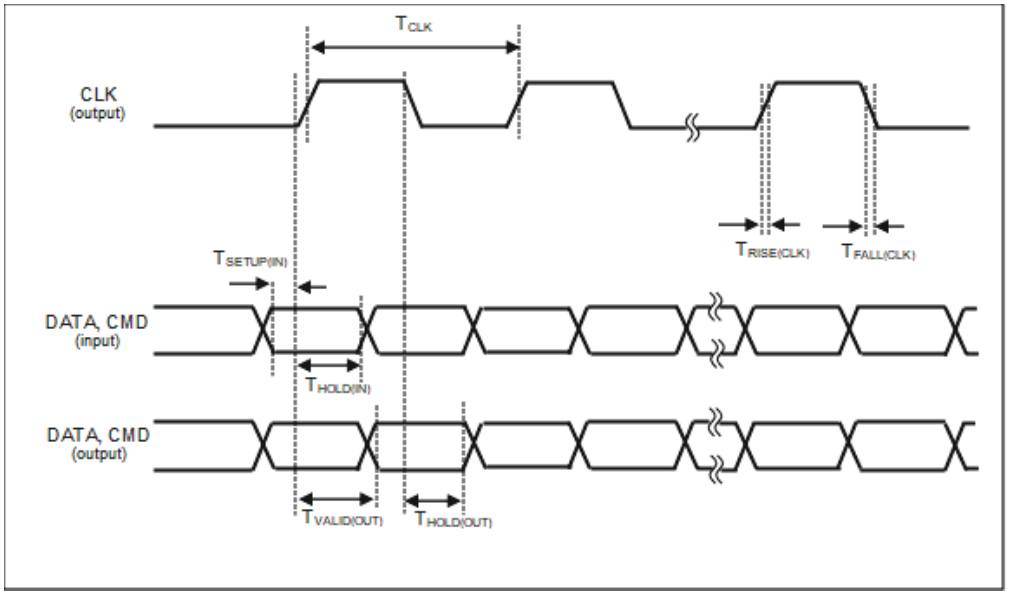


Figure 77. SD DDR50 Mode Interface Timing Diagram

30.18 Audio

30.18.1 I²S Interface

Timing characteristics have been determined by measurements on chip.

Table 72: I²S Subordinate Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} (1/TSCLK)	SCLK frequency range		-	-	12	MHz
$T_{LOW(SCLK)}$	Clock low time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	DS = 1.0x, 30 pF load	-	1.4	-	ns
$T_{FALL(SCLK)}$	Clock fall time	DS = 1.0x, 30 pF load	-	1.6	-	ns
$T_{SETUP(WSIN)}$	WS input data setup time		8	-	-	ns
$T_{HOLD(WSIN)}$	WS input data hold time		9	-	-	ns
$T_{SETUP(SDIN)}$	SDIN input data setup time		8	-	-	ns
$T_{HOLD(SDIN)}$	SDIN input data hold time		9	-	-	ns
$T_{HOLD(SDOUT)}$	SDOUT output data hold time	DS = 1.0x, 30 pF load	0	-	-	ns
$T_{VALID(SDOUT)}$	SDOUT output data valid time	DS = 1.0x, 30 pF load	-	-	25	ns

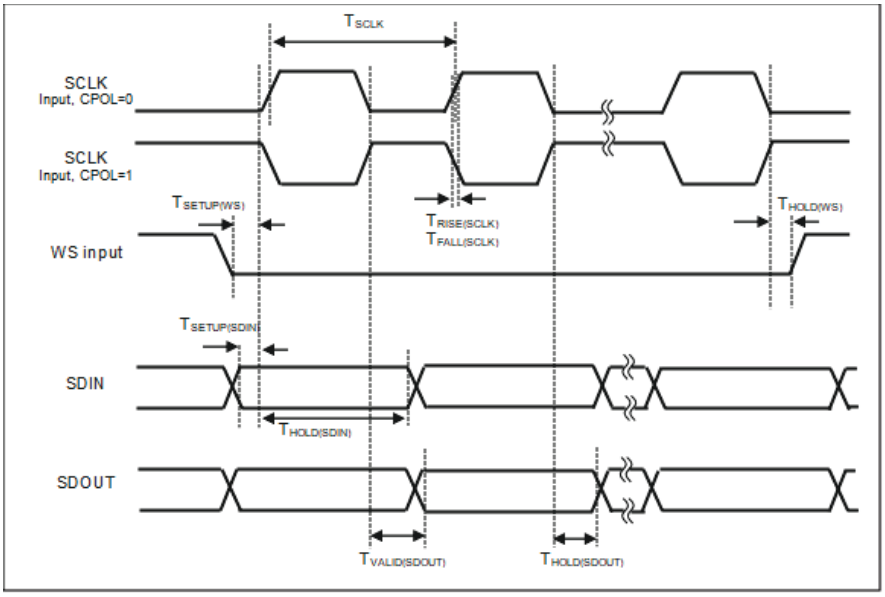


Figure 78. I²S Subordinate Interface Timing Diagram

Timing characteristics have been determined by measurements on chip.

Table 73: I²S Manager Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} (1/TSCLK)	SCLK frequency range		-	-	12	MHz
$T_{LOW(SCLK)}$	Clock low time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	DS = 1.0x, 30 pF load	-	1.4	-	ns
$T_{FALL(SCLK)}$	Clock fall time	DS = 1.0x, 30 pF load	-	1.6	-	ns
$T_{HOLD(WSOUT)}$	WS output data hold time	DS = 1.0x, 30 pF load	0	-	-	ns
$T_{VALID(WSOUT)}$	WS output data valid time	DS = 1.0x, 30 pF load	-	-	25	ns
$T_{SETUP(SDIN)}$	SDIN input data setup time		8	-	-	ns
$T_{HOLD(SDIN)}$	SDIN input data hold time		9	-	-	ns
$T_{HOLD(SDOUT)}$	SDOUT output data hold time	DS = 1.0x, 30 pF load	0	-	-	ns
$T_{VALID(SDOUT)}$	SDOUT output data valid time	DS = 1.0x, 30 pF load	-	-	25	ns

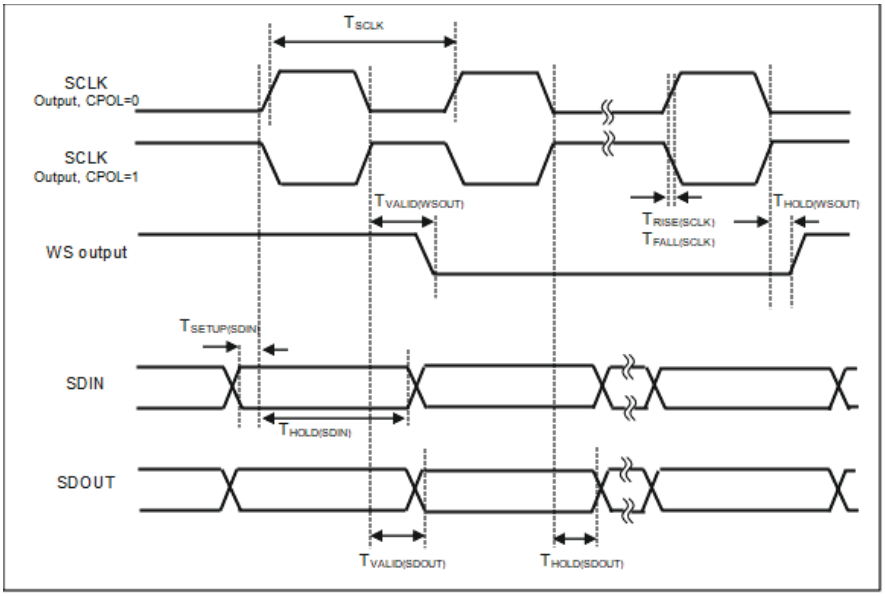


Figure 79. I²S Manager Interface Timing Diagram

30.18.2 PDM Interface

Timing characteristics have been determined by measurements on chip.

Table 74: PDM Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{PDM_CLK} ($1/T_{PDM\_CLK}$)	PDM_CLK frequency range	48 MHz HS XTAL	-	-	12	MHz
$T_{LOW(PDM\_CLK)}$	Clock low time	DS = 0.1x, 15pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{HIGH(PDM\_CLK)}$	Clock high time	DS = 0.1x, 15pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{RISE(PDM\_CLK)}$	Clock rise time	DS = 0.1x, 15pF load	-	2.5	-	ns
$T_{FALL(PDM\_CLK)}$	Clock fall time	DS = 0.1x, 15pF load	-	3	-	ns
$T_{SETUP(PDM\_DAT)}$	PDM input data setup time		25	-	-	ns
$T_{HOLD(PDM\_DAT)}$	PDM input data hold time		0	-	-	ns

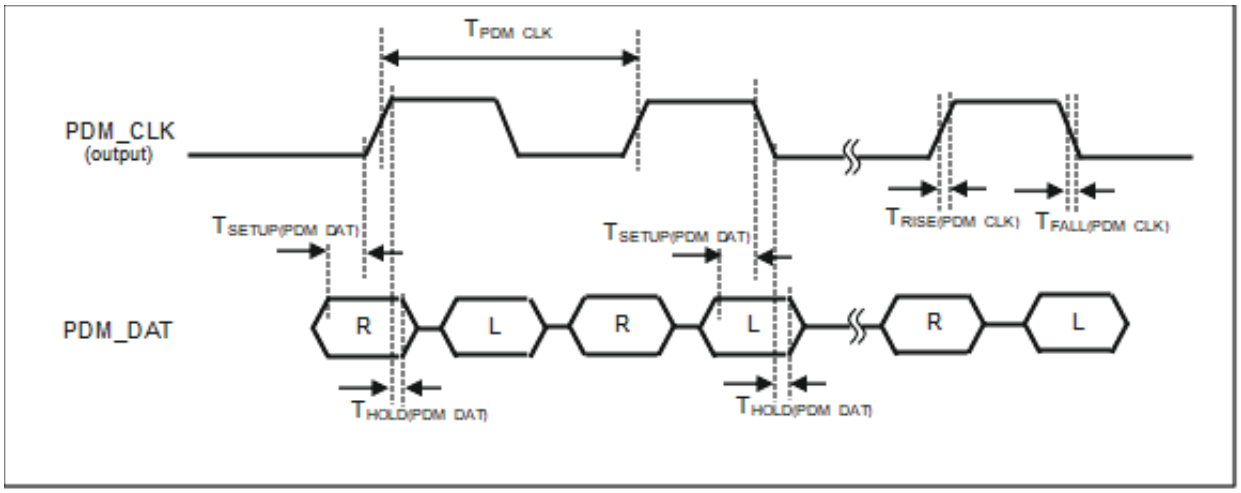


Figure 80. PDM Interface Timing Diagram

30.18.3 Audio Analog-to-Digital Converter (AUDADC)

Timing characteristics have been determined by measurements on chip.

30.18.4 AUDADC Audio Specifications

Table 75: AUDADC Audio Specifications

Symbol	Parameter	Test Condition	Weighting	Min	Typ	Max	Units
A_{AUDADC_PGA}	PGA Gain	Minimum	-	-	-6	-	dB
		Maximum	-	-	45	-	dB
		Step Size	-	-	0.5	-	dB
THD_{AUDADC}	Total Harmonic Distortion + Noise (THD+N) (DRE disabled) PGA Gain	PGA Gain = 0 dB, -1 dBFS	A-weighted	-	-60	-	dB
			Unweighted	-	-54	-	dB
		PGA Gain = 12 dB, -1 dBFS	A-weighted	-	-58	-	dB
			Unweighted	-	-53	-	dB
		PGA Gain = 24 dB, -1 dBFS	A-weighted	-	-53	-	dB
			Unweighted	-	-50	-	dB
FDI_DR_{AUDADC}	Dynamic Range (DR) Fully-differential input (DRE disabled)[1]	PGA Gain = 0 dB	A-weighted	-	-65	-	dB
			Unweighted	-	-63	-	dB
		PGA Gain = 12 dB	A-weighted	-	-63	-	dB
			Unweighted	-	-61	-	dB
		PGA Gain = 24 dB	A-weighted	-	-56	-	dB
			Unweighted	-	-55	-	dB
IC_ISOL_{AUDADC}	Interchannel Isolation	PGA Gain = 0 dB	1 kHz	-	>60	-	dB
		PGA Gain = 24 dB	1 kHz	-	>60	-	dB
$FDIV\_FS_{AUDADC}$	Full Scale Input Voltage (Fully Differential Input)	PGA Gain = -6 dB	-	-	600	-	mVrms
		PGA Gain = 0 dB	-	-	300	-	mVrms
		PGA Gain = 12 dB	-	-	75	-	mVrms
		PGA Gain = 24 dB	-	-	25	-	mVrms
		PGA Gain = 30 dB	-	-	12.5	-	mVrms
MOD_IDX_{AUDADC}	Modulation Index[2]	-	-	-	100	-	%FS
$V_{AUDADCIN}$	DC Voltage Range at Analog Input Pin	Pin floating	-	-	800	-	mV
$V_{AUDADCREF}$	DC Voltage Range at LPADC_REF	See Note[3]	-	-	1200	-	mV
$CMRR_{AUDADC}$	Common Mode Rejection Ratio (CMRR)[4]	100 mVpp on both inputs, Sample Rate = 48 kHz, PGA GAIN = 0 dB	1 Hz	-	>60	-	dB
$ATOT_{AUDADC}$	Audio Turn-on Time	With BGTLP always on and PGA VREFGEN quick charge	-	-	10	-	ms

1. Dynamic Range is measured by looking at the difference between the noise floor and full scale. The minimum signal must be slightly above the noise floor and the maximum signal is 0 dB.

2. Modulation index specifies the percentage of the digital full scale obtained when a full-scale analog input is driven on the PGA inputs for a given gain.
3. LPADC_REF pin may not be loaded due to low current drive (even with a typical voltmeter). For voltage measurements, a high impedance buffer was used before connecting to voltmeter.
4. CMRR is measured by shorting the inputs of the AC coupling capacitors together and to the sinusoidal waveform generator

30.18.5 AUDADC Mic Bias Specifications

In Table 67, the following condition applies unless otherwise indicated.

Table 76: AUDADC Mic Bias Specifications

Symbol	Parameter	Test Condition	Weighting	Min	Typ	Max	Units
V_{AUDADC_OVNL}	Output Voltage (no load)	VOLTAGETRIM = 5	-	-	920	-	mV
V_{AUDADC_OVNL}	Output Voltage (no load)	VOLTAGETRIM = 32	-	-	1280	-	mV
V_{AUDADC_OVNL}	Output Voltage (no load)	VOLTAGETRIM = 52	-	-	1494	-	mV
V_{AUDADC_OVBM}	Output Voltage (Bypass Mode)	VOLTAGETRIM = 63	-	-	>1500	-	mV

30.19 Serial Wire Debug (SWD)

Timing characteristics have been determined through simulations.

Table 77: SWD Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SWCLK} ($1/T_{SWCLK}$)	SWCLK frequency range		-	-	20	MHz
$T_{LOW(SWCLK)}$	SWCLK low time		$0.45/F_{SWCLK}$	-	$0.55/F_{SWCLK}$	s
$T_{HIGH(CLK)}$	SWCLK high time		$0.45/F_{SWCLK}$	-	$0.55/F_{SWCLK}$	s
$T_{RISE(SWCLK)}$	SWCLK rise time		-	-	2	ns
$T_{FALL(SWCLK)}$	SWCLK fall time		-	-	2	ns
$T_{SETUP(IN)}$	SWDIO input setup time		3	-	-	ns
$T_{HOLD(IN)}$	SWDIO input hold time		3	-	-	ns
$T_{HOLD(OUT)}$	SWDIO output hold time		1	-	-	ns
$T_{VALID(OUT)}$	SWDIO output valid time[1]		-	-	35	ns

1. The output valid time is larger than one SWCLK cycle period at max frequency. This means that during SWD read, the SWCLK frequency needs to be adjusted to meet the timing.

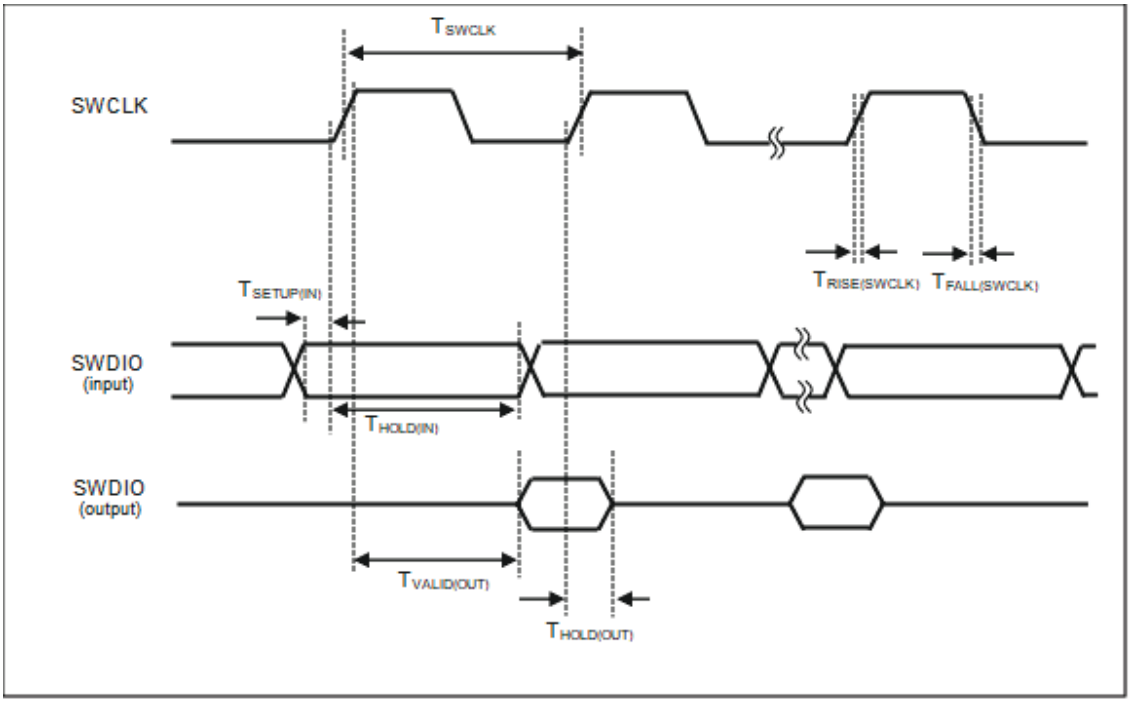


Figure 81. SWD Interface Timing Diagram

31. Ordering Information

Table 78: Ordering Information for Apollo510B SoC

Device Name	Commercial Temp Range (-20°C to 70°C)	Industrial Temp Range (-40°C to 85°C)	Package Type	GPIOs	NVM (MRAM)	SRAM	Connectivity	Package[1] Size (mm)
Apollo510B SoC	AP510BFA-CBR	-	BGA	96	4 MB	3.75 MB	Bluetooth Low Energy	5.6 x 5.6 x 0.8(max) 153-pin WFBGA

1. Packing: Tape and Reel

32. Document Revision History

Table 79: Document Revision List - Apollo510B SoC

Revision	Date	Description
0.3.0	Aug 2024	Initial NDA release
0.9.0	Sep 2025	Initial RTM release
1.0.0	December 2025	CLKGEN: - CLKGEN Block diagram updated and associated note added. UART: - Note about 3 Mbps baud rate updated. Electricals: - In “Components for the BLE Controller” section, added “Required Specifications for L_{DCDC} Alternative Sources” table. - Performance and/or timing specifications updated for BLE Controller, GPIO, Display Controller, PDM, I2S, ADC, AUDADC, SDIO, MSPI, IOM, IOS, SWD. - Universal Asynchronous Receiver/Transmitter (UART) section added.

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