QUICK START GUIDE

Apollo510 EVB

(EVB Revision 2.2)

Ultra-low Power Apollo SoC Family

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Table of Content

List of Figures

List of Tables

1. Introduction

This document provides guidance for setting up the Apollo510 Evaluation Board (EVB), revision 2.2, part number AP510EVB, to get started executing code examples, measuring power consumption in various configurations, and beginning software development.

2. Document Revision History

Rev #	Date	Description
1.0	Jan 2025	Document initial public release
2.0	May 2025	Updated for EVB Revision 2.2

Table 1: Document Revision History

3. Reference Documents and Software

The latest version of the following items, which can be acquired through your Ambiq Sales contact, may be useful in understanding and using the EVB.

- EVB Schematic
- Apollo510 Datasheet
- Apollo510 Errata List
- AmbiqSuite SDK

4. Quick Start

The EVB Kit comes with the following items:

- Apollo510 Evaluation Board (EVB), revision 2.2
- USB Type C cable
- Four adhesive-backed rubber feet
- Extra jumpers

Caution: The EVB has components loaded on the back of the board. Care should be taken to not damage these components. The included rubber feet should be applied to the bottom of the board to prevent direct contact between the components and a desk surface.

The EVB comes with jumpers pre-configured for default operation. To start EVB program execution, connect the USB-C cable from a USB port on a PC to the J-Link USB connector (J16) on the EVB, and turn on the power switch (SW4). The green LED next to the power switch should illuminate.

The AmbiqSuite SDK provides many example programs that may be run on the EVB. To run these examples, download the SDK via the link provided above and select any of the pre-built examples in the SDK at /boards/apollo510_evb/examples. The examples should be programmed at address 0x410000. Updates to support the Apollo510 for IAR and Keil are available in the /debugger_updates/ folder of the SDK.

5. Overview of the Apollo510 EVB

The Apollo510 EVB has the following features:

- Apollo510 Arm® Cortex®-M55 based SoC in the BGA package (AP510NFA-CBR)
- USB Type C connector for power/download/debug (J16)
- USB Type C connector for power/data to Apollo510 (J18)
- On-board Segger J-Link debugger
- Debug-in port (J2) (SWD or ETM)
- Three user-controlled LEDs
- Two push buttons for application use, plus a reset push button
- Power slide switch with LED power indicator
- On-board interfaces:
  - MSPI x16 (Hex) PSRAM (AP Memory APS512XXN-AOB4BI-WBRZ)
  - MSPI x8 Octal Flash memory (ISSI IS25WX064-JHL)
  - SDIO 8 GB eMMC (ISSI IS21EF08G-JCLI)
  - High-speed expansion connector
  - MikroBUS socket interface
- General purpose male headers (J8 and J9) for I/O and power access to a shield board
- Test points for power measurements
- Solder bridge options for power supply flexibility and peripheral access options
- RoHS compliant

CAUTION: The EVB has components loaded on the back of the board. Care should be taken to not damage these components.

The following figures show the board layout, its major components and the location of all components.

Figure 1. EVB Top View

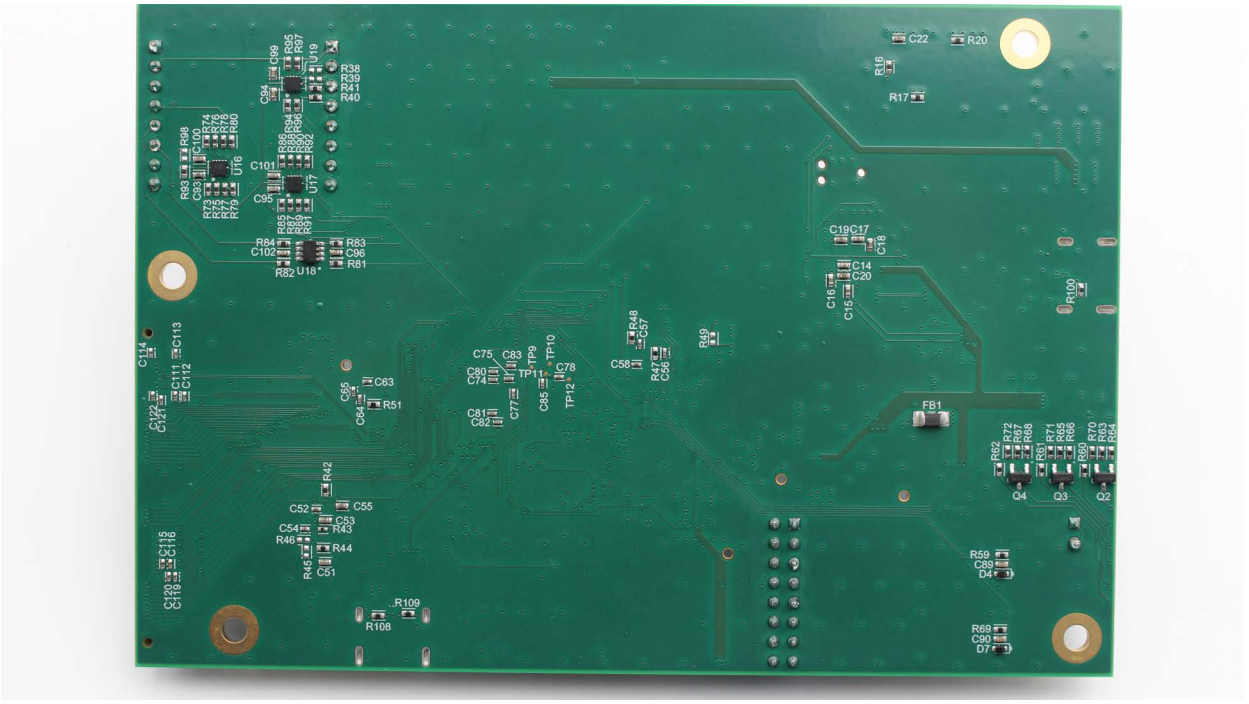
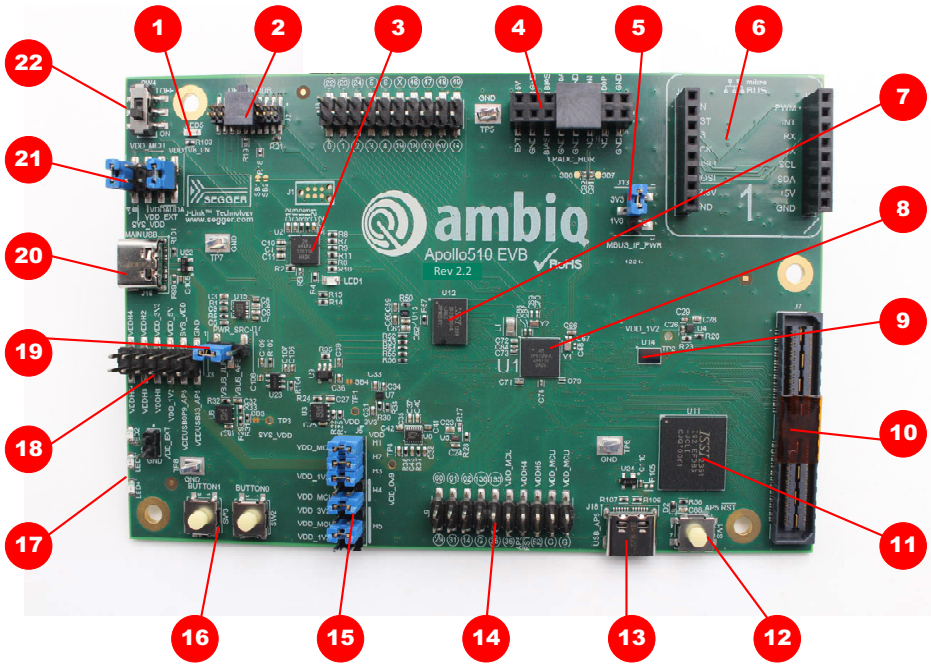


Figure 2. EVB Bottom View



1. Power LED
2. Debug in Connector
3. JLINK Controller
4. Voice-on-SPOT (VOS) Connector
5. MikroBUS I/F Voltage Header
6. MikroBUS Conectors
7. MSPI1 - IS25WX064-JHL
8. Apollo510 BGA MCU
9. MSPI0 - APS512XXB-AOB5NI-WA
10. High Speed Connector
11. eMMC0 - IS21EF08G-JCLI
12. Reset Switch
13. Apollo5 USB Connector
14. Dual-Row Headers (2x)
15. VDDHx Source Selection Header
16. User Switches (2x)
17. User LEDs
18. Power Test Points Header
19. Power Source Header
20. JLINK USB Comm
21. Power Config Header
22. Power Switch

Figure 3. EVB Major Components

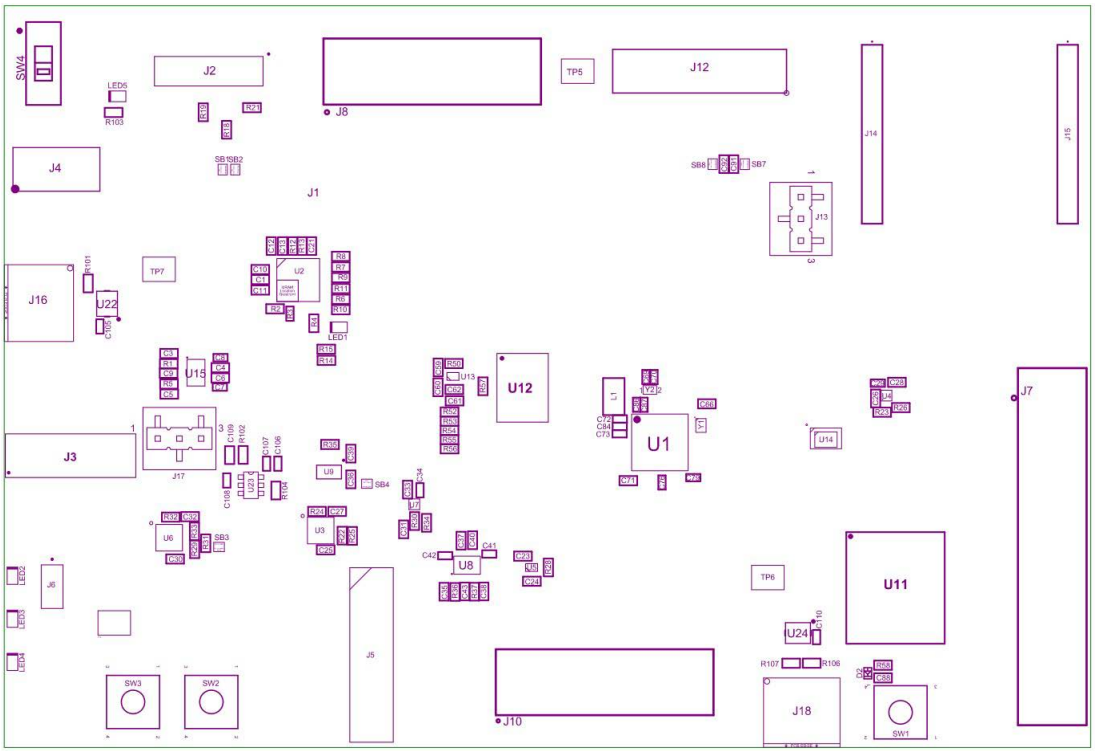


Figure 4. EVB Top Side Components

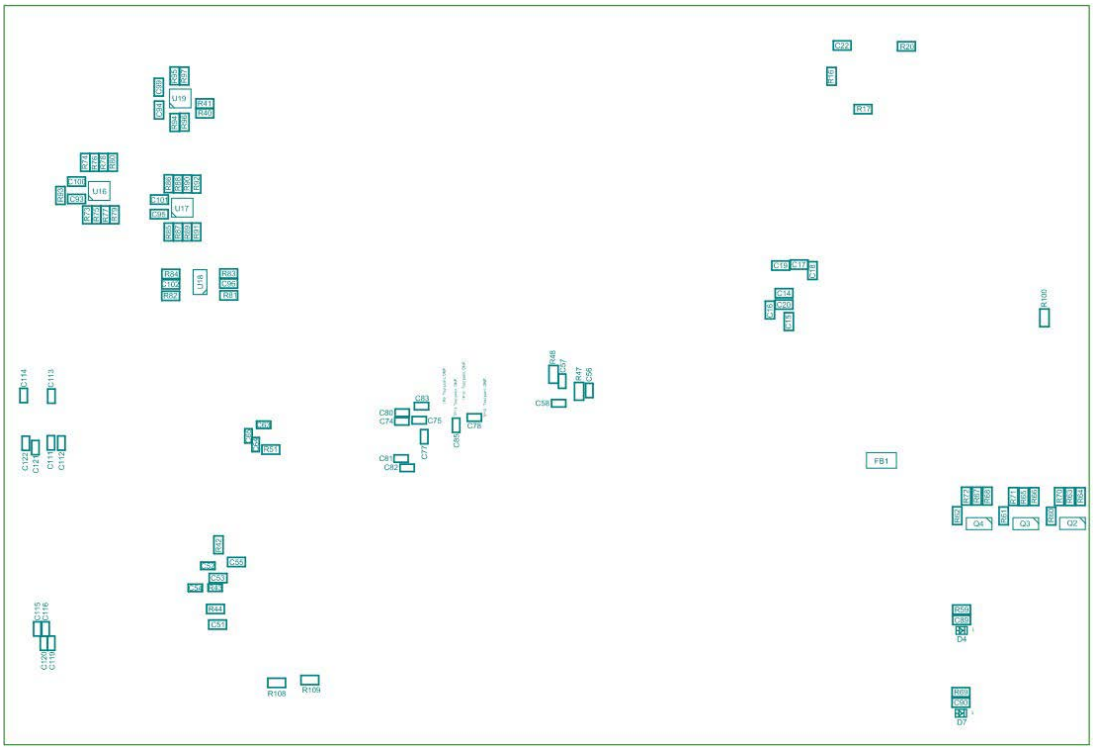


Figure 5. EVB Bottom Side Components

6. Secure Boot on the Apollo510 SoC

The on-board Apollo510 SoC is preprogrammed with a Secure Bootloader and an uninitialized Customer Info Space, referred to as INFO0. Initial provisioning of the part would include programming a valid INFO0 and programming the main firmware image in the flash. The Apollo510 EVB is shipped with the INFO0 configuration pre-programmed with optimal settings for the EVB layout which would include the following features/settings:

1. Default boot to non-secure mode
2. Enable Boot Override to Push Button on GPIO93 (OTP setting) - BTN0/SW2.
3. Enable wired updates over UART0
    A. UART0 is mapped to J-Link (OTP Setting).
    B. Baud rate is 115200 bps, no-parity, 8-bit data length, no flow control.
    C. Timeout is 5 seconds.

For reference, the following settings are programmed into INFO0 on the Apollo510 SoC resident on the EVB:

- Secure Bootloader (SBL) interface is configured to UART using GPIO30 and GPIO55, which allows secure boot to be performed over the J-Link COM interface of the EVB.
- SBL override pin is configured to GPIO93 which is Button 0 on the EVB.

For information on changing the INFO0 settings as well as using the Secure Bootloader, please refer to the README.txt file found in the tools\apollo5b_scripts folder of the latest SDK release supporting the Apollo5 family. This folder contains a number of python scripts to demonstrate generation of INFO0 settings, customer main images, and the creation of images for the Wired Update protocol over UART.

Please consult your Ambiq sales team for any additional documentation on INFO0 settings or Secure Bootloader.

7. Header Pin Assignments

This section provides an overview of the Apollo510 EVB connectivity and pin function options.

7.1 MikroBUS Headers

The Apollo510 EVB provides a MikroBUS header to enable rapid prototyping. The interface is accessed through headers J14 and J15 as shown in Figure 6. Function options for the GPIO on the header pins are as shown.

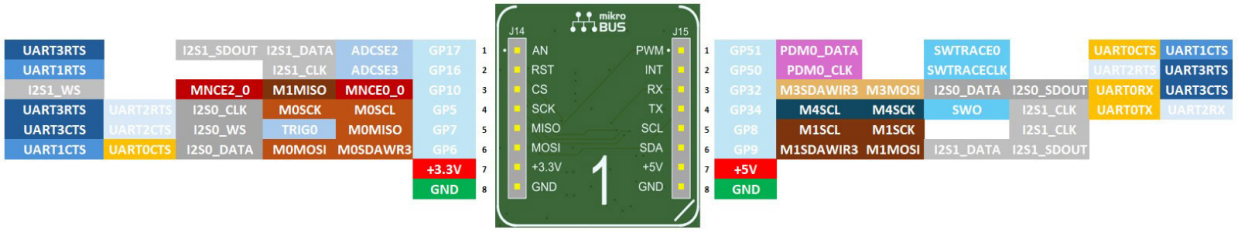


Figure 6. J14/J15 MikroBUS Headers - Function Options

7.2 General Purpose Headers

Function options for pins of general purpose headers J8 and J9 are as shown in Figure 7.

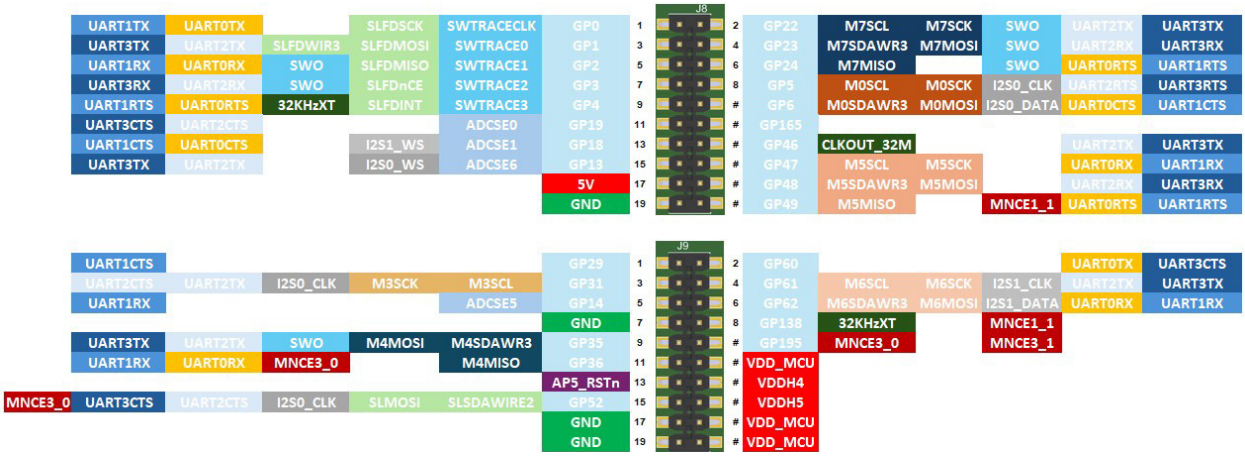


Figure 7. J8/J9 General Purpose Headers - Function Options

7.3 High-speed Header

Function options for pins of the high-speed header J7 are as shown in Figure 7.

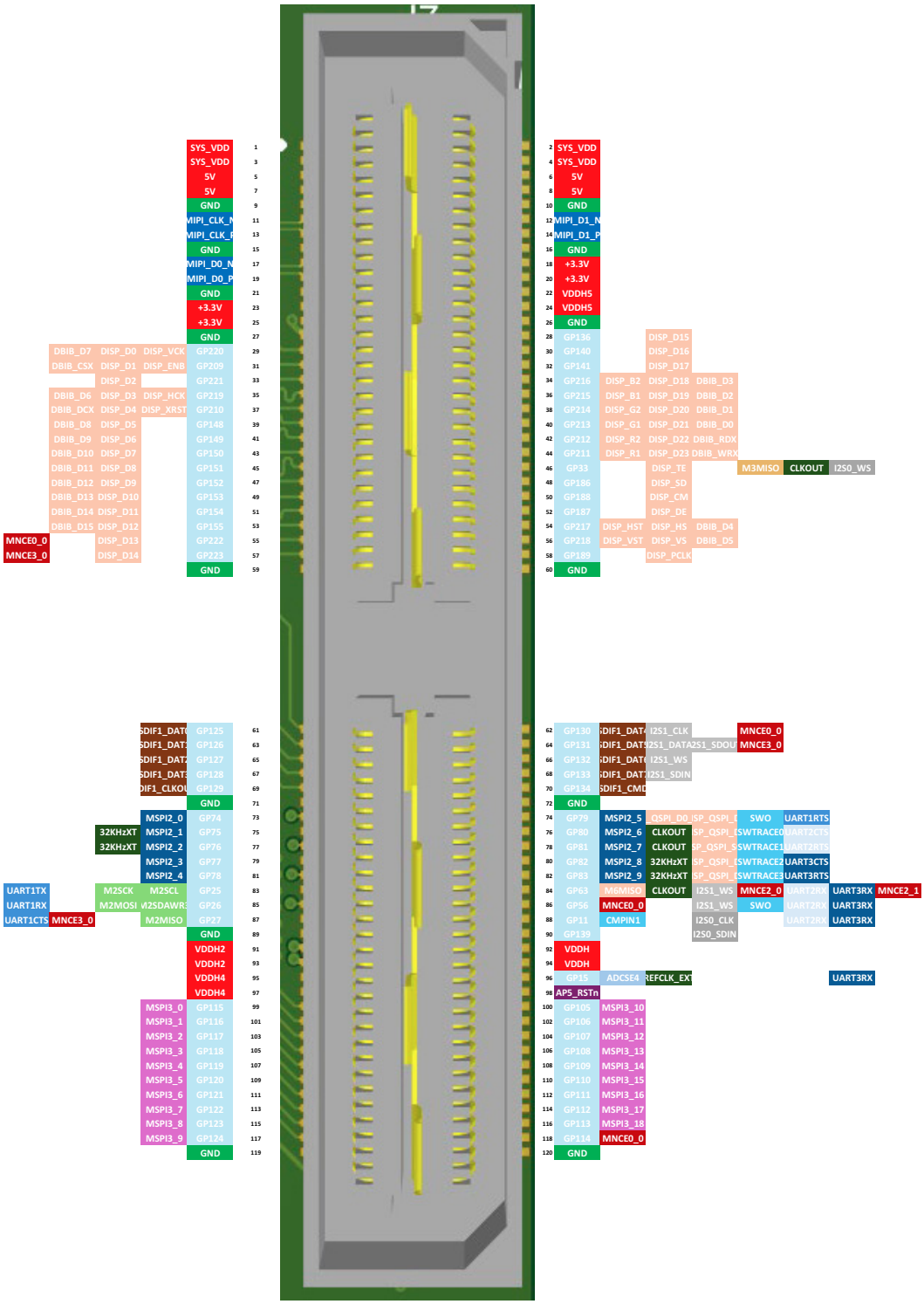


Figure 8. J7 High-speed Header - Function Options

Figure 8 shows board view of the J7 high-speed header which is located on the right edge of the EVB. The protective tape should be removed from the header before use.

Figure 9. Board View of J7 High-speed Header

8. Debug Interface

Figure 10 shows the Apollo510 EVB set up for standard debug using the on-board J-Link debugger and on-board power supply.

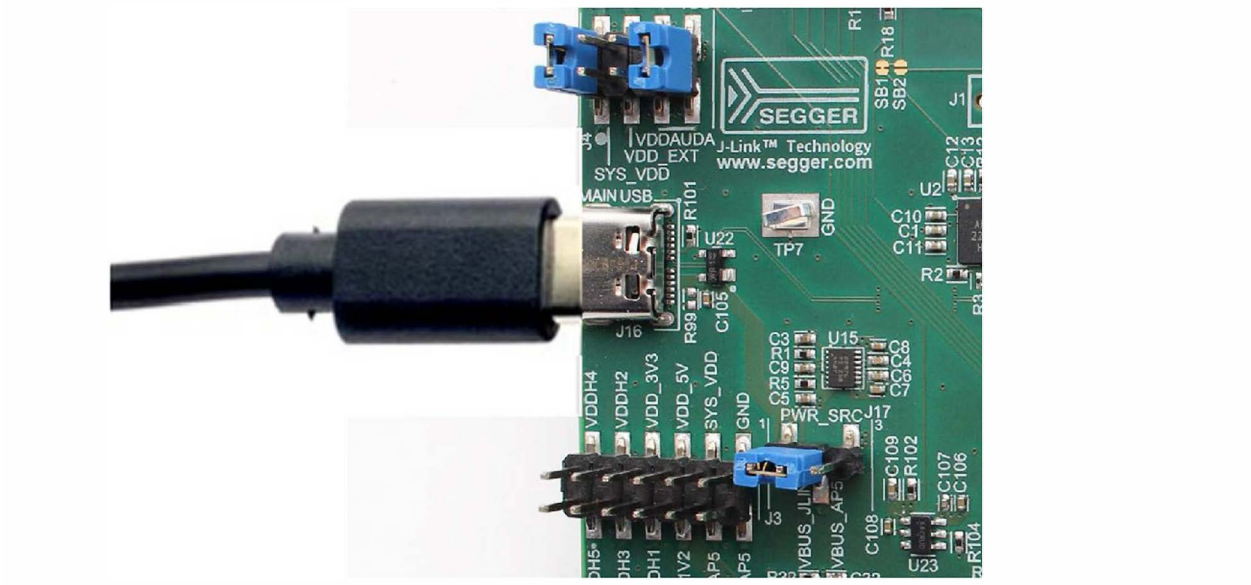


Figure 10. Using On-board J-Link Debugger

The debug interface is supported by standard J-Link drivers from Segger. Please refer to “Software Development Tools” on page 17 for more details on J-Link debug support.

8.1 Use of External Debugger

This EVB also supports the use of an external SWD debug interface through a 20-pin debug-in header (DEBUG HDR – J2) as shown in Figure 5-2. See the EVB schematic for connector pinout.

Figure 11. J2 Debug-In Header

No jumper changes are required to use an external debug adapter. Simply connect the external debug adapter with a ribbon cable connector to the “DEBUG HDR” header.

NOTE: Remove protective guard before attempting to connect to the debug header.

9. Software Development Tools

The standard Segger J-Link debug interface is used on the Apollo510 EVB. See the \Ambiq-Suite\debugger_updates\ folder in the AmbiqSuite SDK for interim updates for Keil, IAR, and JLINK.

Regardless of IDE used, please install the Segger J-Link software - see https://www.segger.com/downloads/jlink. All of the above-mentioned development environments support J-Link, but you must have the latest J-Link software installed. Most alternate development environments also support J-Link.

Please refer to the AmbiqSuite SDK Getting Started Guide for more details on setting up development IDEs to use J-Link.

10. Power Supply Options and Measuring Current

The Apollo510 EVB is intended to operate off a 5 V supply, which is used to generate down-stream voltages.

There are two power supply options for the EVB SoC:

- Operate at 1.8 V by default as provided by the on-board power SYS_VDD. This can be adjusted to 1.9 V by cutting SB3 shown on the Power Supplies page of the EVB schematic.
- Provide externally supplied power via J6 (shown but not labeled) in Figure 12.

Figure 12. J6 External Supply Header

The EVB utilizes jumpers for connecting and disconnecting rails from power supplies, whether generated on-board or off-board. The following figures show the jumper connection strategy among various on-board power supplies and the SoC's power rails.

Figure 13 shows the power sourcing options for VDD_MCU.

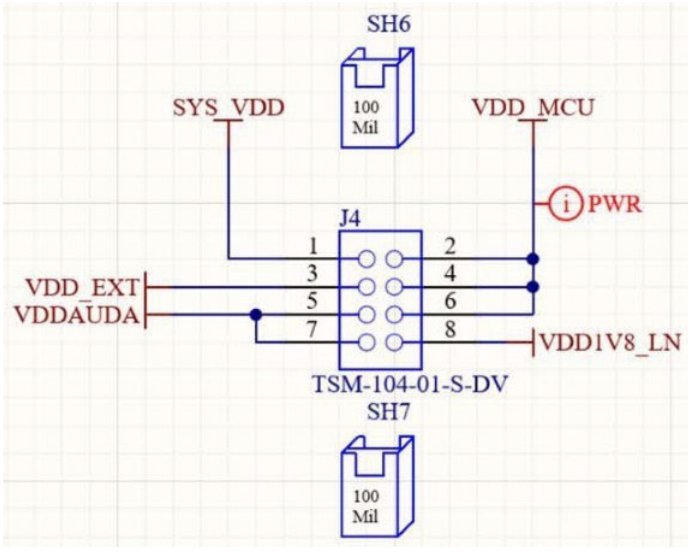


Figure 13. J4 Power Supply Jumper Connections

The J4 default jumper configuration is as shown in Figure 14 and Table 2.

Figure 14. J4 Default Jumper Configuration

Power Supply Source	From Header Pin	To Header Pin	Power Supply Destination
SYS_VDD	J4-1	J4-2	VDD_MCU
VDDAUDA	J4-7	J4-8	VDD1V8_LN

Table 2: J4 Default Jumper Configuration Table

Figure 15 shows the power sourcing options for VDDH4 and VDDH5. VDDH1 and VDDH2 are always sourced from VDD_MCU, and VDDH3 is always sourced from VDD_1V2. VDDH4 can be sourced from VDD_MCU or VDD_1V2, and VDDH5 can be sourced from VDD_MCU, VDD_1V2 or VDD_3V3.

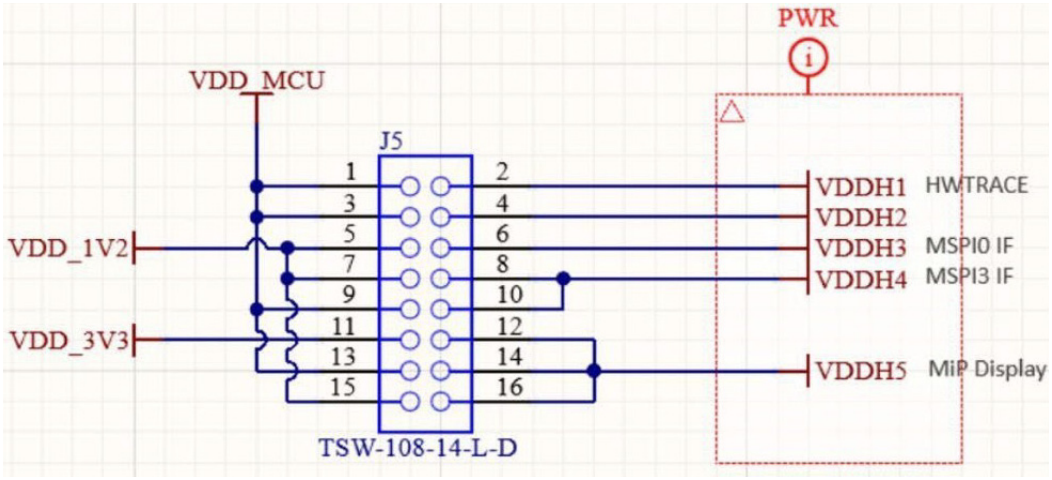


Figure 15. J5 Power Supply Jumper Connections

The J5 default jumper configuration is as shown in Figure 16 and Table 3.

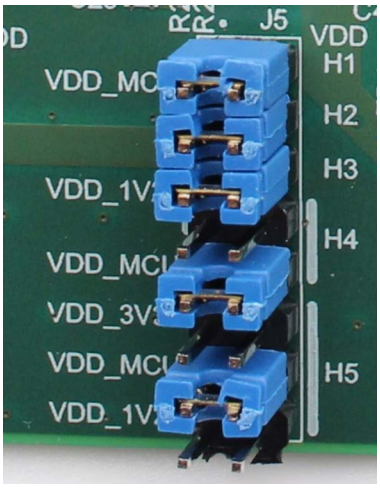


Figure 16. J5 Default Jumper Configuration

Power Supply Source	From Header Pin	To Header Pin	Power Supply Destination
VDD_MCU	J5-1	J5-2	VDDH1
VDD_MCU	J5-3	J5-4	VDDH2
VDD_1V2	J5-5	J5-6	VDDH3
VDD_MCU	J5-9	J5-10	VDDH4
VDD_MCU	J5-13	J5-14	VDDH5

Table 3: J5 Default Jumper Configuration Table

10.1 USB and VDD18/MIPI Load Switch Circuits

Figure 17 shows the USB load switch circuit producing the voltage supplied to VDDUSB33_AP5 and VDDUSB0P9_AP5.

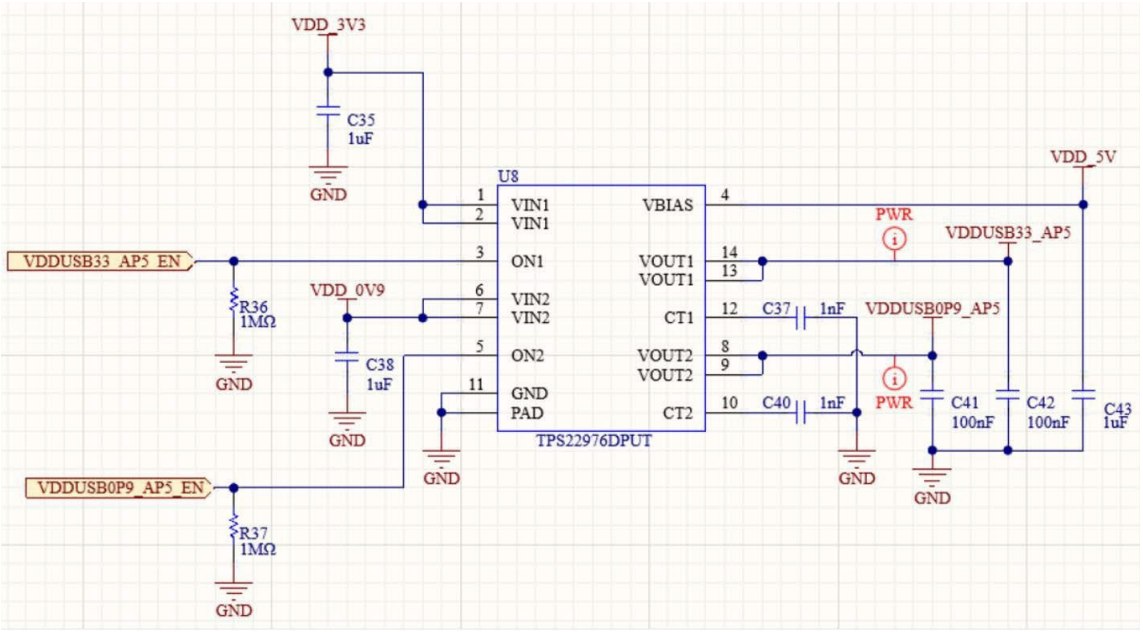


Figure 17. USB Load Switch Circuit

Similarly, Figure 18 shows the load switch circuit that produces the voltage supplied to the MIPI DPHY VDD18.

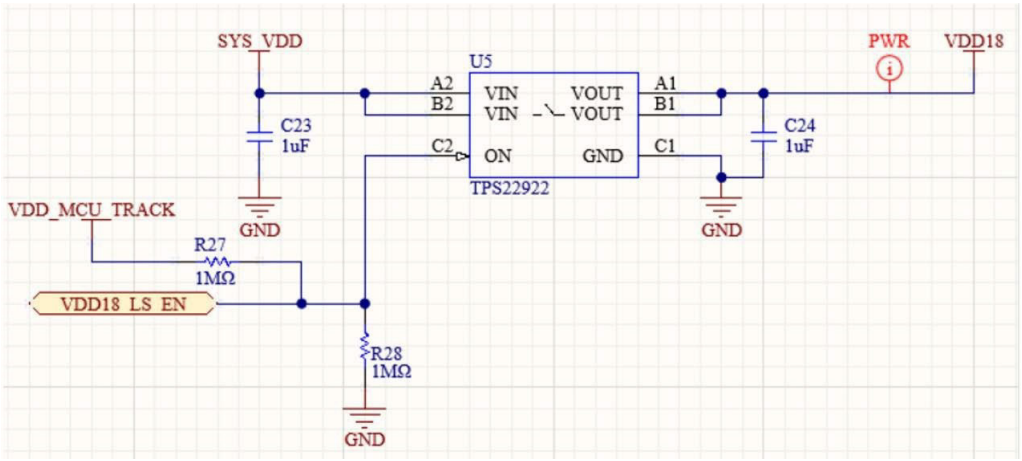


Figure 18. VDD18/MIPI Load Switch Circuit

10.2 Monitoring or Externally Supplying Supply Voltages

As shown in Figure 19 and Figure 19, header J3 provides easy access to the various system and chip-level power supplies present on the EVB. These can be used to monitor voltage or provide externally generated power to each specific rail after assuring that the on-board supply has been disconnected.

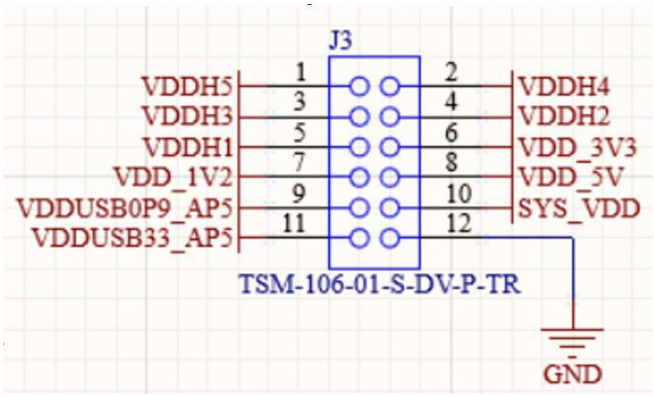


Figure 19. J3 Voltage Test Points Header

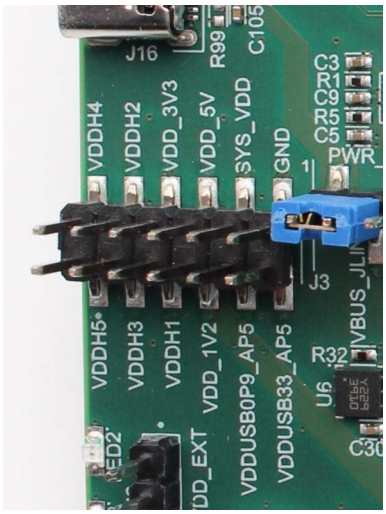


Figure 20. Board View of J3 Voltage Test Points Header

10.3 Measuring Current

Current consumption of the Apollo510 EVB can be measured by connecting an ammeter between the corresponding DUT supplies. Refer to Figure 13 or Figure 15 to measure the current draw from the power supply of interest. Before using an ammeter, turn the power off, remove the corresponding jumper and install the ammeter properly prior to powering the board back on.

When the current measurements have been completed, reposition the jumper at its former location.

11. Ordering Information

Device Name	Orderable Part Number	EVB Revision	SoC
Apollo510 EVB	AP510EVB	2.2	Apollo510 BGA

Table 4: EVB Ordering Information

Device Name[a]	Commercial Temp Range (-20°C to 70°C)	Industrial Temp Range (-40°C to 85°C)	Package Type	GPIOs	NVM (MRAM)[b]	SRAM	Package[c] Size (mm)
Apollo510 SoC	AP510NFA-CBR	AP510NFA-IBR	BGA	183	4 MB	3.75 MB	6.6 x 6.6 x 0.75 225-pin BGA
Apollo510 SoC	AP510NFA-CCR	AP510NFA-ICR	WLCSP	144	4 MB	3.75 MB	4.9 x 4.7 182-pin WLCSP

Table 5: Apollo510 SoC Ordering Information

a. The silicon revision is identified by the first letter in the bottom row of the package's top marking.
b. Factory-installed Cortex-M4 firmware reduces the amount of available NVM which varies for each series derivative. The amount of NVM used will be made available in a future datasheet release.
c. Packing: Tape and Reel

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