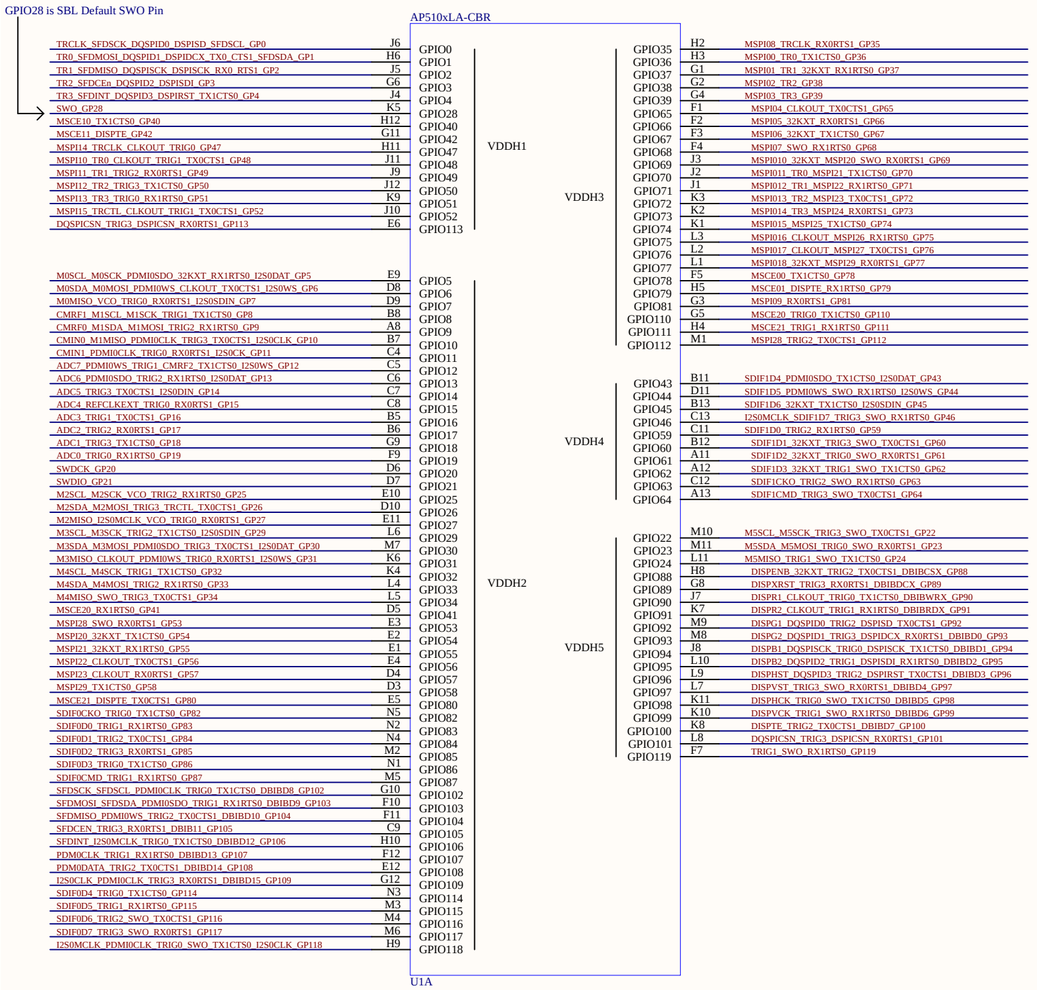
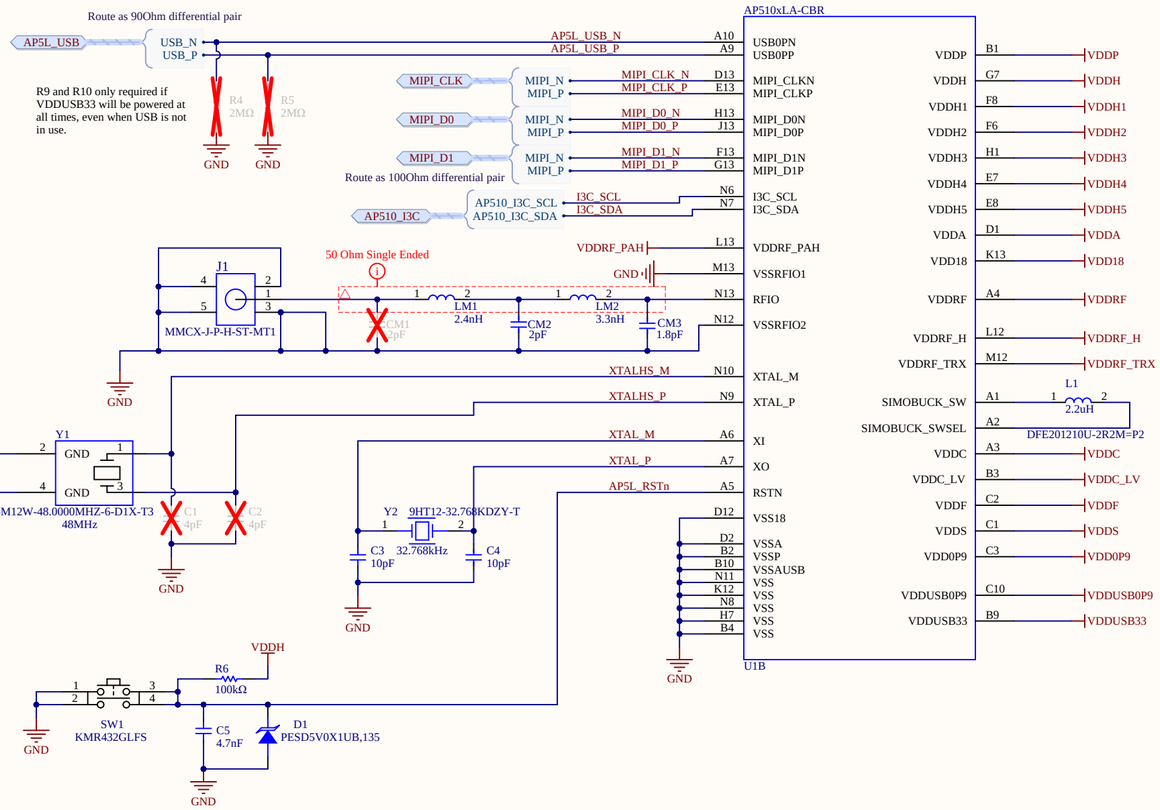




Power Supply Requirements

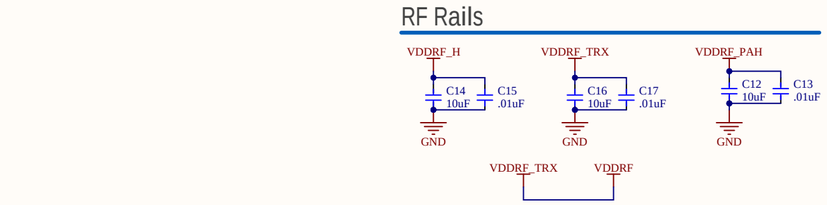
1. VDDP, VDDH, VDDH1, VDDH2, and VDDA should be connected together and powered by the primary rail (1.71 - 2.20V)
2. VDD18, VDDRF_H, and VDDRF_PAH should be supplied by a regulated, low noise, low quiescent current 1.8V LDO.
3. VDDUSB33 should be supplied by a 3.3V regulated supply (3.0 - 3.63V).
4. A 1uF decoupling capacitor can be used for VDDUSB0P9 on BGA package.
5. A 2.2uF decoupling capacitor can be used for VDDUSB33 on BGA package.
6. **If unused, VDDUSB33 and VDDUSB0P9 should be tied to ground on the BGA package. If using USB. It is recommended to have VDDUSB0P9 tied to 0.9V LDO output on the BGA.**
7. VDDH1, VDDH2, VDDH3, VDDH4, and VDDH5 must be tied to VDDH if not used.
8. VDD18 can be tied to ground if MIPI-DSI and Display PLL are not used. MIPI and Display are not available on the Apollo330 Plus Series.

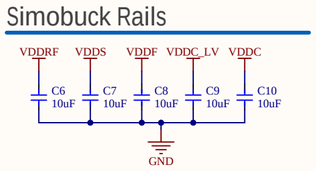
Supply Input Rails

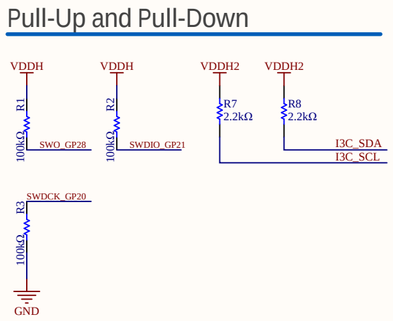
VDDP = 1.71 - 2.20V SIMOBUCK/LDO Supply
VDDH = 1.71 - 2.20V I/O Supply
VDDH1 = 1.71 - 2.20V I/O Supply
VDDH2 = 1.71 - 2.20V GP and I3C I/O
VDDH3 = 1.14 - 2.20V I/O Supply (MSPI support limited to nominal 1.8V)
VDDH4 = 1.71 - 3.63V I/O Supply
VDDH5 = 1.71 - 3.63V I/O Supply
VDDA = 1.71 - 2.20V Analog Supply
VDD18 = 1.71 - 2.20V MIPI PHY Supply - Apollo510L Series Only
VDDUSB33 = 3.0 - 3.63V USB Analog Supply
VDDUSB0P9 = 0.84 - 0.99V USB Core Supply. See VDD0P9 under Regulated Rails.
VDDRF_H = 1.71 - 1.98V RF High Voltage Supply
VDDRF_TRX = 0.95 - 1.98V RF Core Supply
VDDRF_PAH = 1.65 - 1.98V RF High-Power PA Supply

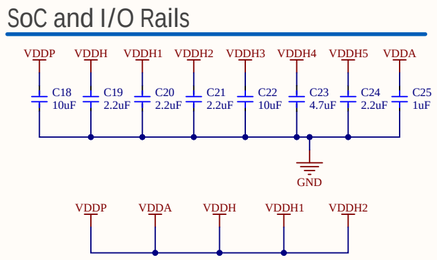
Regulated Rails

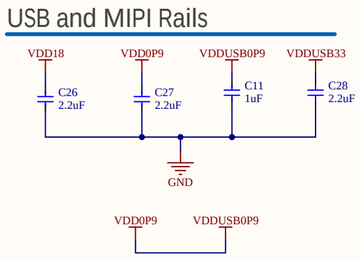
VDDC = Nominal Core (From VDDP)
VDDC_LV = Low Power Core (From VDDP)
VDDF = Nominal Memory (From VDDP)
VDDS = Memory Retention (From VDDP)
VDDRF = Radio IF (From VDDP)
VDD0P9 = LDO for USB PHY Core. VDDUSB0P9 can be connected to the VDD0P9 output.











Title	Apollo510L/Apollo330P BGA Reference
Revision	1.2
Sheet Name	SoC
Sheet	1 of 1
Date	5/22/2026
Number	BGA Reference Schematic