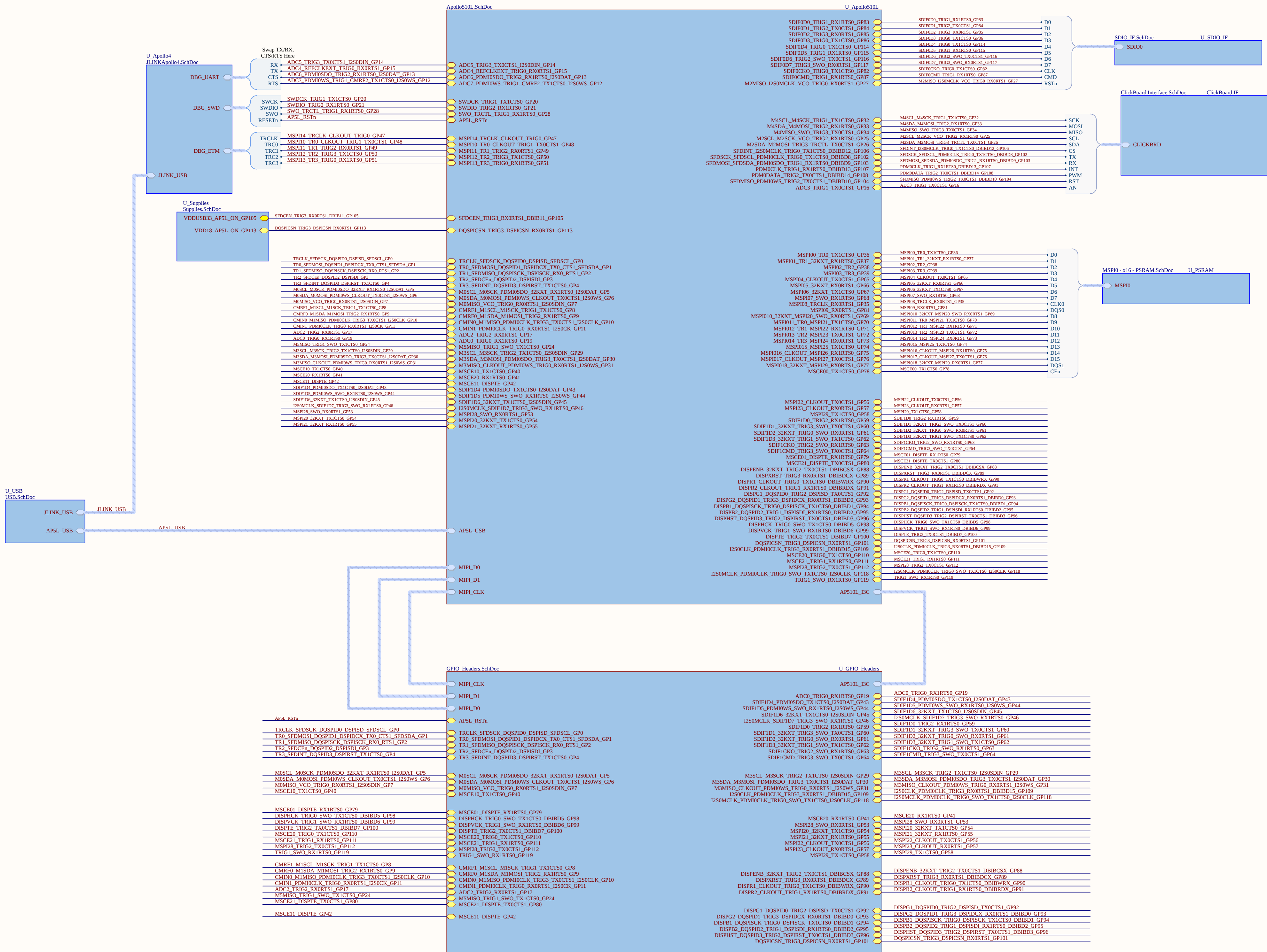


Apollo510L EVB Connection Diagram

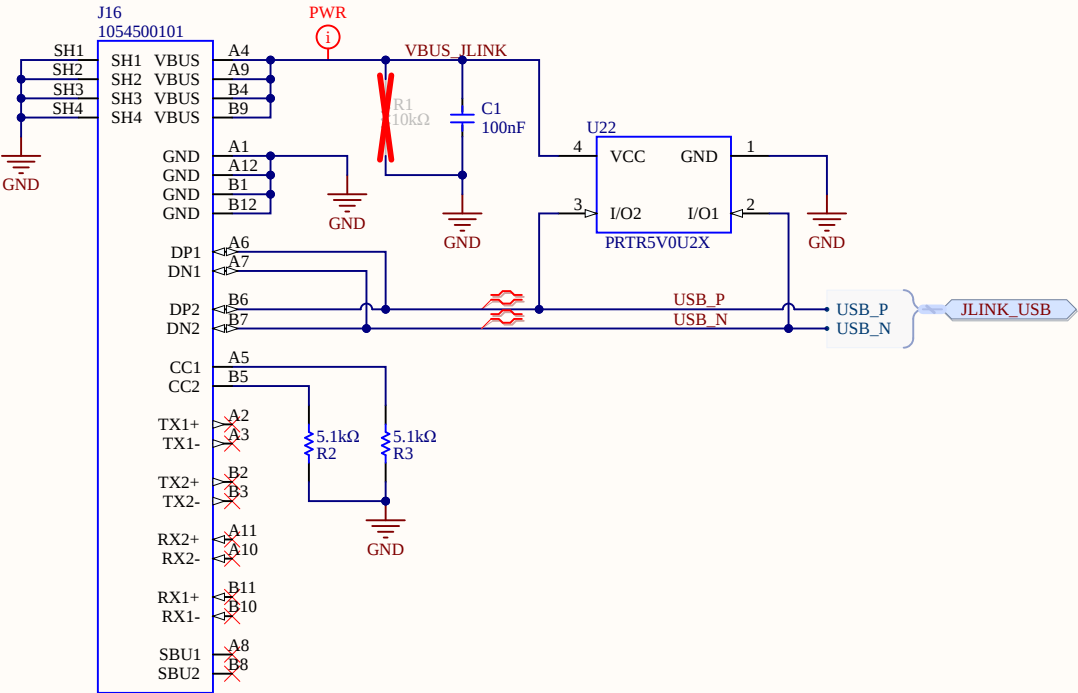


Fiducial Marks

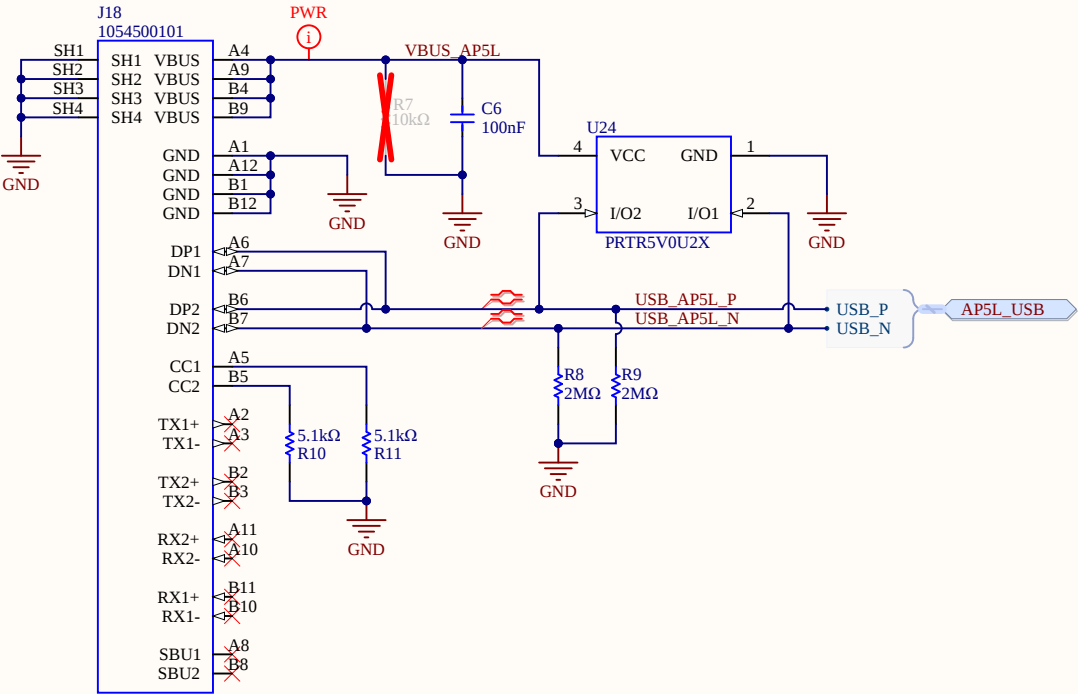
M3 Standoffs

GND Hooks

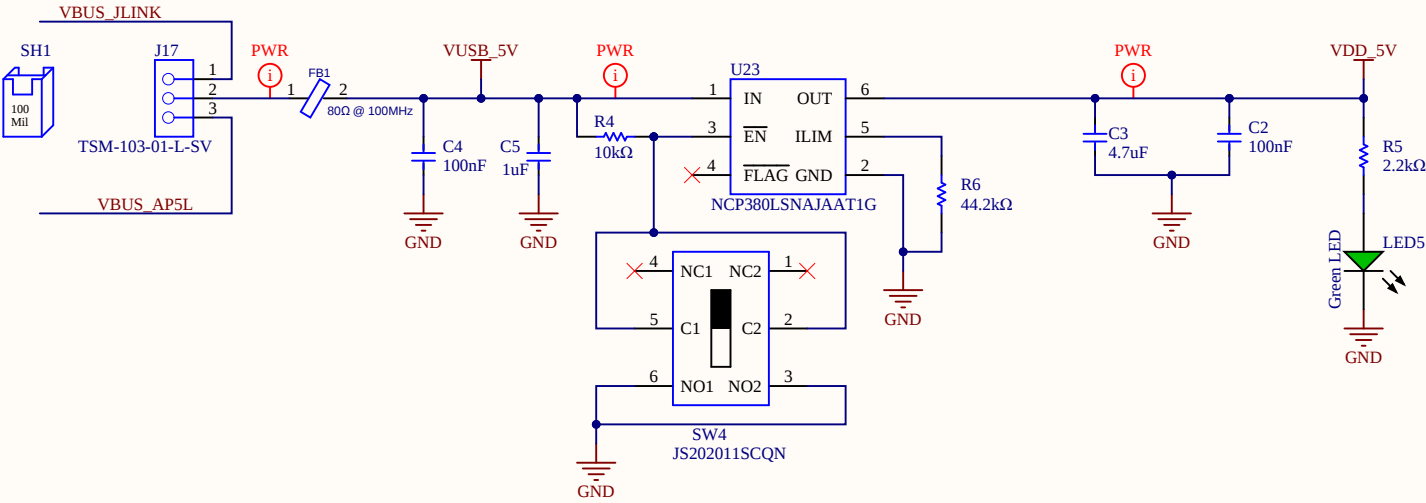
USB-C Connector



AP5 USB-C Connector



5V Source Select & USB Protection Circuit

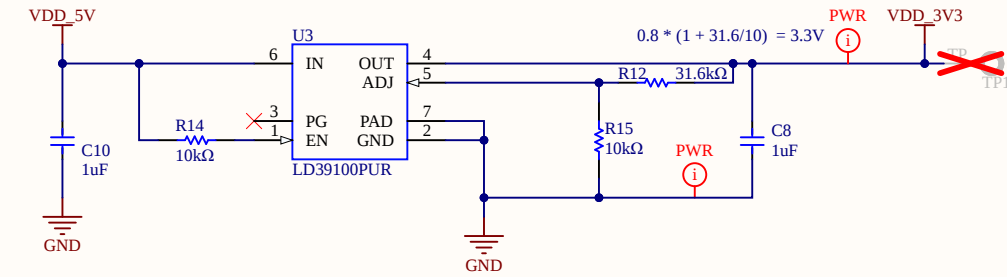




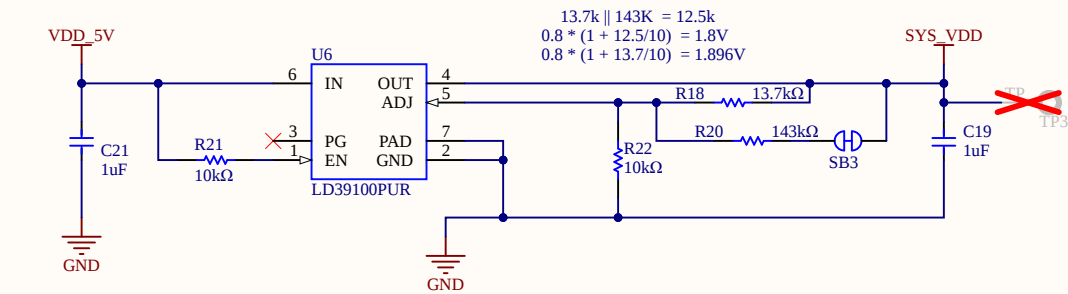
ambiq
endpoint intelligence

Title		Apollo510 Lite Series EVB		Revision	
Sheet Name		USB		2.0	
Date		9/15/2025		Sheet 2 of 9	
Number		AP510DLEVB			
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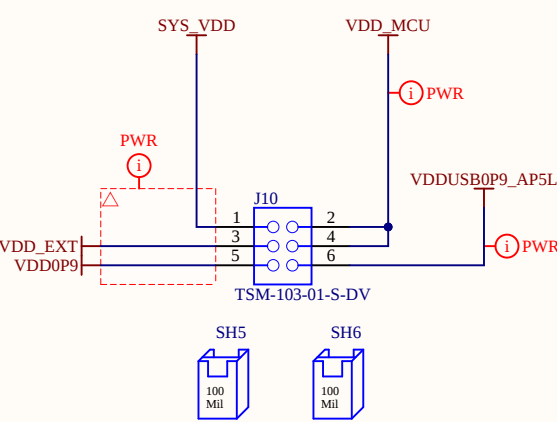
3.3V Supply



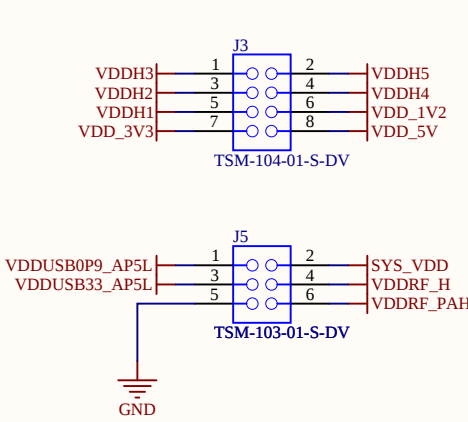
1.8V Supply



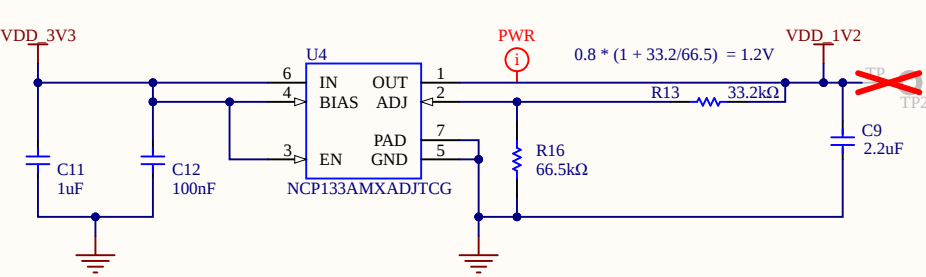
Supply selection



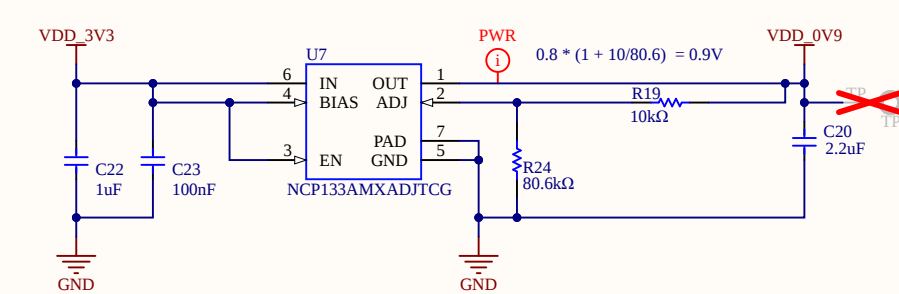
Supply visibility



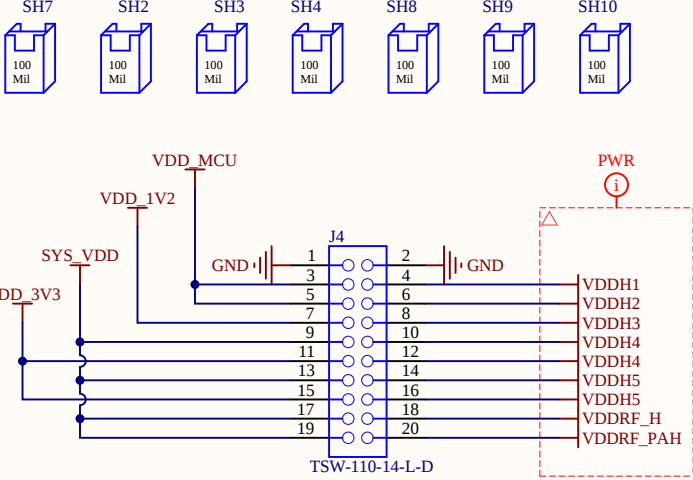
1.2V Supply



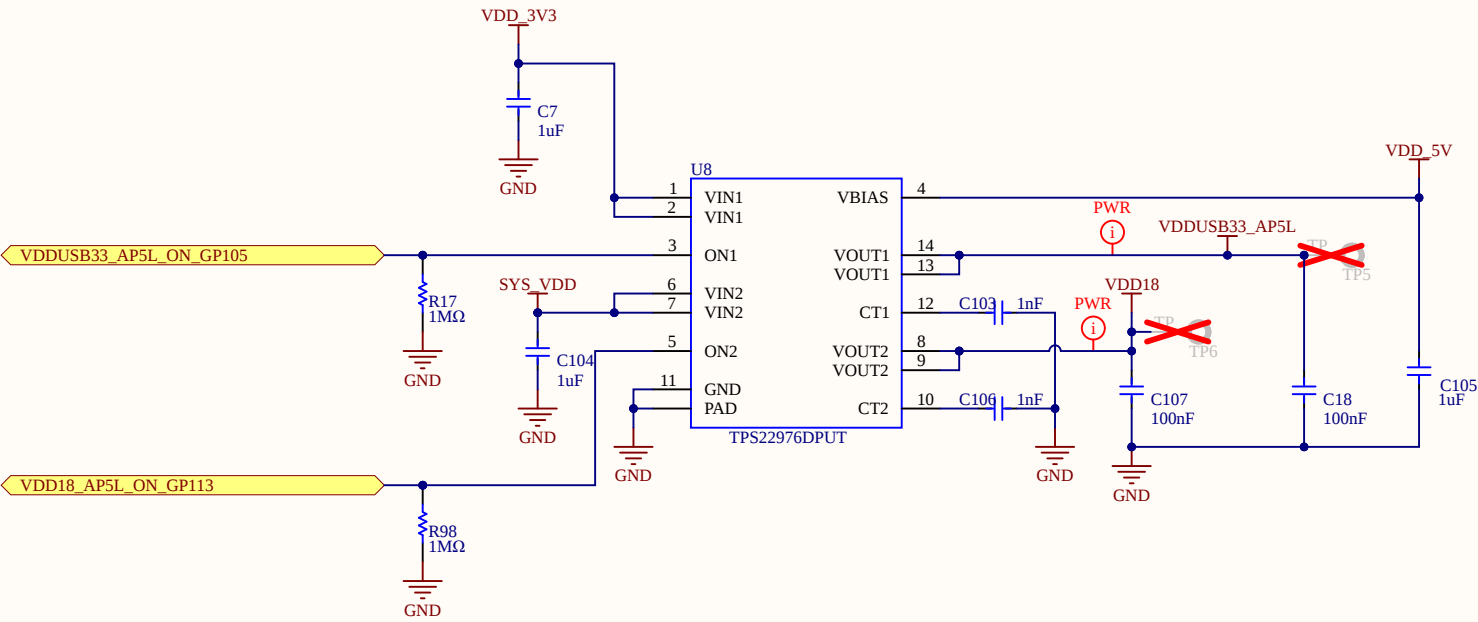
0.9V USB Supply for Apollo4 JLINK OB



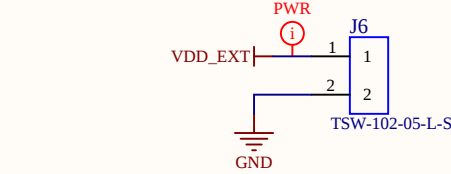
Power Configuration Header



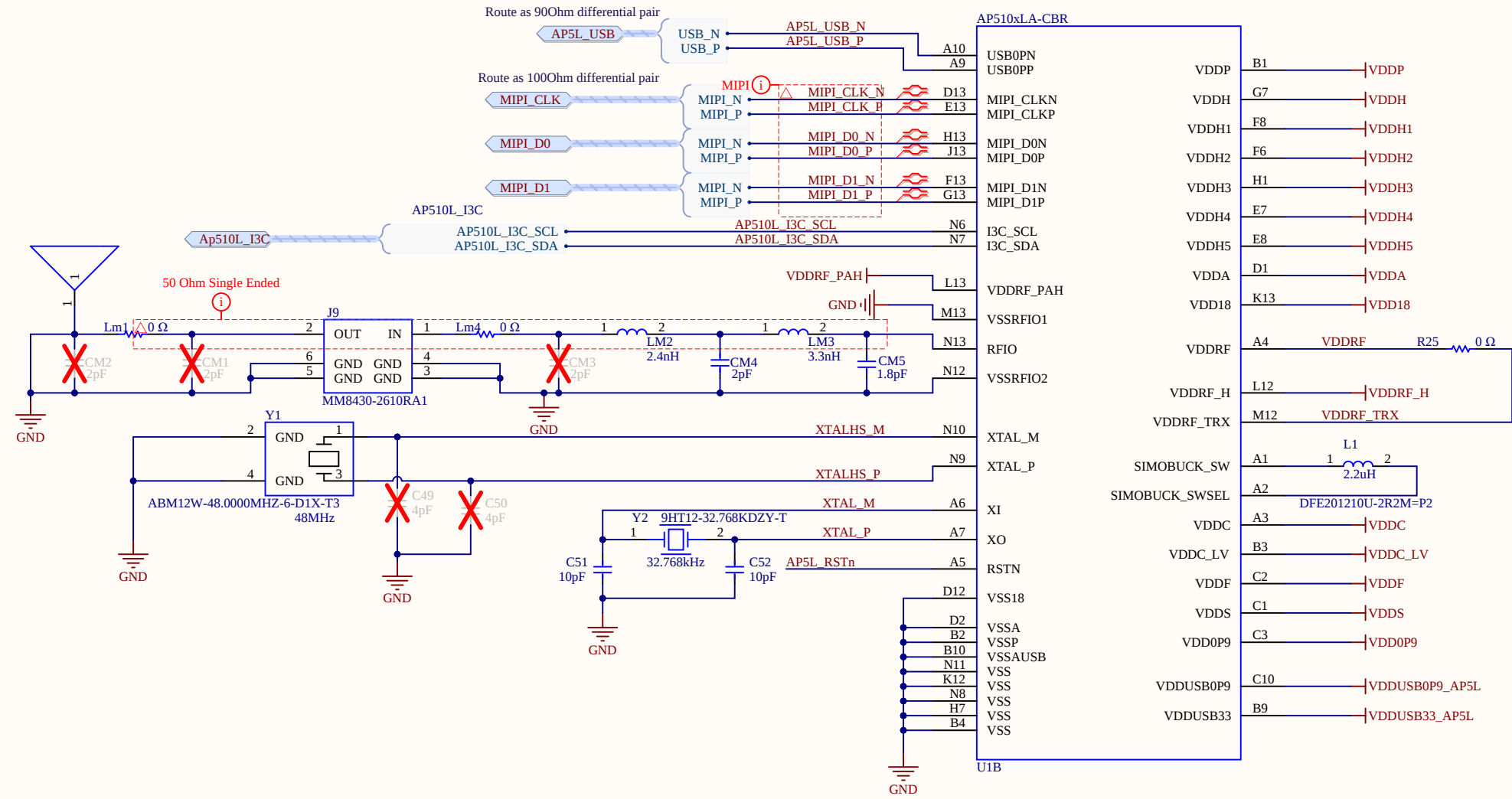
USB 3.3V and Display Controller Loadswitch



External Supply Input

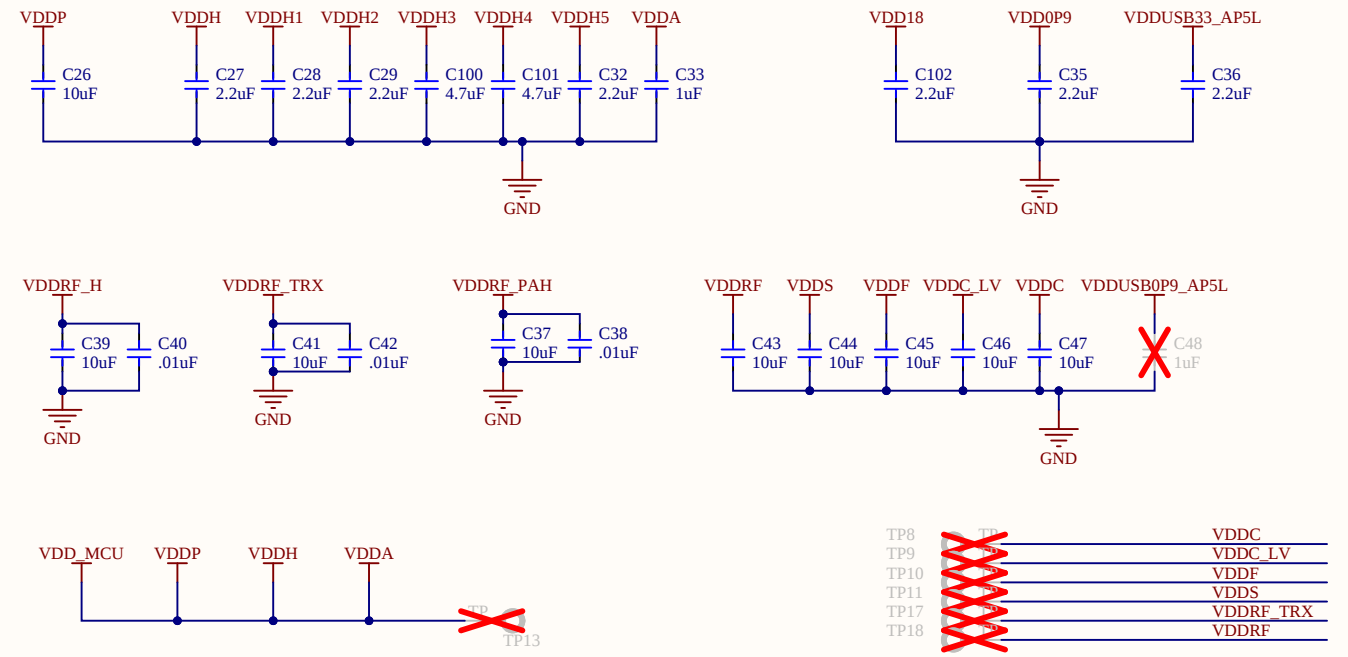


Apollo510L

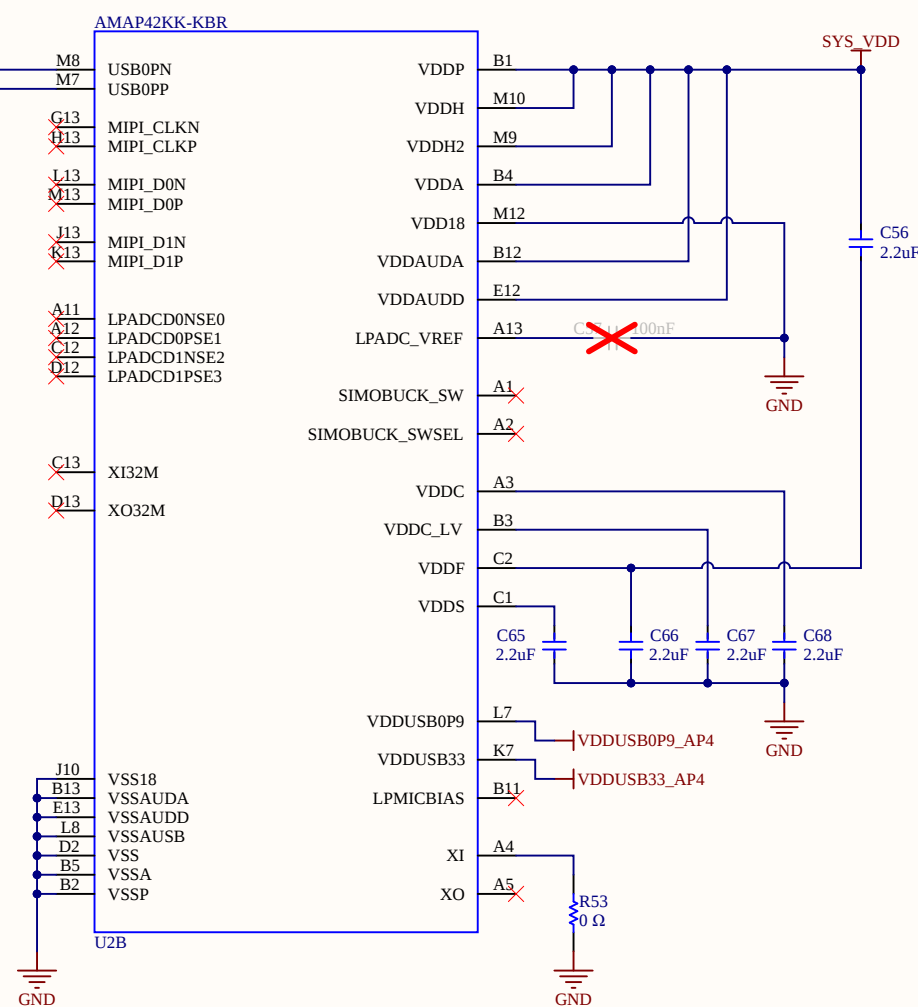
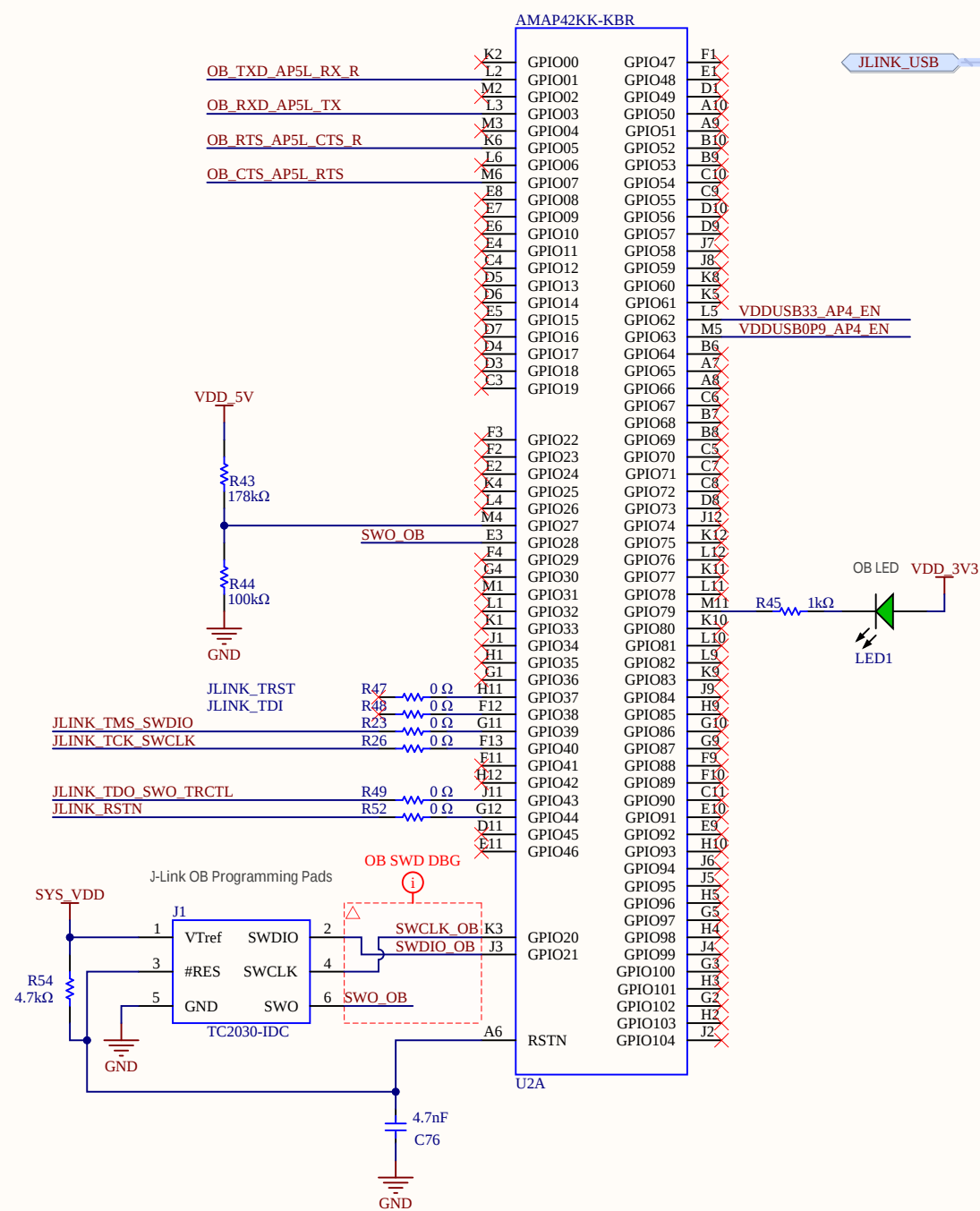


AP510xLA-CBR			
TRCLK_SFDSCK_DQSPID0_DSPISD_SFDSCL_GP0	TRCLK_SFDSCK_DQSPID0_DSPISD_SFDSCL_GP0	J6	GPI05
TR0_SFDMOSI_DQSPID1_DSPIDCX_TX0_CTS1_SFSDSA_GP1	TR0_SFDMOSI_DQSPID1_DSPIDCX_TX0_CTS1_SFSDSA_GP1	J5	GPI01
TR1_SFDMISO_DQSPISCK_DSPISCK_RX0_RTS1_GP2	TR1_SFDMISO_DQSPISCK_DSPISCK_RX0_RTS1_GP2	J6	GPI02
TR2_SFDCEN_DQSPID2_DSPISDI_GP3	TR2_SFDCEN_DQSPID2_DSPISDI_GP3	J4	GPI03
TR3_SFDMISO_DQSPID3_DSPISDI_TXICTS0_GP4	TR3_SFDMISO_DQSPID3_DSPISDI_TXICTS0_GP4	J6	GPI04
SWO_TRCTL_TRIG1_RXIRTS0_GP28	SWO_TRCTL_TRIG1_RXIRTS0_GP28	K5	GPI028
MSCE10_TXICTS0_GP40	MSCE10_TXICTS0_GP40	H12	GPI040
MSCE11_DISPTE_GP42	MSCE11_DISPTE_GP42	G11	GPI042
MSPI14_TRCLK_CLKOUT_TRIG0_GP47	MSPI14_TRCLK_CLKOUT_TRIG0_GP47	H11	GPI047
MSPI10_TR0_CLKOUT_TRIG1_TXOCTS1_GP48	MSPI10_TR0_CLKOUT_TRIG1_TXOCTS1_GP48	J11	GPI048
MSPI11_TR1_TRIG2_RXORTS1_GP49	MSPI11_TR1_TRIG2_RXORTS1_GP49	J9	GPI049
MSPI12_TR2_TRIG3_TXICTS0_GP50	MSPI12_TR2_TRIG3_TXICTS0_GP50	J12	GPI050
MSPI12_TR2_TRIG3_TXICTS0_GP50	MSPI12_TR2_TRIG3_TXICTS0_GP50	K9	GPI051
MSPI13_TR3_TRIG0_RXIRTS0_GP51	MSPI13_TR3_TRIG0_RXIRTS0_GP51	J10	GPI052
MSPI15_TRCTL_CLKOUT_TRIG1_TXOCTS1_GP52	MSPI15_TRCTL_CLKOUT_TRIG1_TXOCTS1_GP52	J10	GPI053
DQSPICSN_TRIG3_DSPICSN_RXORTS1_GP113	DQSPICSN_TRIG3_DSPICSN_RXORTS1_GP113	E6	GPI0113
MSCL_M5SCK_PDMIOSD0_32KXT_RXIRTS0_I2S0DAT_GP5	MSCL_M5SCK_PDMIOSD0_32KXT_RXIRTS0_I2S0DAT_GP5	E9	GPI05
M5SDA_M5MOSI_PDMIOWS_CLKOUT_TXOCTS1_I2S0WS_GP6	M5SDA_M5MOSI_PDMIOWS_CLKOUT_TXOCTS1_I2S0WS_GP6	D8	GPI06
M5MISO_VCO_TRIG0_RXORTS1_I2S0SDIN_GP7	M5MISO_VCO_TRIG0_RXORTS1_I2S0SDIN_GP7	D9	GPI07
CMRF1_M5SCK_M5SCK_TRIG1_TXICTS0_GP8	CMRF1_M5SCK_M5SCK_TRIG1_TXICTS0_GP8	B8	GPI08
CMRF0_M5SDA_M5MOSI_TRIG2_RXIRTS0_GP9	CMRF0_M5SDA_M5MOSI_TRIG2_RXIRTS0_GP9	A8	GPI09
CMIN0_M5MISO_PDMIOCLK_TRIG3_TXOCTS1_I2S0CLK_GP10	CMIN0_M5MISO_PDMIOCLK_TRIG3_TXOCTS1_I2S0CLK_GP10	B7	GPI010
CMIN1_PDMIOCLK_TRIG0_RXORTS1_I2S0CK_GP11	CMIN1_PDMIOCLK_TRIG0_RXORTS1_I2S0CK_GP11	C4	GPI011
ADC7_PDMIOWS_TRIG1_CMRF2_TXICTS0_I2S0WS_GP12	ADC7_PDMIOWS_TRIG1_CMRF2_TXICTS0_I2S0WS_GP12	C5	GPI012
ADC6_PDMIOSD0_TRIG2_RXIRTS0_I2S0DAT_GP13	ADC6_PDMIOSD0_TRIG2_RXIRTS0_I2S0DAT_GP13	C6	GPI013
ADC5_TRIG3_TXOCTS1_I2S0DIN_GP14	ADC5_TRIG3_TXOCTS1_I2S0DIN_GP14	C7	GPI014
ADC4_REFCLKEXT_TRIG0_RXORTS1_GP15	ADC4_REFCLKEXT_TRIG0_RXORTS1_GP15	C8	GPI015
ADC3_TRIG1_TXOCTS1_GP16	ADC3_TRIG1_TXOCTS1_GP16	B5	GPI016
ADC2_TRIG2_RXORTS1_GP17	ADC2_TRIG2_RXORTS1_GP17	B6	GPI017
ADC0_TRIG0_RXIRTS0_GP19	ADC0_TRIG0_RXIRTS0_GP19	F9	GPI018
SWDCK_TRIG1_TXICTS0_GP20	SWDCK_TRIG1_TXICTS0_GP20	D6	GPI019
SWDIO_TRIG2_RXIRTS0_GP21	SWDIO_TRIG2_RXIRTS0_GP21	D7	GPI020
M2SCL_M2SCK_VCO_TRIG2_RXIRTS0_GP25	M2SCL_M2SCK_VCO_TRIG2_RXIRTS0_GP25	E10	GPI021
M2SDA_M2MOSI_TRIG3_TRCTL_TXOCTS1_GP26	M2SDA_M2MOSI_TRIG3_TRCTL_TXOCTS1_GP26	D10	GPI022
M2MISO_I2S0MCLK_VCO_TRIG0_RXORTS1_GP27	M2MISO_I2S0MCLK_VCO_TRIG0_RXORTS1_GP27	E11	GPI023
M3SCL_M3SCK_TRIG2_TXICTS0_I2S0SDIN_GP29	M3SCL_M3SCK_TRIG2_TXICTS0_I2S0SDIN_GP29	L6	GPI029
M3SDA_M3MOSI_PDMIOSD0_TRIG3_TXOCTS1_I2S0DAT_GP30	M3SDA_M3MOSI_PDMIOSD0_TRIG3_TXOCTS1_I2S0DAT_GP30	M7	GPI030
M4SCL_M4SCK_TRIG1_TXICTS0_GP32	M4SCL_M4SCK_TRIG1_TXICTS0_GP32	K4	GPI032
M4SDA_M4MOSI_TRIG2_RXIRTS0_GP33	M4SDA_M4MOSI_TRIG2_RXIRTS0_GP33	L4	GPI033
M4MISO_SWO_TRIG3_TXOCTS1_GP34	M4MISO_SWO_TRIG3_TXOCTS1_GP34	L5	GPI034
MSCE20_RXIRTS0_GP41	MSCE20_RXIRTS0_GP41	D5	GPI041
MSPI28_SWO_RXORTS1_GP53	MSPI28_SWO_RXORTS1_GP53	E1	GPI053
MSPI20_32KXT_TXICTS0_GP54	MSPI20_32KXT_TXICTS0_GP54	E2	GPI054
MSPI21_32KXT_RXIRTS0_GP55	MSPI21_32KXT_RXIRTS0_GP55	E3	GPI055
MSPI22_32KXT_TXICTS0_GP56	MSPI22_32KXT_TXICTS0_GP56	E4	GPI056
MSPI23_CLKOUT_TXOCTS1_GP57	MSPI23_CLKOUT_TXOCTS1_GP57	D4	GPI057
MSPI23_CLKOUT_TXOCTS1_GP57	MSPI23_CLKOUT_TXOCTS1_GP57	D3	GPI058
MSPI29_TXICTS0_GP58	MSPI29_TXICTS0_GP58	D3	GPI059
MSCE21_DISPTE_TXOCTS1_GP80	MSCE21_DISPTE_TXOCTS1_GP80	E5	GPI080
SDIF0CKO_TRIG0_TXICTS0_GP82	SDIF0CKO_TRIG0_TXICTS0_GP82	N5	GPI082
SDIF0D0_TRIG1_RXIRTS0_GP83	SDIF0D0_TRIG1_RXIRTS0_GP83	N2	GPI083
SDIF0D1_TRIG2_TXOCTS1_GP84	SDIF0D1_TRIG2_TXOCTS1_GP84	N4	GPI084
SDIF0D2_TRIG3_RXORTS1_GP85	SDIF0D2_TRIG3_RXORTS1_GP85	N1	GPI085
SDIF0D3_TRIG0_TXICTS0_GP86	SDIF0D3_TRIG0_TXICTS0_GP86	N1	GPI086
SDIF0D4_TRIG1_RXIRTS0_GP87	SDIF0D4_TRIG1_RXIRTS0_GP87	M5	GPI087
SFDSCK_SFDSCL_PDMIOCLK_TRIG0_TXICTS0_DBIBD0_GP102	SFDSCK_SFDSCL_PDMIOCLK_TRIG0_TXICTS0_DBIBD0_GP102	G10	GPI0102
SFDMOSI_SFSDSA_PDMIOSD0_TRIG1_RXIRTS0_DBIBD0_GP103	SFDMOSI_SFSDSA_PDMIOSD0_TRIG1_RXIRTS0_DBIBD0_GP103	F10	GPI0103
SFDMISO_PDMIOWS_TRIG2_TXOCTS1_DBIBD10_GP104	SFDMISO_PDMIOWS_TRIG2_TXOCTS1_DBIBD10_GP104	F11	GPI0104
SFDCEN_TRIG3_RXORTS1_DBIB11_GP105	SFDCEN_TRIG3_RXORTS1_DBIB11_GP105	C9	GPI0105
SFDMISO_PDMIOWS_TRIG2_TXOCTS1_DBIBD10_GP106	SFDMISO_PDMIOWS_TRIG2_TXOCTS1_DBIBD10_GP106	H10	GPI0106
PDMIOCLK_TRIG1_RXIRTS0_DBIBD13_GP107	PDMIOCLK_TRIG1_RXIRTS0_DBIBD13_GP107	F12	GPI0107
PDMIODATA_TRIG2_TXOCTS1_DBIBD14_GP108	PDMIODATA_TRIG2_TXOCTS1_DBIBD14_GP108	F12	GPI0108
I2S0CLK_PDMIOCLK_TRIG3_RXORTS1_DBIBD15_GP109	I2S0CLK_PDMIOCLK_TRIG3_RXORTS1_DBIBD15_GP109	N3	GPI0109
SDIF0D4_TRIG0_TXICTS0_GP114	SDIF0D4_TRIG0_TXICTS0_GP114	N3	GPI0114
SDIF0D5_TRIG1_RXIRTS0_GP115	SDIF0D5_TRIG1_RXIRTS0_GP115	M3	GPI0115
SDIF0D6_TRIG2_SWO_TXOCTS1_GP116	SDIF0D6_TRIG2_SWO_TXOCTS1_GP116	M4	GPI0116
SDIF0D7_TRIG3_SWO_RXORTS1_GP117	SDIF0D7_TRIG3_SWO_RXORTS1_GP117	M6	GPI0117
I2S0MCLK_PDMIOCLK_TRIG0_SWO_TXICTS0_I2S0CLK_GP118	I2S0MCLK_PDMIOCLK_TRIG0_SWO_TXICTS0_I2S0CLK_GP118	H9	GPI0118

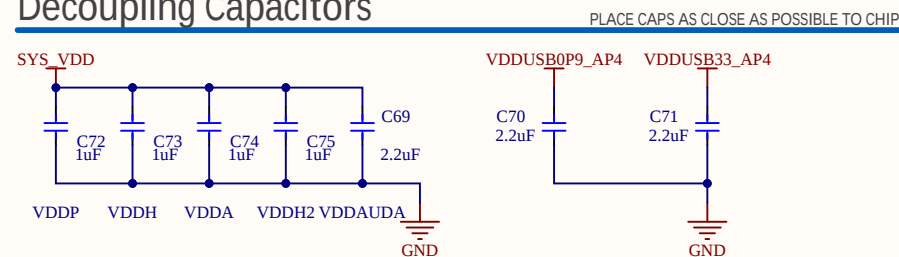
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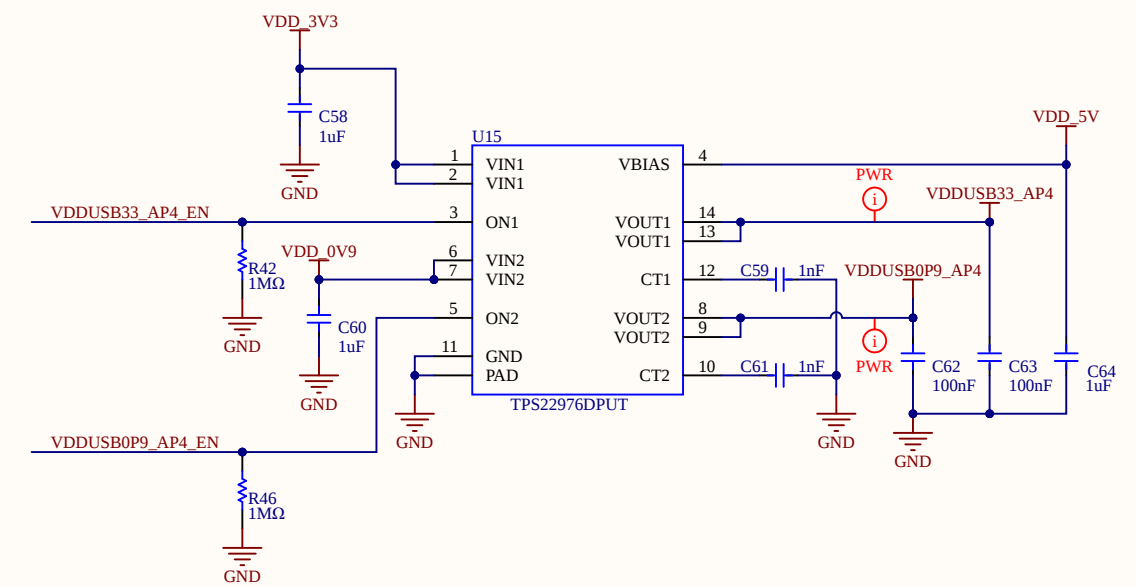
JLINK OB Debugger



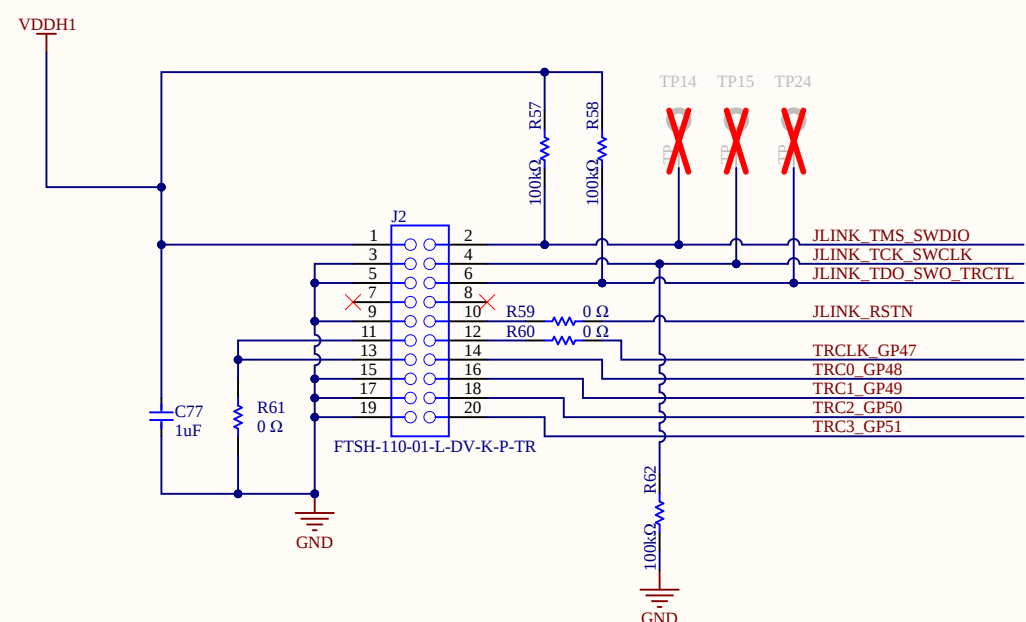
Decoupling Capacitors



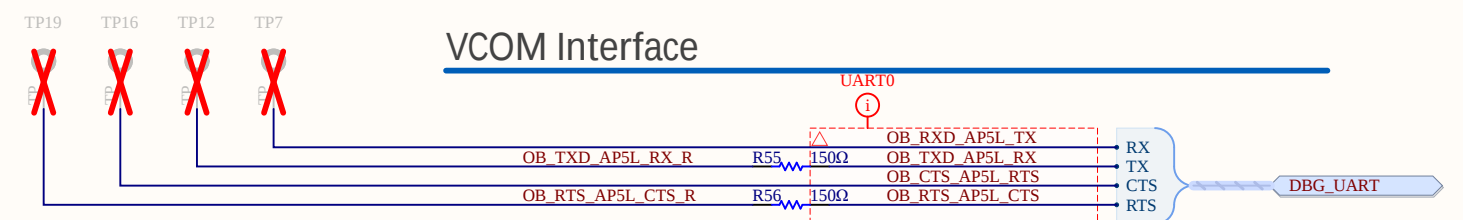
USB Sequencing for OB



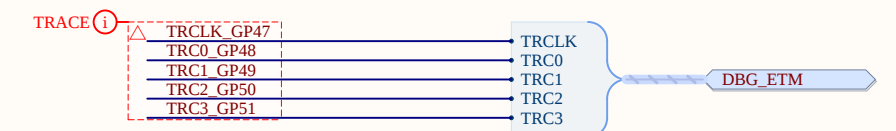
20Pin Cortex Debug + ETM



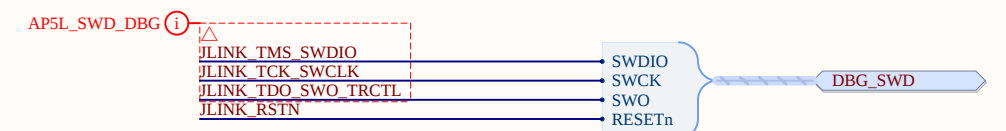
VCOM Interface



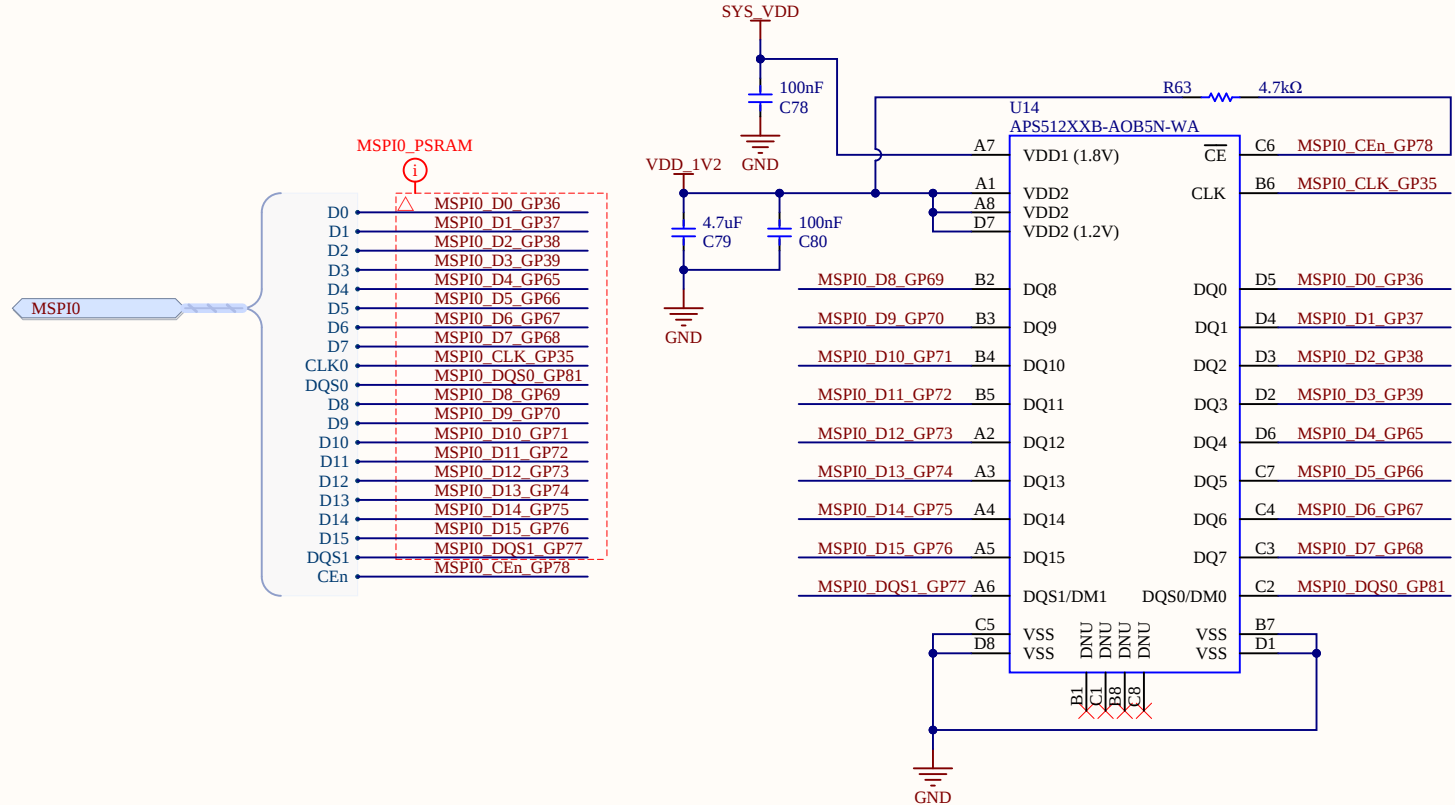
ETM Interface



Target Debug Interface



MSPI0 - x16 - PSRAM



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MSPI0 - x16 - PSRAM

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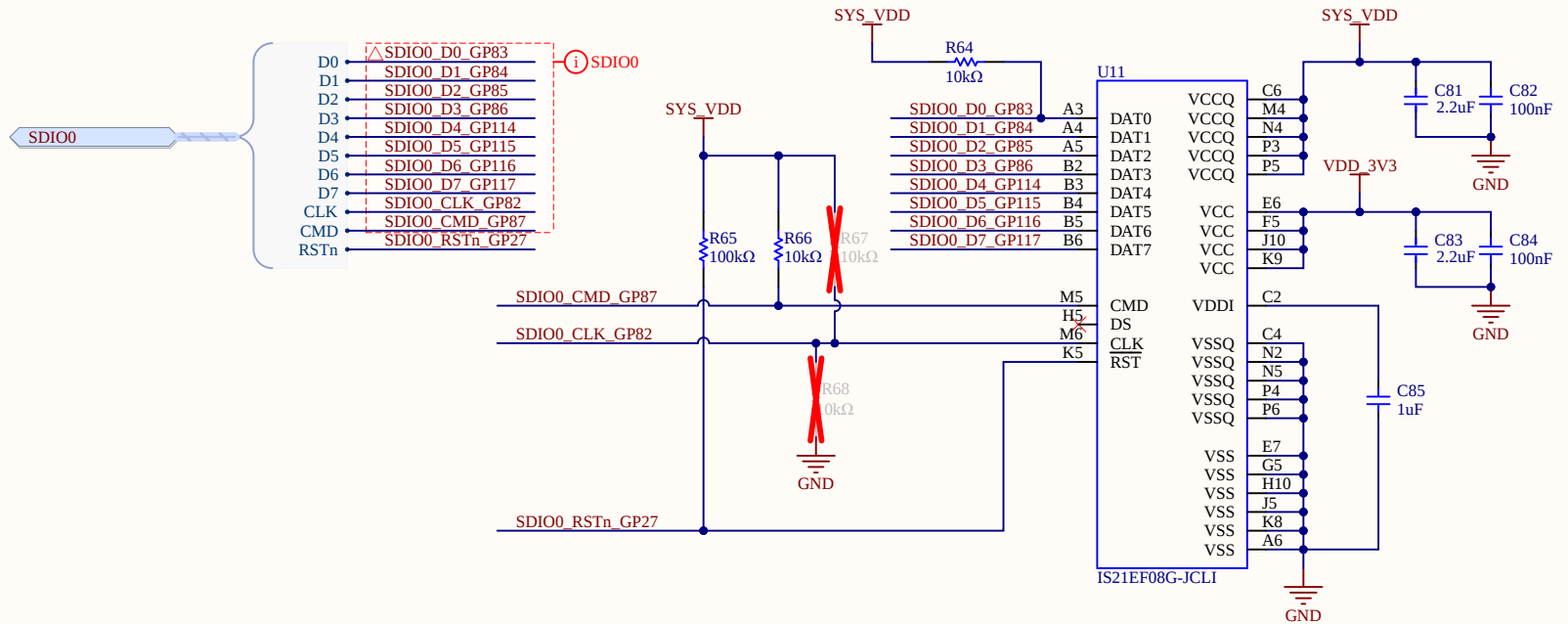
Date
8/7/2025

Number
AP510DLEVB

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SDIOs Ports

eMMC0



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SDIO_IF		
Date	Number	
10/20/2025	AP510DLEVB	

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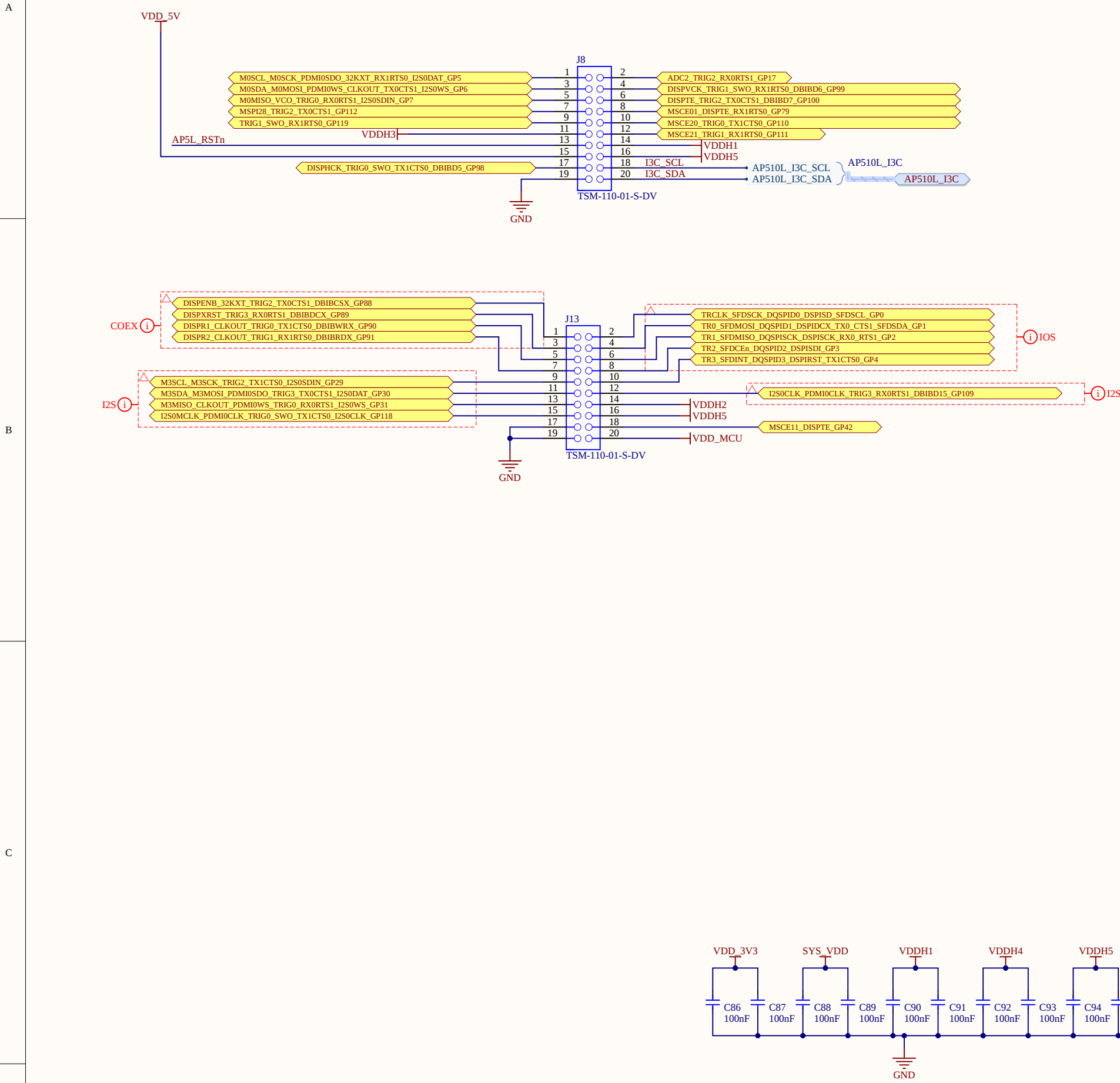
GPIO Headers

A

B

C

D



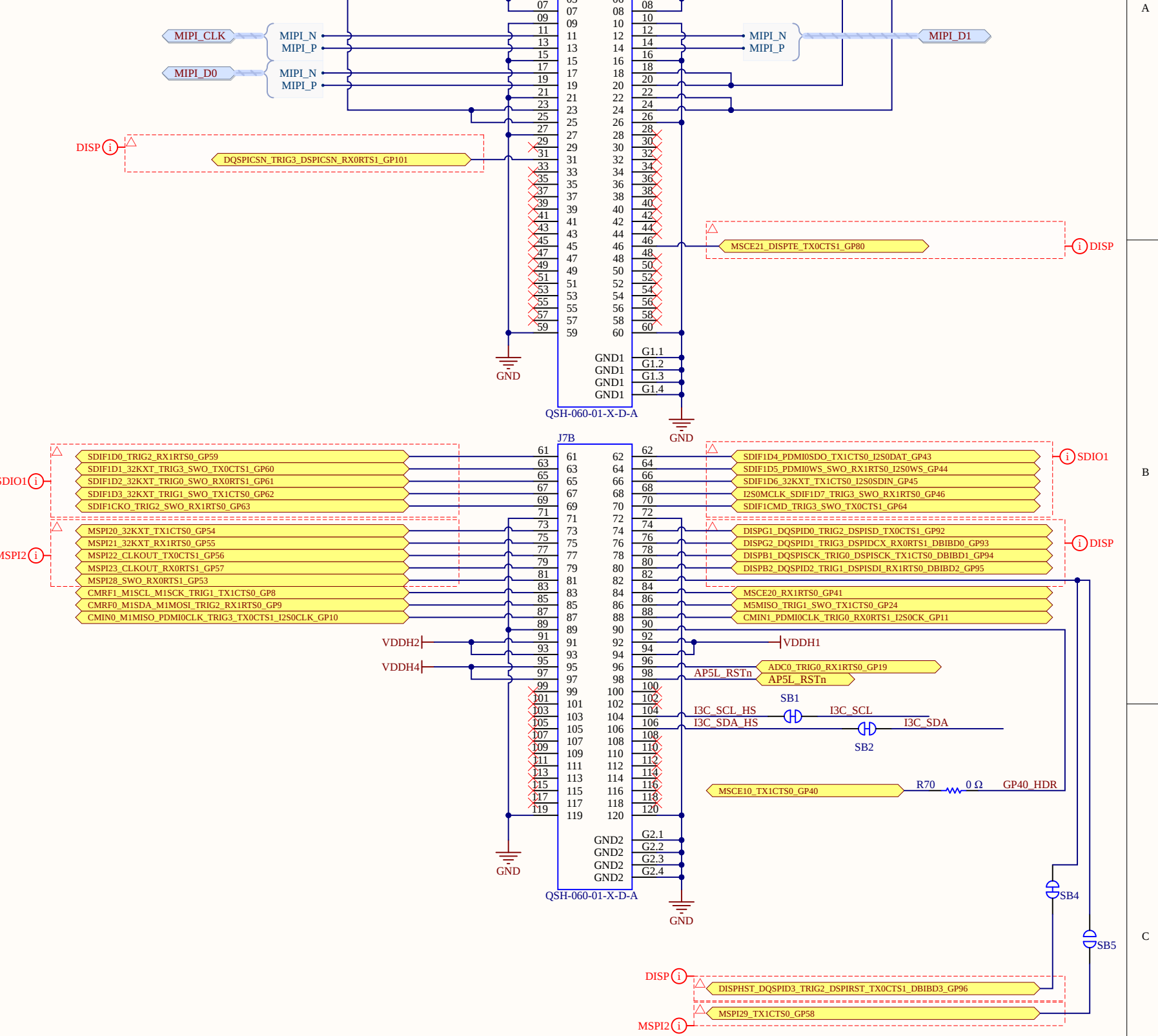
High-Speed Header

A

B

C

D



ClickBoard Interface

