QUICK START GUIDE

Apollo510 Lite Series EVB

(EVB Revision 2.0)

Ultra-low Power Apollo SoC Family

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Document Revision 2.0, June 2026

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1. Introduction

This document provides guidance for setting up the Apollo510 Lite Series Evaluation Board (EVB), revision 2.0, part number AP510DLEVB, to get started executing code examples, measuring power consumption in various configurations, and beginning software development.

FCC Regulatory Notice
This kit has not been authorized under the rules of the FCC. It is designed to: 1. Allow product developers to evaluate electronic components, circuitry or software associated with the kit to determine whether to incorporate such items in a finished product. 2. Enable software developers to write software applications for use with the end product. This kit is not a finished product and may not be resold or otherwise marketed unless all required FCC authorizations are first obtained. **Developers using this reference design in their product are responsible for obtaining all required FCC equipment authorizations.** Operation of this kit is subject to the condition that it does not cause harmful interference to licensed radio stations and that it accepts any harmful interference received. Unless the assembled kit is designed to operate under part 15, part 18, or part 95 of 47 CFR Chapter I - FCC, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of the latter chapter.

2. Document Revision History

Table 1: Document Revision History

Rev #	Date	Description
1.0	Dec 2025	Document initial beta release
2.0	June 2026	- Updated for EVB Revision 2.0 - Updated Legal Information and Disclaimers - Added Power Consumption Measurement Procedure for Apollo510 Lite - Updated EVB and SoC Ordering Information tables

3. Reference Documents and Software

The latest version of the following items, which can be acquired through your Ambiq Sales contact, may be useful in understanding and using the EVB.

- EVB Schematic
- Apollo510 Lite Series Datasheet
- Apollo5 Family Technical Reference Manual
- Apollo510 Lite Series Errata List
- AmbiqSuite SDK

4. Quick Start

The EVB Kit comes with the following items:

- Apollo510 Lite Series Evaluation Board (EVB), revision 2.0
- USB Type C cable
- Four adhesive-backed rubber feet
- Extra jumpers

Caution: The EVB has components loaded on the back of the board. Care should be taken to not damage these components. The included rubber feet should be applied to the bottom of the board to prevent direct contact between the components and a desk surface.

The EVB comes with jumpers pre-configured for default operation. To start EVB program execution, connect the USB-C cable from a USB port on a PC to the J-Link USB connector (J16) on the EVB, and turn on the power switch (SW4). The green LED next to the power switch should illuminate.

The AmbiqSuite SDK provides many example programs that may be run on the EVB. To run these examples, download the SDK from the Ambiq Content Portal (https://contentportal.ambiq.com/login) and select any of the pre-built examples in the SDK at /boards/apollo510dL_evb/examples. The examples should be programmed at address 0x410000.

5. Overview of the Apollo510 Lite Series EVB

The Apollo510 Lite Series EVB has the following features:

- Apollo510D Lite Arm® Cortex®-M55 based SoC in the BGA package (AP510DLA-CBR)
- USB Type C connector for power/download/debug (J16)
- USB Type C connector for power/data to Apollo510D Lite SoC (J18)
- On-board Segger J-Link debugger
- Debug-in port (J2) (SWD or ETM)
- Three user-controlled LEDs
- Two push buttons for application use, plus a reset push button
- Power slide switch with LED power indicator
- On-board interfaces:
  - SDIO 8 GB eMMC (ISSI IS21EF08G-JCLI)
  - High-speed expansion connector
  - MikroBUS socket interface (3.3V or 1.8V interface)
- General purpose male headers (J8 and J13) for I/O and power access to a shield board
- High-speed connector (J7 - QSH-060-01-X-D-A) for interfacing to add-on cards
- RF switch/connector (Murata MM8430-2610RA1) for BLE PHY testing
- Test points for voltage measurements and jumpers for current measurements
- Solder bridge options for power supply flexibility and peripheral access options
- RoHS compliant

CAUTION: The EVB has components loaded on the back of the board. Care should be taken to not damage these components.

NOTE: This EVB may be used for non-BLE applications and in this use case, simply disregard the BLE features.

NOTE: All Revision 2.0 EVBs have the PSRAM (U14) and its corresponding passive components (C78, C79, C80, and R63) de-populated.

The following figures show the board layout, its major components and the location of all components.

Figure 1. EVB Top View - Rev 2.0

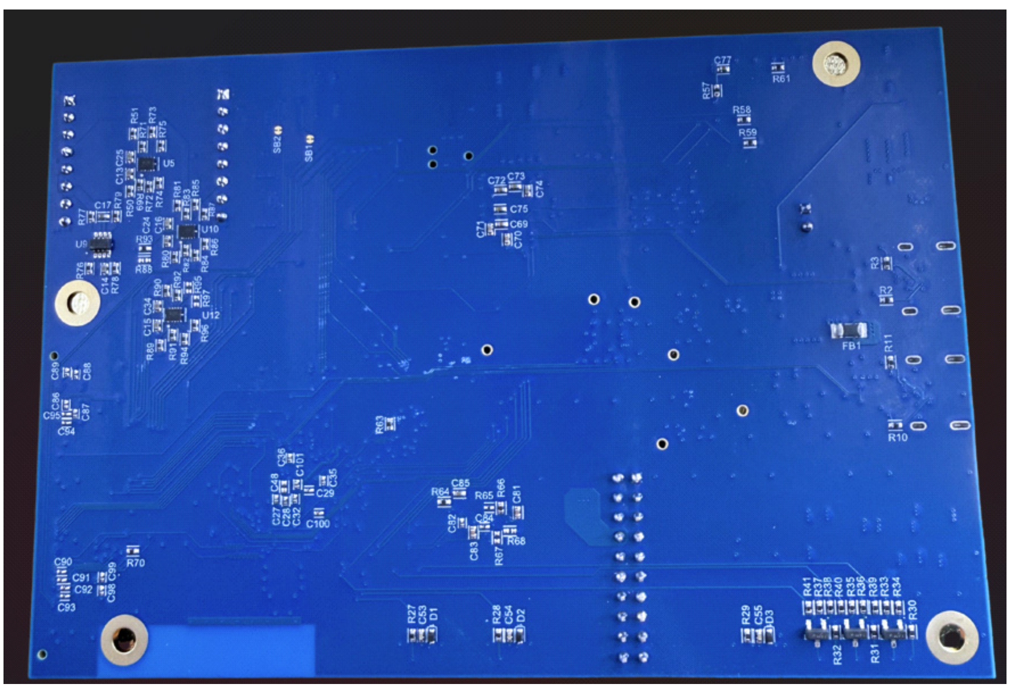
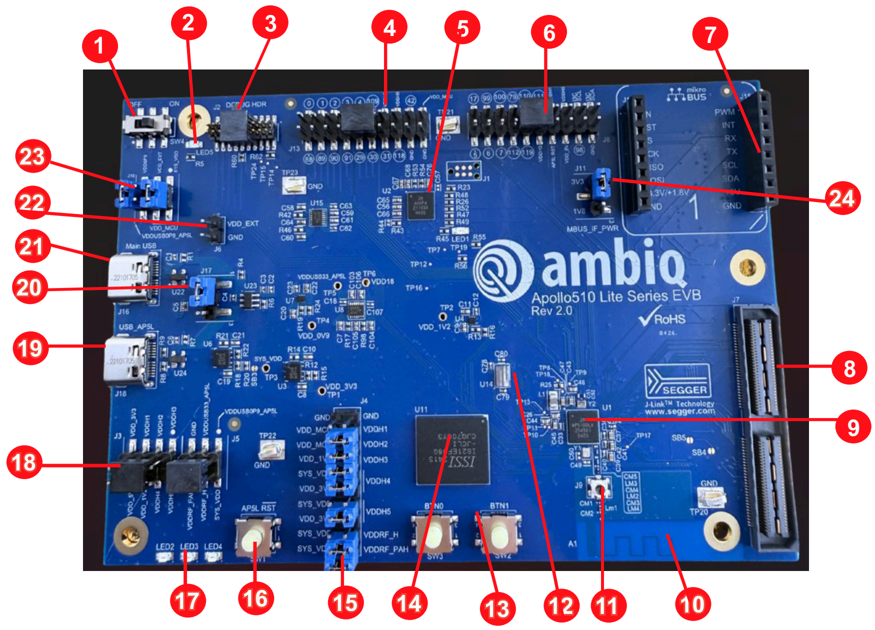


Figure 2. EVB Bottom View- Rev 2.0



1. Power Switch
2. Power LED
3. Debug Header
4. Dual-Row Header #1
5. JLINK Controller
6. Dual-Row Header #2
7. MikroBUS Connectors (2x)
8. High Speed Connector
9. Apollo510 Lite Series BGA MCU (AP510DLA-CBR)
10. PCB Trace Antenna
11. RF Switch/Connector
12. MSPI0 - APS512XXN-AOB4BI-WBRZ – Not populated[(1)]
13. User Buttons (2x)
14. eMMC - IS21EF08G-JCLI
15. Power Configuration Header
16. Reset Button
17. User LEDs (3x)
18. Power Test Points Header
19. Apollo510 LiteSeries USB Connector
20. Power Source Header
21. JLINK USB Connector
22. External Power Connector
23. MCU Supply Selection
24. MikroBUS Interface Power Selection

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1. See “EVB Known Issues” on page 30.

Figure 3. EVB Major Components

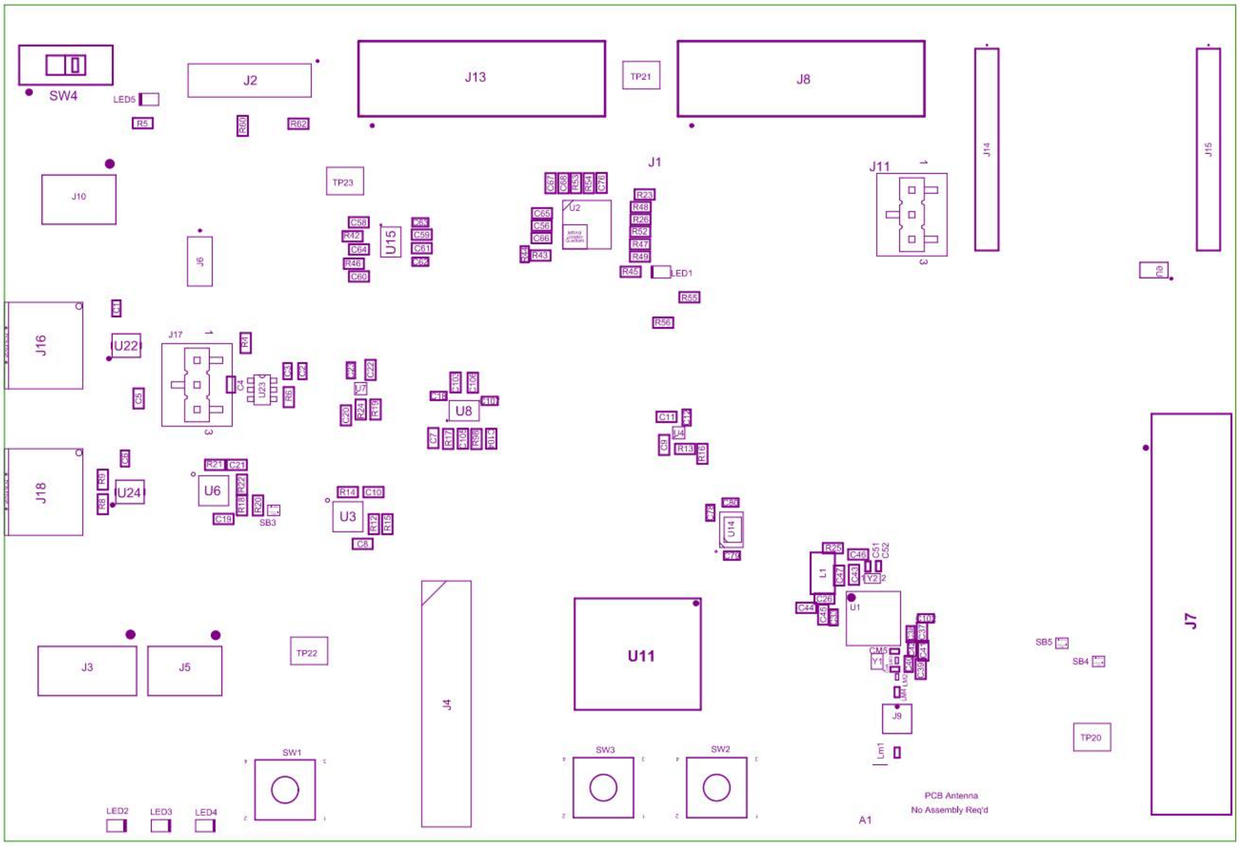


Figure 4. EVB Top Side Components

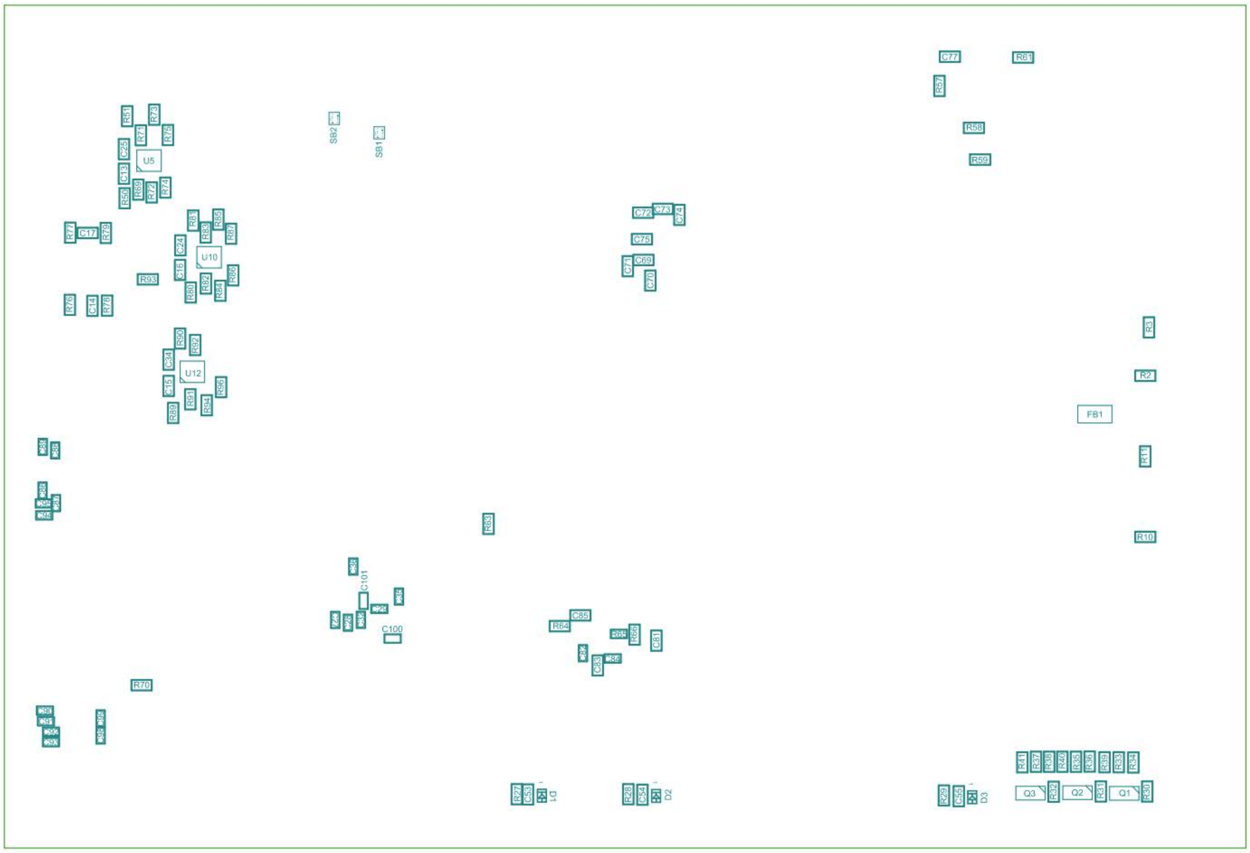


Figure 5. EVB Bottom Side Components

6. Secure Boot on the Apollo510 Lite Series SoC

The on-board Apollo510 Lite Series SoCs are preprogrammed with a Secure Bootloader and an uninitialized Customer Info Space, referred to as INFO0. Initial provisioning of the part would include programming a valid INFO0 and programming the main firmware image in the flash.

For information on changing the INFO0 settings as well as using the Secure Bootloader, please refer to the README.txt file found in the tools\apollo510L_scripts folder of the latest SDK release supporting the Apollo510 Lite Series. This folder contains a number of python scripts to demonstrate generation of INFO0 settings, customer main images, and the creation of images for the Wired Update protocol over UART.

Please consult your Ambiq sales team for any additional documentation on INFO0 settings or Secure Bootloader, and visit the Content Portal for security documentation for the Apollo510 Lite Series.

7. Header Pin Assignments

This section provides an overview of the Apollo510 Lite Series EVB connectivity and pin function options.

7.1 MikroBUS Headers

The Apollo510 Lite Series EVB provides a MikroBUS header to enable rapid prototyping. The interface is accessed through headers J14 and J15 as shown in Figure 6. The IO Voltage for this interface is selected by a jumper on J11 labeled MBUS_IF_PWR. Place the jumper between pins 1-2 for 3.3V (default) or pins 2-3 for 1.8V.

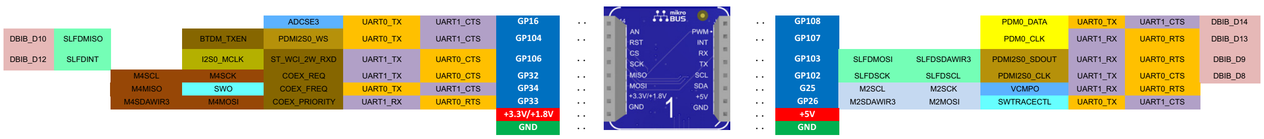


Figure 6. J14/J15 MikroBUS Headers - Function Options

7.2 General Purpose Headers

Function options for pins of general purpose headers J8 and J13 are as shown in Figure 7.

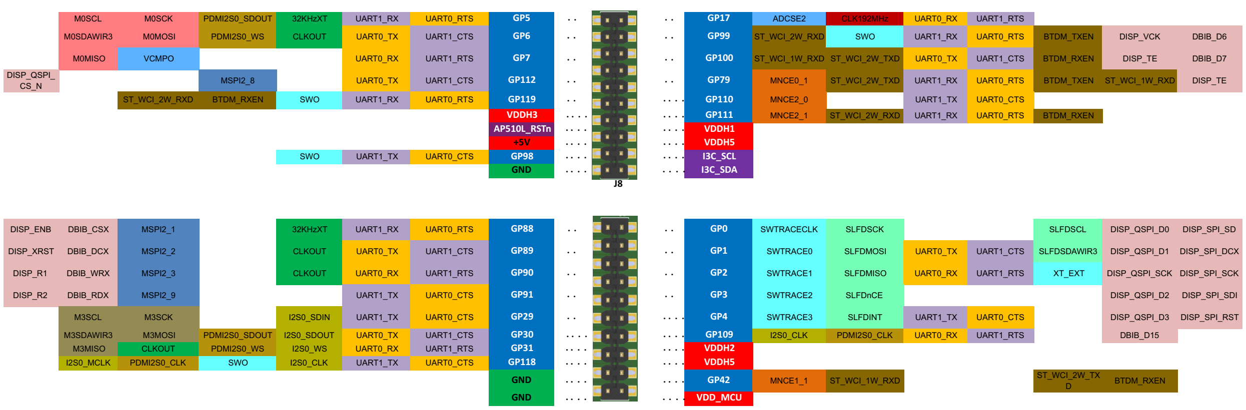


Figure 7. J8/J13 General Purpose Headers - Function Options

There are 2 solder bridges (SB1 and SB2) which will connect the I3C signals (I3C_SCL and I3C_SDA) from the GPIO header (J8) to 2 pins on the high-speed header (J7). By defaults, these solder bridges are shorted and the connection is made. These 2 solder bridges are located on the back of the EVB.

7.3 High-speed Header

Function options for pins of the high-speed header J7 are as shown in Figure 8.

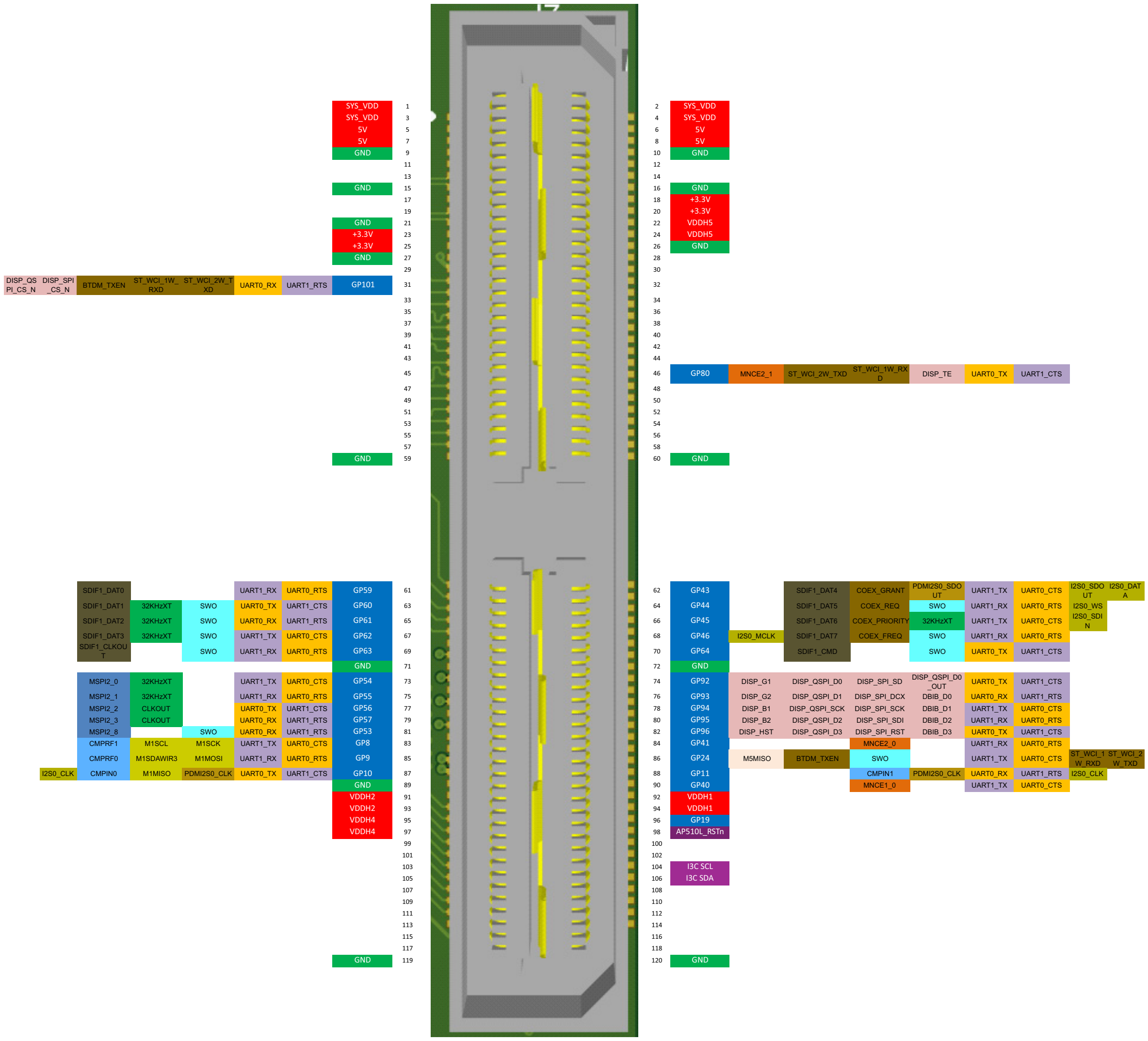


Figure 8. J7 High-speed Header - Function Options

Pin 82 of the high-speed header can be connected to either GPIO96 or GPIO58 using solder bridge. By default, this is connected to GPIO96.

Figure 9 shows the board view of the J7 high-speed header which is located on the right edge of the EVB. The protective tape should be removed from the header before use.

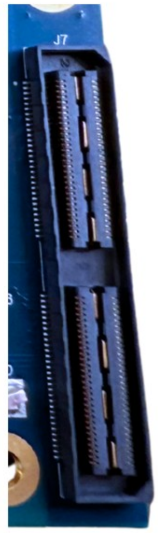


Figure 9. Board View of J7 High-speed Header

8. Debug Interface

Figure 10 shows the Apollo510 Lite Series EVB set up for standard debug using the on-board J-Link debugger, selected by the PWR_SRC header (J17) set to VBUS_JLINK, connected through the MAIN USB connector (J16).

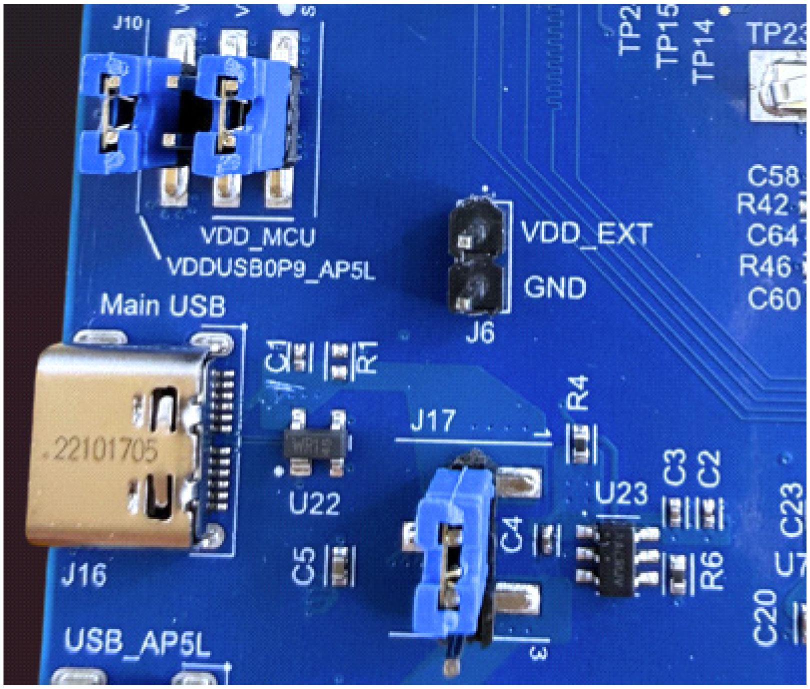


Figure 10. On-board J-Link Debug Connector (MAIN USB)

The debug interface is supported by standard J-Link drivers from Segger. Please refer to “Software Development Tools” on page 19 for more details on J-Link debug support.

8.1 Use of External Debugger

This EVB also supports the use of an external SWD debug interface through a 20-pin debug-in header (DEBUG HDR – J2) as shown in Figure 11. See the EVB schematic for connector pinout.

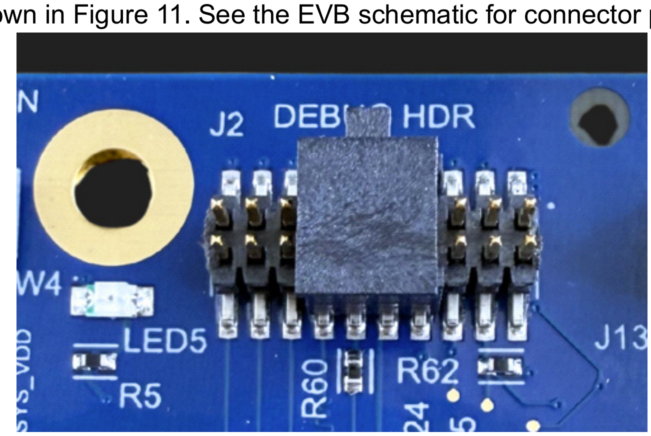


Figure 11. J2 Debug-In Header

No jumper changes are required to use an external debug adapter. Simply connect the external debug adapter with a ribbon cable connector to the “DEBUG HDR” header.

NOTE: Remove protective guard before attempting to connect to the debug header.

9. Software Development Tools

The standard Segger J-Link debug interface is used on the Apollo510 Lite Series EVB. Regardless of IDE used, please install the Segger J-Link software - see https://www.segger.com/downloads/jlink. Refer to the AmbiqSuite SDK for version numbers of the IDEs used for that release, and see the \Ambiq-Suite\debugger_updates\ folder in the AmbiqSuite SDK for interim updates for Keil and JLINK.

IMPORTANT NOTE
When installing the Segger J-Link software described above, it may be necessary to select the “Install Legacy USB Driver” option in order to properly enable the USB connection. This option is not selected by default in the Segger installation setup dialog box, so the checkbox has to be checked to install the legacy USB driver. (This is the only default installation option that needs to be changed when installing the software.)

10. Power Supply Options and Measuring Current

The Apollo510 Lite Series EVB is intended to operate off a 5 V supply, which is used to generate down-stream voltages.

There are two options for the main power supply (VDD_MCU) for the EVB SoC (configured via J10):

- Operate at a nominal 1.8 V regulated down from the VDD_5V supply to source the on-board power rail SYS_VDD (default). Note that this voltage can be adjusted to 1.9 V by cutting SB3 shown on the Power Supplies page of the EVB schematic.
- Provide externally-supplied power via J6 in Figure 12.

NOTE: If externally supplying VDD_MCU from VDD_EXT, the supplied voltage range is 1.71 V to 2.2 V.

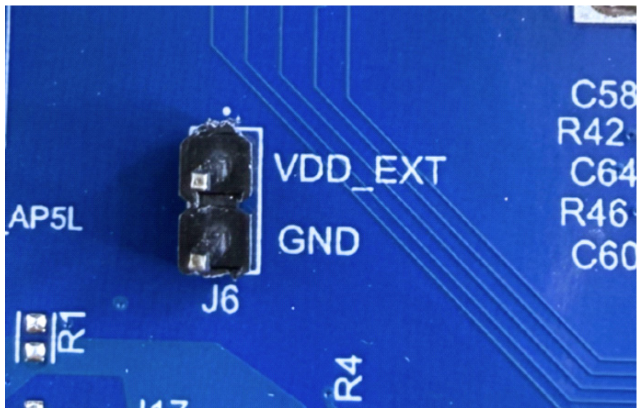


Figure 12. J6 External Supply Header

The EVB utilizes jumpers for connecting and disconnecting rails from power supplies, whether generated on-board or off-board. The following figures show the jumper connection strategy among various on-board power supplies and the SoC's power rails.

Figure 13 shows the power sourcing options for VDD_MCU.

VDD0P9 is connected to VDDUSB0P9_AP5L via a jumper on pins 5-6 of J10. VDD0P9 is a 0.9 V supply generated by an LDO in the SoC and is used to power the 0.9 V supply for the USB. The header will allow current measurement on that rail.

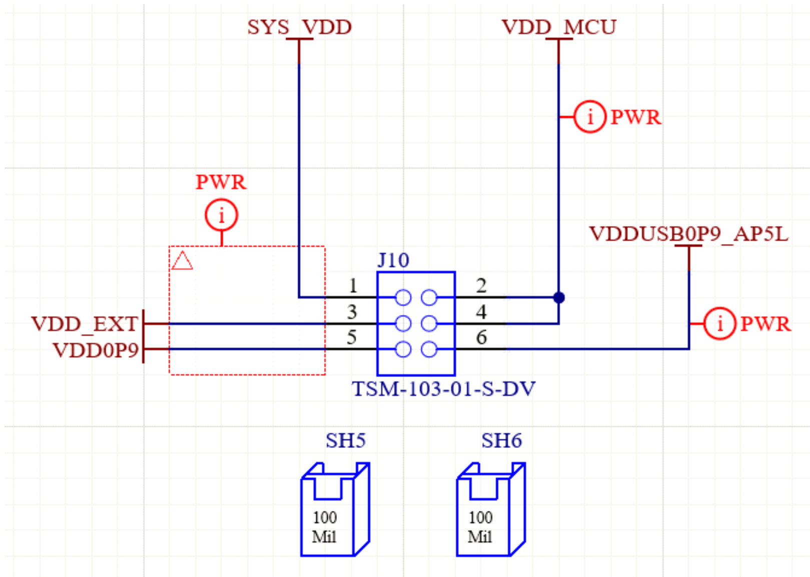


Figure 13. J10 Power Supply Jumper Connections

The J10 default jumper configuration is as shown in Figure 14 and in bold in Table 3.

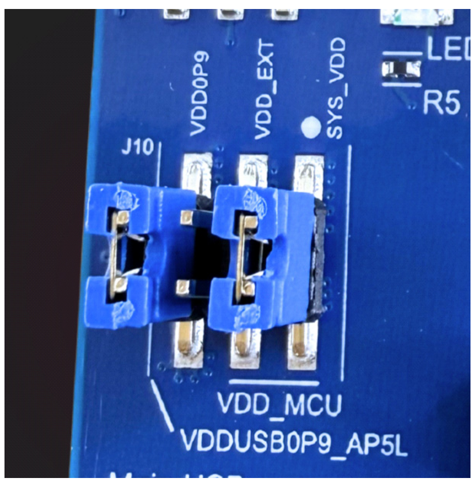


Figure 14. J10 Default Jumper Configuration

Table 2: J10 Jumper Configuration Table (Default Configuration in Bold)

Power Supply Source	From Header Pin	To Header Pin	Power Supply Destination
SYS_VDD	**J10-1**	**J10-2**	**VDD_MCU**
VDD_EXT	J10-3	J10-4	VDD_MCU
VDD0P9	**J10-5**	**J10-6**	**VDDUSB0P9_AP510L**

Figure 15 shows the power sourcing for VDDH1, VDDH2, VDDH3, VDDH4, VDDH5, VDDRF_H, and VDDRF_PAH.

- VDDH1 and VDDH2 are always sourced from VDD_MCU (Voltage depending on the selection on J10. By default they are 1.8 V).
- VDDH3 is always sourced from 1.2V.
- VDDH4 and VDDH5 may be sourced from default 1.8 V (SYS_VDD) or 3.3 V (VDD_3V3).
- VDDRF_H and VDDRF_PAH are always sourced from 1.8 V (SYS_VDD).

This header can be used to measure current on any of the supplies.

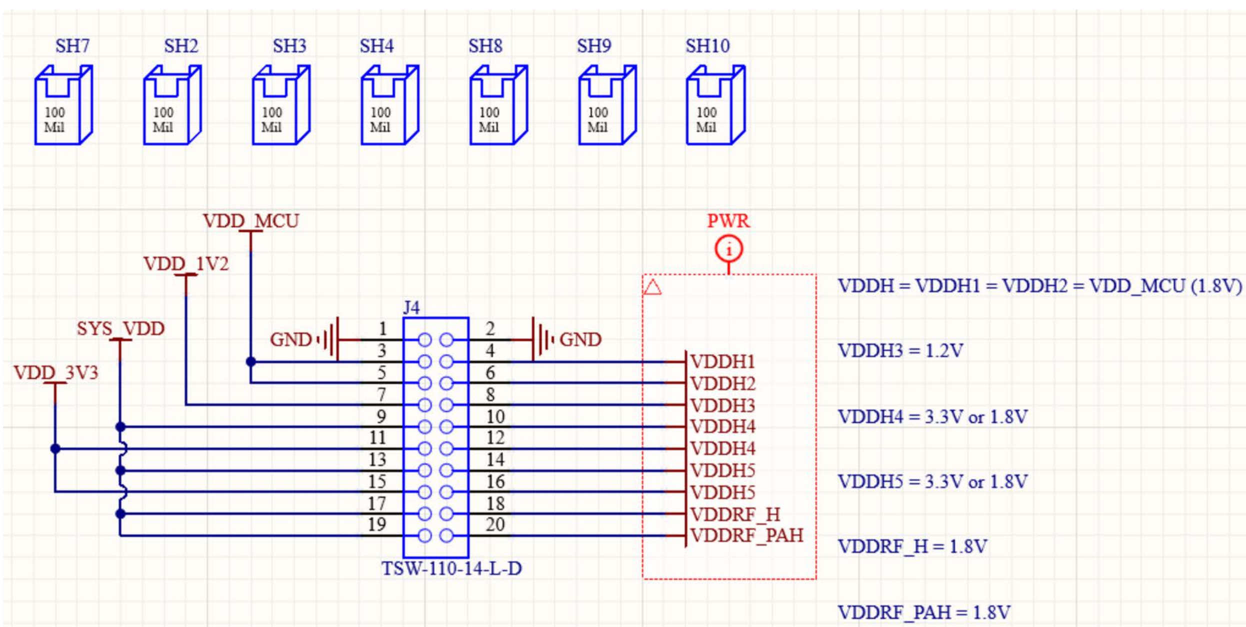


Figure 15. J4 Power Supply Jumper Connections

The J4 default jumper configuration is as shown in Figure 16 and Table 3.

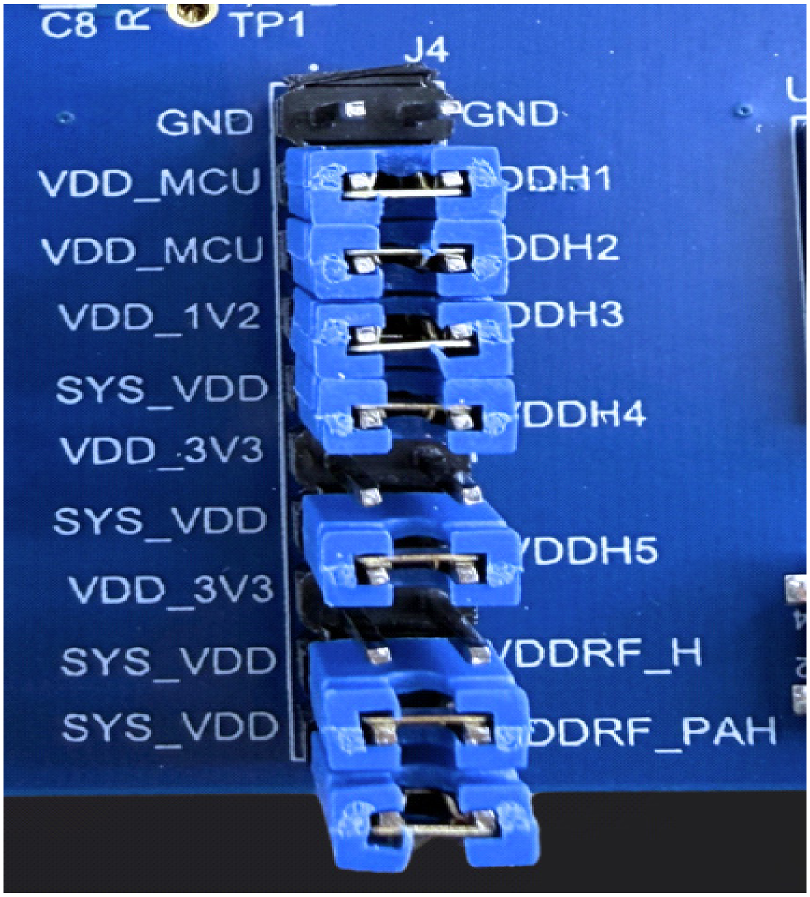


Figure 16. J4 Default Jumper Configuration

Table 3: J4 Jumper Configuration Table (Default Configuration in Bold)

Power Supply Source	From Header Pin	To Header Pin	Power Supply Destination
GND	**J4-1**	**J4-2**	**GND**
VDD_MCU	**J4-3**	**J4-4**	**VDDH1**
VDD_MCU	**J4-5**	**J4-6**	**VDDH2**
VDD_1V2	**J4-7**	**J4-8**	**VDDH3**
SYS_VDD	**J4-9**	**J4-10**	**VDDH4**
VDD_3V3	J4-11	J4-12	VDDH4
SYS_VDD	**J4-13**	**J4-14**	**VDDH5**
VDD_3V3	J4-15	J4-16	VDDH5
SYS_VDD	**J4-17**	**J4-18**	**VDDRF_H**
SYS_VDD	**J4-19**	**J4-20**	**VDDRF_PAH**

10.1 USB 3.3 V and Display Load Switch Circuit

Figure 17 shows the USB and Display dual load switch circuit producing the voltage supplied to VDDUSB33_AP510L (for USB) and VDD18 (for Display).

Note that VDDUSB0P9_AP510L (0.9 V supply for the USB) is connected through a jumper to the MCU LDO output pin VDD0P9, therefore no additional load switch is needed for that.

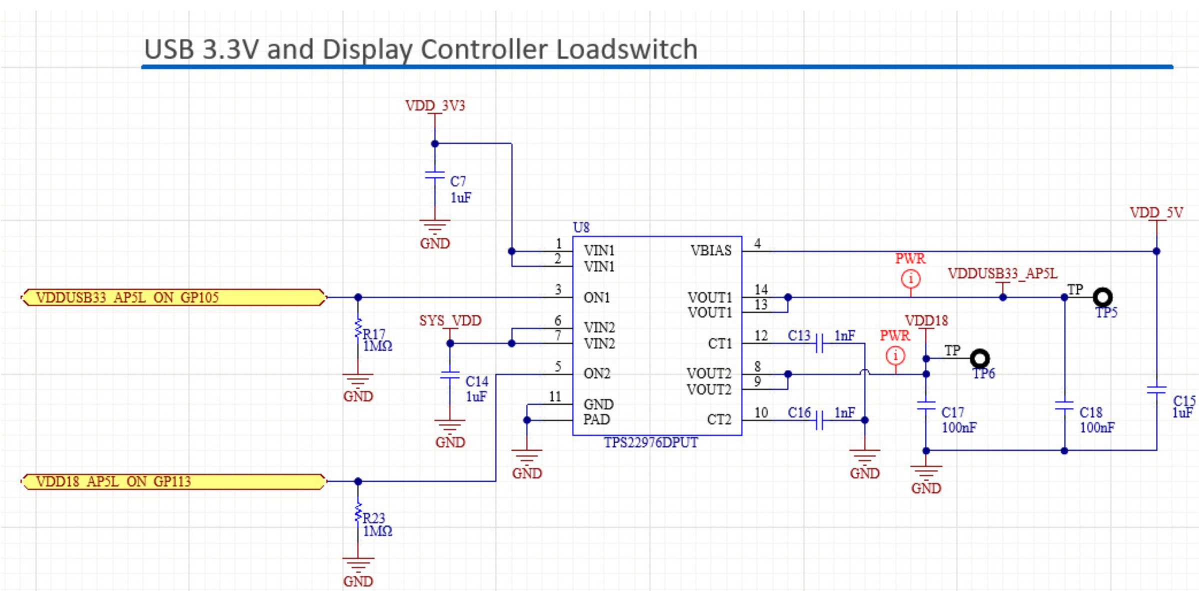


Figure 17. USB 3.3 V and Display Load Switch Circuit

10.2 Monitoring or Externally Supplying Supply Voltages

As shown in Figure 18, headers J3 and J5 provide easy access to the various system and chip-level power supplies present on the EVB. These can be used to monitor voltage or provide externally generated power to each specific rail after assuring that the on-board supply has been disconnected.

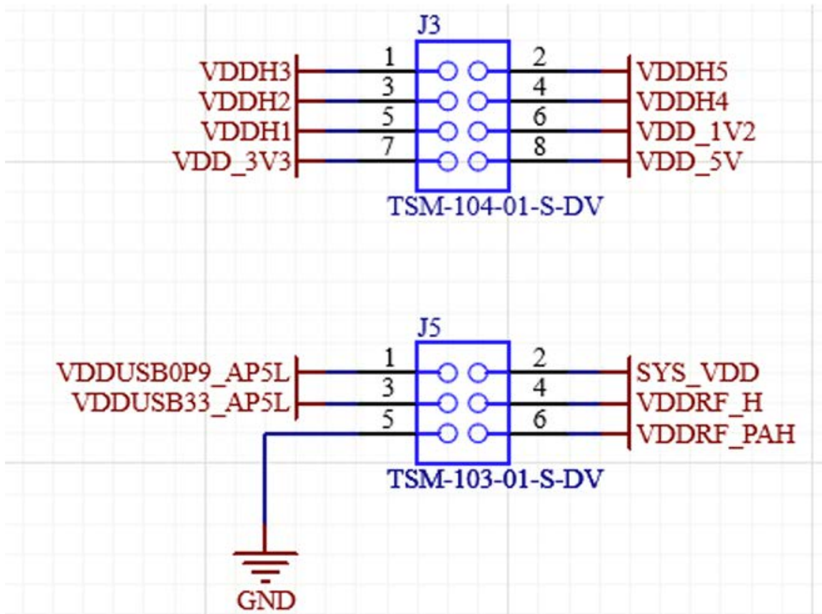


Figure 18. J3 and J5 Voltage Test Point Headers

The J3 and J5 headers are as shown in Figure 19. The header guard may need to be removed before connecting to or probing the header pins.

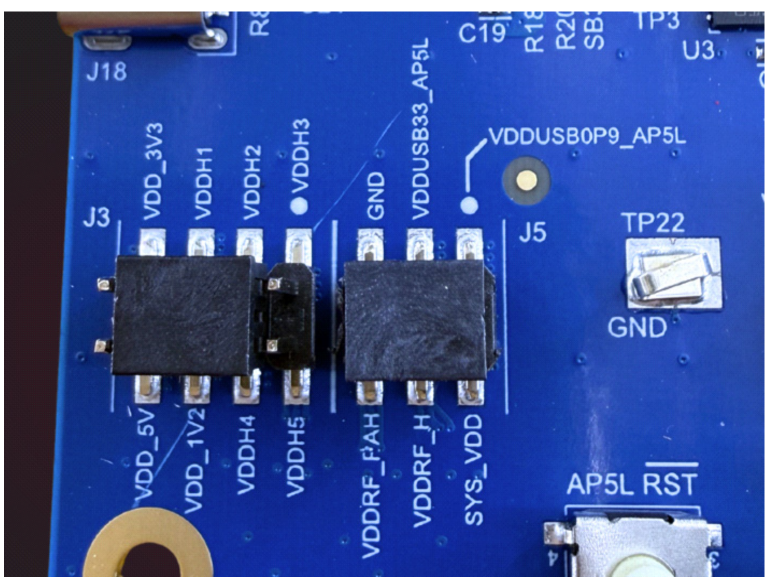


Figure 19. Board View of J3 and J5 Voltage Test Points Headers

10.3 Measuring Current

Current consumption of the Apollo510 Lite Series EVB can be measured by connecting an ammeter between the corresponding DUT supplies. Refer to Figure 13 or Figure 15 to measure the current draw from the power supply of interest. Before using an ammeter, turn the power off, remove the corresponding jumper and install the ammeter properly prior to powering the board back on. When the current measurements have been completed, reposition the jumper at its former location.

10.4 BLE Power Consumption Measurement for the Apoll0510D Lite SoC

This section describes the procedure for measuring BLE power consumption using the Apollo510D Lite SoC on Revision 2.0 of the EVB. It covers preparation of the EVB as well as connection to, and current measurement with, the Joulescope JS220.

10.4.1 Setup

1. Set up the HW connection as shown below to measure the BLE power consumption:
    A. The EVB's power source is via the Main USB (J16) connected to a PC (used to program the binary). Perform the following setup before applying power.
    B. Remove jumper between pin 19 (SYS_VDD) and pin 20 (VDDRF_PAH) on header J4.
    C. Remove jumper between pin 17 (SYS_VDD) and pin 18 (VDDRF_H) on header J4.
    D. Remove jumper between pin 1 (SYS_VDD) and pin 2 (VDD_MCU) on header J10.
    E. Connect pin 20 (VDDRF_PAH) and pin 18 (VDDRF_H) on header J4 to pin 2 (VDD_MCU) on header J10 and to the Joulescope's "Current-" connector.
    F. Connect pin 1 (SYS_VDD) on header J4 to the Joulescope's "Voltage+" connector and the "+Current" connector.
    G. Connect the EVB ground test point TP23 to the Joulescope's "-Voltage" connector. (See "EVB Top View - Rev 2.0" on page 9.)

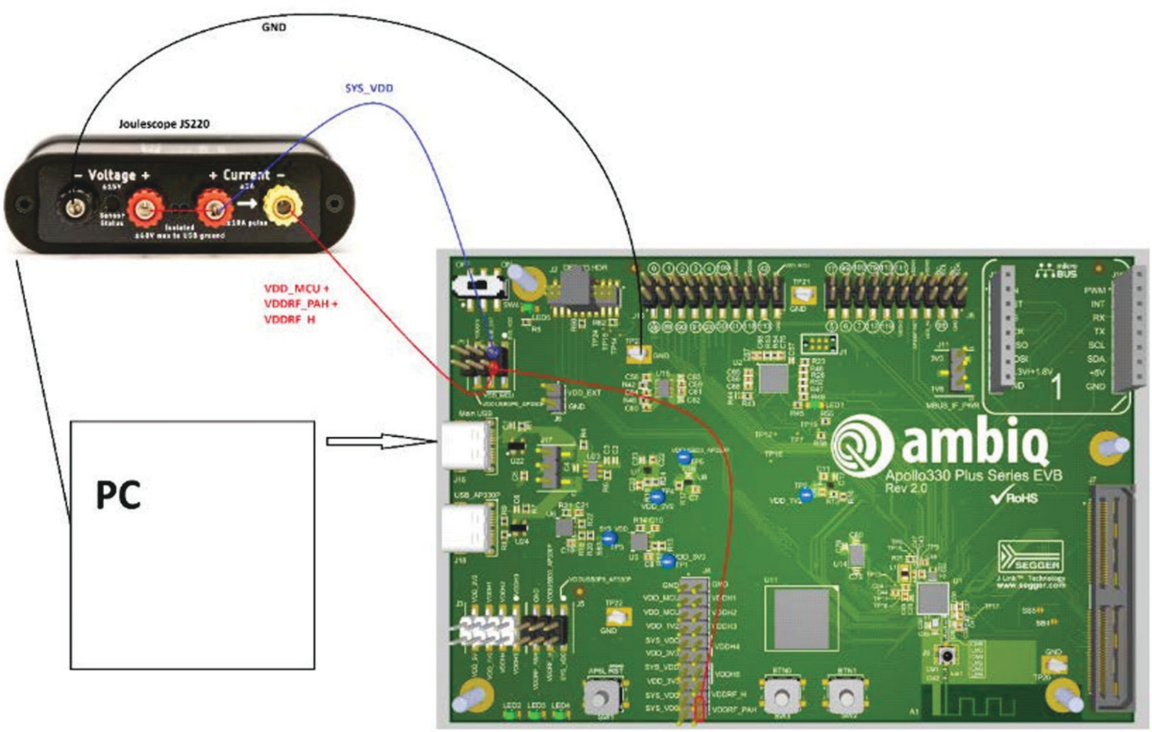


Figure 20. Joulescope to EVB Power Connections

2. Build and download the uart_hci_bridge.bin on the Apollo 510 Lite EVB.

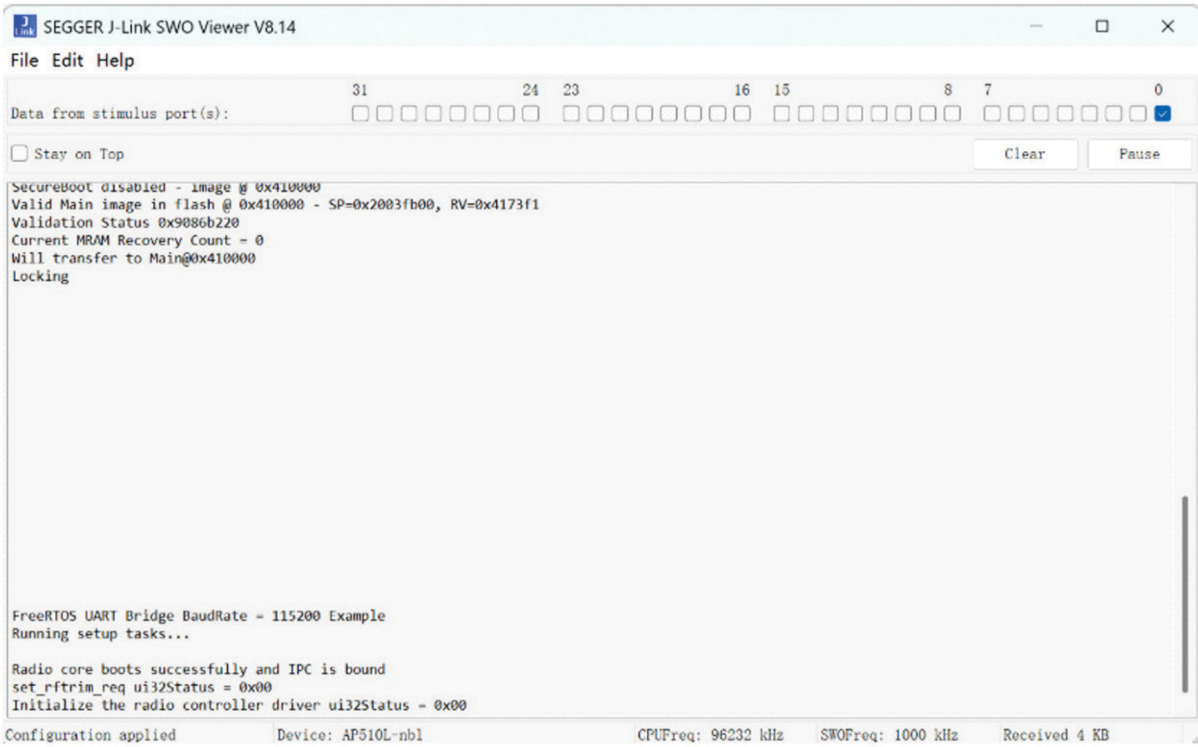


Figure 21. Download Messages in J-Link SWO Viewer

3. Refer to the latest "Guidelines for RF Testing in Apollo-Blue Family" document for HCI command lists to run the test.

10.4.2 Measuring Baseline Current

1. Reset the radio using the HCI reset command (0x01 0x03 0x0C 0x00).
2. Check the average current/power reading for VDD_MCU/VDDRF_H/VDDRF_PAH on the Joule-scope.

10.4.3 Measuring Radio RX Mode Current

1. Enable the Radio LE RX mode by the HCI_LE_Receiver_test command.
2. Check the average current/power reading for VDD_MCU/VDDRF_H/VDDRF_PAH on the Joule-scope.
3. Disable the Radio LE RX mode by the HCI LE Test command (0x01 0x1F 0x20 0x00).

10.4.4 Setting HCI_LE_Receiver_Test Command Format

Table 4 lists the format and content of an example HCI LE Receiver test command for channel 5, 1 MHz RX frequency, modulation index 0, using opcode 0x2033: 0x01 0x33 0x20 0x03 0x05 0x01 0x00.

Table 4: Example of HCI_LE_Receiver_Test Command Format

HCI Command Header	Opcode Low	Opcode High	Parameter Length	PHY	Frequency	Modulation Index
0x01	0x33	0x20	0x03	0x05	0x01	0x00

10.4.5 Setting HCI_LE_Test_End Command Format

Table 5 lists the format and content of an example HCI LE Test End command with opcode 0x201F: 0x01 0x1F 0x20 0x00.

Table 5: Example of HCI_LE_Test_End Command Format

HCI Command Header	Opcode Low	Opcode High	Parameter Length
0x01	0x1F	0x20	0x00

10.4.6 Measuring Radio TX Mode Current

1. Set the specific TX power level with the vendor command of set LE transmit power level.
2. Enable the Radio LE TX Continuous wave without modulation mode with the HCI_LE_Transmitter_test command.
3. Check the average current/power reading for VDD_MCU/VDDRF_H/VDDRF_PAH on Joulescope.
4. Disable the Radio LE TX mode with the HCI LE Test command (0x01 0x1F 0x20 0x00).

The TX-mode current is equal to the measured current less the baseline current.

10.4.7 Setting LE Transmit Power Level Command Format

Table 6 lists the format and content of an example which sets the LE transmit power level to 0 dBm using opcode 0xFC83: 0x01 0x83 0xFC 0x01 0x00.

Table 6: Example of HCI_LE_Test_End Command Format

HCI Command Header	Opcode Low	Opcode High	Parameter Length	Power Level
0x01	0x83	0xFC	0x01	0x00

To set the power level to -2 dBm, the command would be: 0x01 0x83 0xFC 0x01 0xFE, as the power level is int8_t type and a negative number is represented in complement form. The enumerated type for the power level range would be as below:

```
typedef enum
{
    TX_POWER_LEVEL_MINUS_20P0_dBm = -20,
    TX_POWER_LEVEL_MINUS_18P0_dBm = -18,
```



```
    TX_POWER_LEVEL_MINUS_16P0_dBm = -16,
    TX_POWER_LEVEL_MINUS_14P0_dBm = -14,
    TX_POWER_LEVEL_MINUS_12P0_dBm = -12,
    TX_POWER_LEVEL_MINUS_10P0_dBm = -10,
    TX_POWER_LEVEL_MINUS_8P0_dBm = -8,
    TX_POWER_LEVEL_MINUS_6P0_dBm = -6,
    TX_POWER_LEVEL_MINUS_4P0_dBm = -4,
    TX_POWER_LEVEL_MINUS_2P0_dBm = -2,
    TX_POWER_LEVEL_0P0_dBm = 0,
    TX_POWER_LEVEL_PLUS_1P0_dBm = 1,
    TX_POWER_LEVEL_PLUS_2P0_dBm = 2,
    TX_POWER_LEVEL_PLUS_3P0_dBm = 3,
    TX_POWER_LEVEL_PLUS_4P0_dBm = 4,
    TX_POWER_LEVEL_PLUS_5P0_dBm = 5,
    TX_POWER_LEVEL_PLUS_6P0_dBm = 6,
    TX_POWER_LEVEL_PLUS_7P0_dBm = 7,
    TX_POWER_LEVEL_PLUS_8P0_dBm = 8,
    TX_POWER_LEVEL_PLUS_9P0_dBm = 9,
    TX_POWER_LEVEL_PLUS_10P0_dBm = 10,
    TX_POWER_LEVEL_PLUS_11P0_dBm = 11,
    TX_POWER_LEVEL_PLUS_12P0_dBm = 12,
    TX_POWER_LEVEL_PLUS_13P0_dBm = 13,
    TX_POWER_LEVEL_INVALID,
} txPowerLevel_t;
```

10.4.8 Setting HCI_LE_Transmitter_test Command Format

Table 7 lists the format and content of an example to run a HCI LE Transmitter test command using channel 5, packet type 0x04, packet length 0x11,1 MHz TX frequency, packet type 0x10 (continuous wave without modulation). The command using opcode 0x2034 would be: 0x01 0x34 0x20 0x04 0x05 0x11 0x10 0x01.

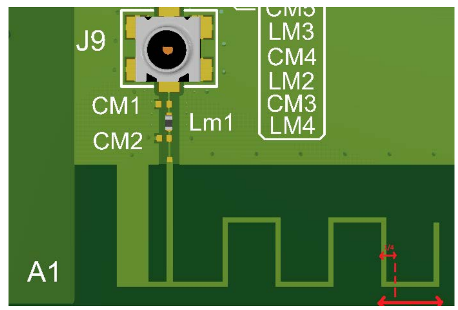
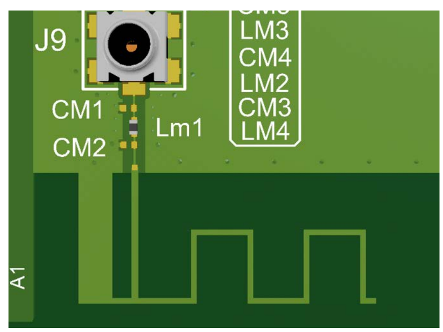
Table 7: Example of HCI_LE_Test_End Command Format

HCI Command Header	Opcode Low	Opcode High	Parameter Length	PHY	Parameter (Packet) Length	Packet Type	Frequency
0x01	0x34	0x20	0x04	0x05	0x11	0x10	0x01

11. EVB Known Issues

Table 8 lists the known issues with the Apollo510 Lite Series EVB Revision 2.0.

Table 8: Apollo510 Lite **Series EVB Revision 2.0 - Known Issues**

Affected EVB	Issue	Rework
Apollo510 Lite Series EVB Revision 2.0	PSRAM scan window issue at 1.2 V supply	All boards have the PSRAM (U14) and its corresponding passive components (C78, C79, C80, and R63) de-populated due to this issue.
Apollo510 Lite Series EVB Revision 2.0	RF performance optimization	The trace antenna must be cut at about ¼ of the segment length as shown below for the best RF performance. From:  To: 

12. Ordering Information

Table 9: EVB Ordering Information

Device Name	Orderable Part Number	EVB Revision	SoC
Apollo510D Lite EVB	AP510DLEVB	2.0	Apollo510D Lite BGA

Table 10: Apollo510 Lite Series SoC Ordering Information

Device Name[a]	Commercial Temp Range (-20°C to 70°C)	Industrial Temp Range (-40°C to 85°C)	Package Type	GPIOs	NVM (MRAM)	SRAM	Connectivity	Package[b] Size (mm)
Apollo510 Lite	AP510NLA-CCR	-	CSP	68	2 MB	2 MB	No Connectivity	4.047 x 3.948 x 0.510(max) 110-pin
Apollo510 Lite	AP510NLA-CBR	-	BGA	120	2 MB	2 MB	No Connectivity	5.3 x 5.3 x 0.8(max) 169-pin
Apollo510B Lite	-	AP510BLA-ICR	CSP	68	2 MB	2 MB	BLE 5.4	4.047 x 3.948 x 0.510(max) 110-pin
Apollo510D Lite	AP510DLA-CCR	-	CSP	68	2 MB	2 MB	BLE 5.4, BT Classic	4.047 x 3.948 x 0.510(max) 110-pin
Apollo510D Lite	AP510DLA-CBR	AP510DLA-IBR	BGA	120	2 MB	2 MB	BLE 5.4, BT Classic	5.3 x 5.3 x 0.8(max) 169-pin

a. The silicon revision is identified by the first letter in the bottom row of the package's top marking.
b. Packing: Tape and Reel

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